



Integrated Device Technology, Inc.

# CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256SA

### FEATURES:

- 32K x 8 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - Military: 15/20/25ns
  - Commercial: 12/15/20/25ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Military product compliant to MIL-STD-883, Class B
- Available in 28-pin Sidebraze DIP, Plastic DIP, Plastic SOJ, and 32-pin LCC packages

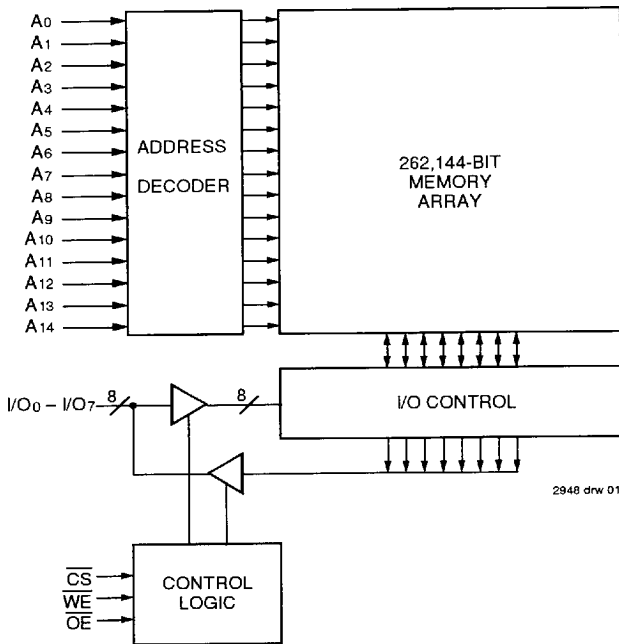
### DESCRIPTION:

The ID71256SA is a 262,144-bit high-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The ID71256SA has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the ID71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The ID71256SA is packaged in 28-pin 300 mil Sidebraze DIP, 28-pin 300 mil Plastic DIP, 28-pin 300 mil Plastic SOJ, and 32-pin Leadless Chip Carrier packages.

### FUNCTIONAL BLOCK DIAGRAM



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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**MAY 1994**

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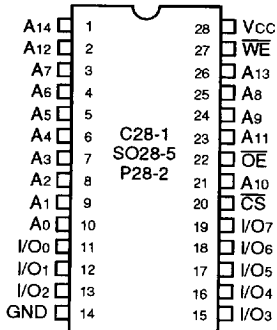
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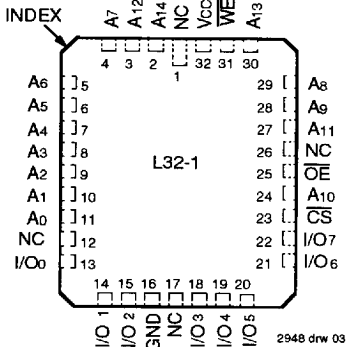
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**PIN CONFIGURATIONS**



DIP/SOJ TOP VIEW 2948 drw 02



LCC TOP VIEW 2948 drw 03

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Com'l.	Mil.	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V

**CAPACITANCE**

(T<sub>A</sub> = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	11	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	11	pF

**NOTE:**

- This parameter is guaranteed by device characterization, but not production tested.

**RECOMMENDED DC OPERATING CONDITIONS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> +0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

- V<sub>IL</sub> (min.) = -1.5V for pulse width less than 10ns, once per cycle.

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max, V <sub>IN</sub> = GND to V <sub>CC</sub>	—	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min	2.4	—	V

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**DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

(V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub>-0.2V)

Symbol	Parameter	71256SA12		71256SA15		71256SA20		71256SA25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I <sub>CC</sub>	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max, f = f <sub>MAX</sub> <sup>(2)</sup>	160	—	150	170	145	150	145	150	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , Outputs Open, V <sub>CC</sub> = Max, f = f <sub>MAX</sub> <sup>(2)</sup>	50	—	40	50	40	45	40	45	mA
I <sub>SB1</sub>	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$ , Outputs Open, V <sub>CC</sub> = Max, f = 0 <sup>(2)</sup> V <sub>IN</sub> ≤ V <sub>LC</sub> or V <sub>IN</sub> ≥ V <sub>HC</sub>	15	—	15	30	15	30	15	30	mA

**NOTES:**

- All values are maximum guaranteed values
- f<sub>MAX</sub> = 1/t<sub>rc</sub> (all address inputs are cycling at f<sub>MAX</sub>), f = 0 means no address input lines are changing

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**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

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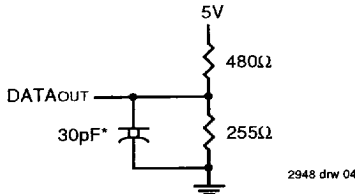


Figure 1. AC Test Load

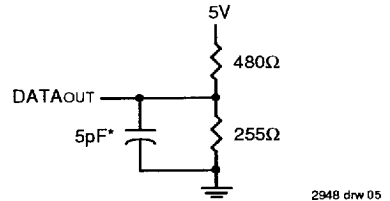


Figure 2. AC Test Load  
(for t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>OW</sub>, and t<sub>WHZ</sub>)

\*Including jig and scope capacitance.

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges)

Symbol	Parameter	71256SA12 <sup>(1)</sup>		71256SA15		71256SA20		71256SA25		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	20	—	25	ns
t <sub>ACS</sub>	Chip Select Access Time	—	12	—	15	—	20	—	25	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	0	6	0	7	0	10	0	11	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	6	—	7	—	10	—	11	ns
t <sub>OLZ</sub> <sup>(2)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(2)</sup>	Output Disable to Output in High-Z	0	6	0	6	0	8	0	10	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t <sub>PU</sub> <sup>(2)</sup>	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(2)</sup>	Chip Deselect to Power Down Time	—	12	—	15	—	20	—	25	ns
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t <sub>AW</sub>	Address Valid to End of Write	9	—	10	—	15	—	20	—	ns
t <sub>CW</sub>	Chip Select to End of Write	9	—	10	—	15	—	20	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	9	—	10	—	15	—	20	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End of Write	6	—	7	—	11	—	13	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(2)</sup>	Output Active from End of Write	4	—	4	—	4	—	4	—	ns
t <sub>WHZ</sub> <sup>(2)</sup>	Write Enable to Output in High-Z	0	6	0	6	0	10	0	11	ns

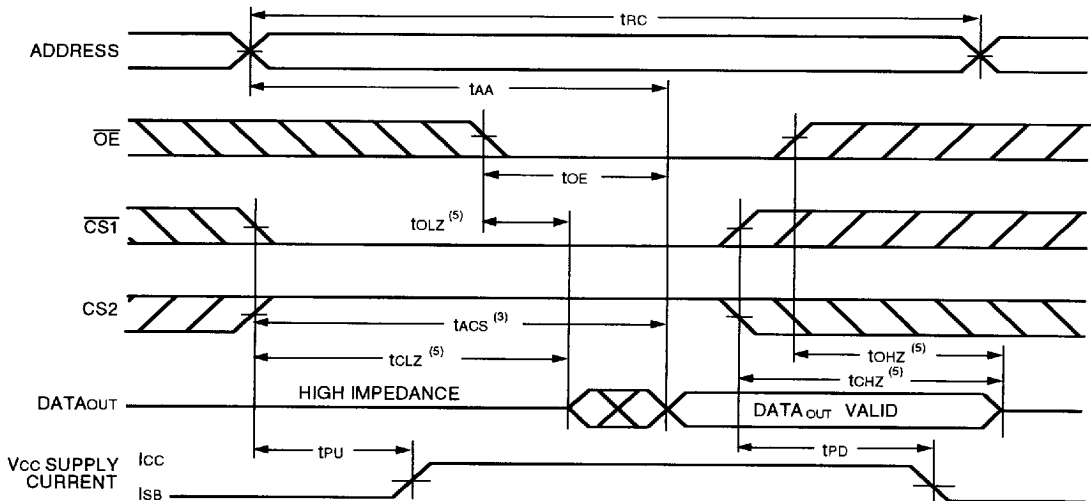
**NOTES:**

- 0° to +70°C temperature range only
- This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested

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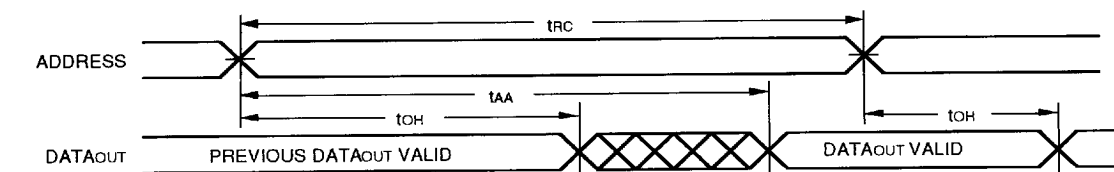
**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



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**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1,2,4)</sup>**

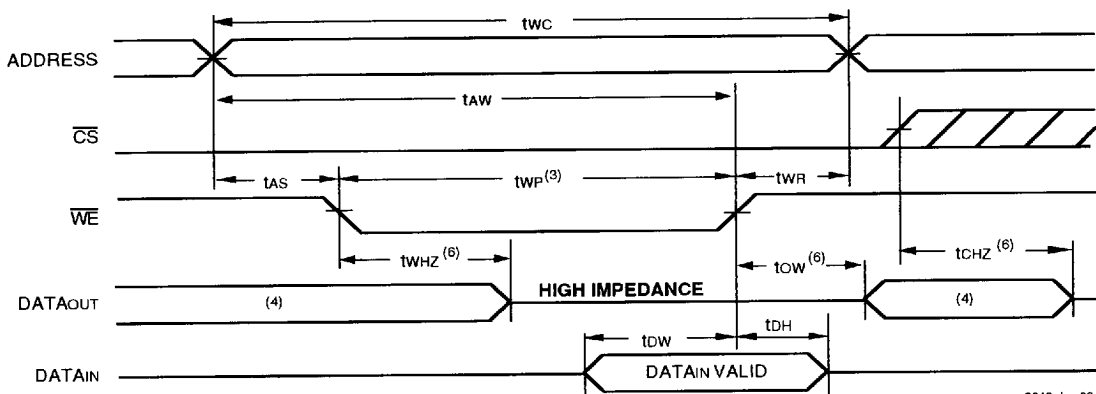


**NOTES:**

1.  $\overline{WE}$  is HIGH for Read Cycle
2. Device is continuously selected,  $\overline{CS}$  is LOW
3. Address must be valid prior to or coincident with the later of  $\overline{CS}$  transition LOW, otherwise  $t_{AA}$  is the limiting parameter
4.  $\overline{OE}$  is LOW
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

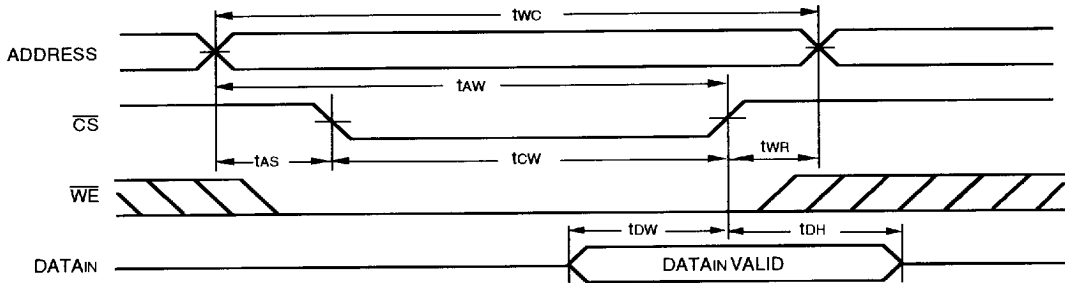
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**TIMING WAVEFORM OF WRITE CYCLE NO.1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1,2,3,5)</sup>**



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**TIMING WAVEFORM OF WRITE CYCLE NO.2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1,2,5)</sup>**

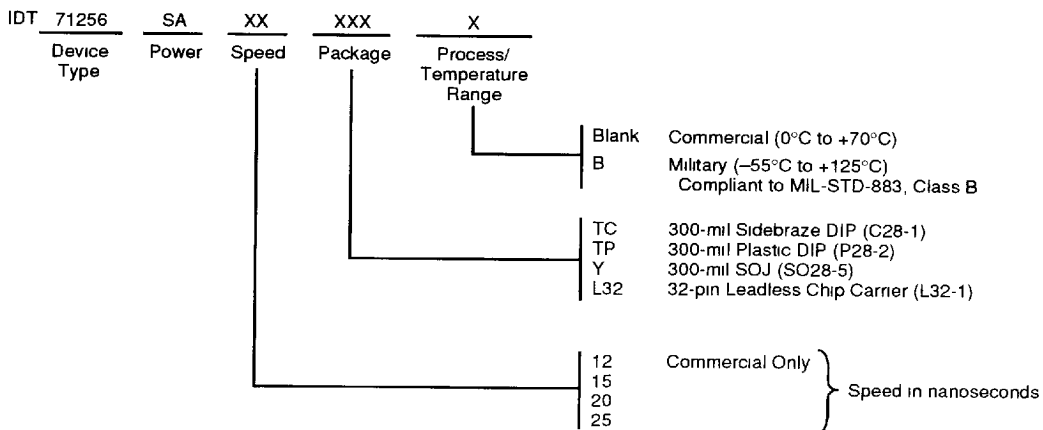


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**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions
2. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$
3.  $\overline{OE}$  is continuously HIGH. If during a  $\overline{WE}$  controlled write cycle  $\overline{OE}$  is LOW,  $t_{WP}$  must be greater than or equal to  $t_{WHZ} + t_{OW}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified  $t_{WP}$
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state

ORDERING INFORMATION



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