

SANYO

No.3619A

LC7232**Single-chip PLL and Microcontroller
with LCD Driver****OVERVIEW**

The LC7232 is a single-chip microcontroller that incorporates a phase-locked loop (PLL), which can operate up to 150 MHz, and a liquid-crystal display (LCD) driver, making it ideal for digital tuners. It incorporates frequency and period measurement circuits, and a large number of input/output ports on chip.

The LC7232 comprises on-chip RAM and ROM, a programmable high-speed divider, a 6-bit analog-to-digital converter, two 8-bit digital-to-analog converters and a low-voltage detection reset circuit.

The LC7232 operates from a single 5 V supply and is available in 80-pin QIPs.

FEATURES

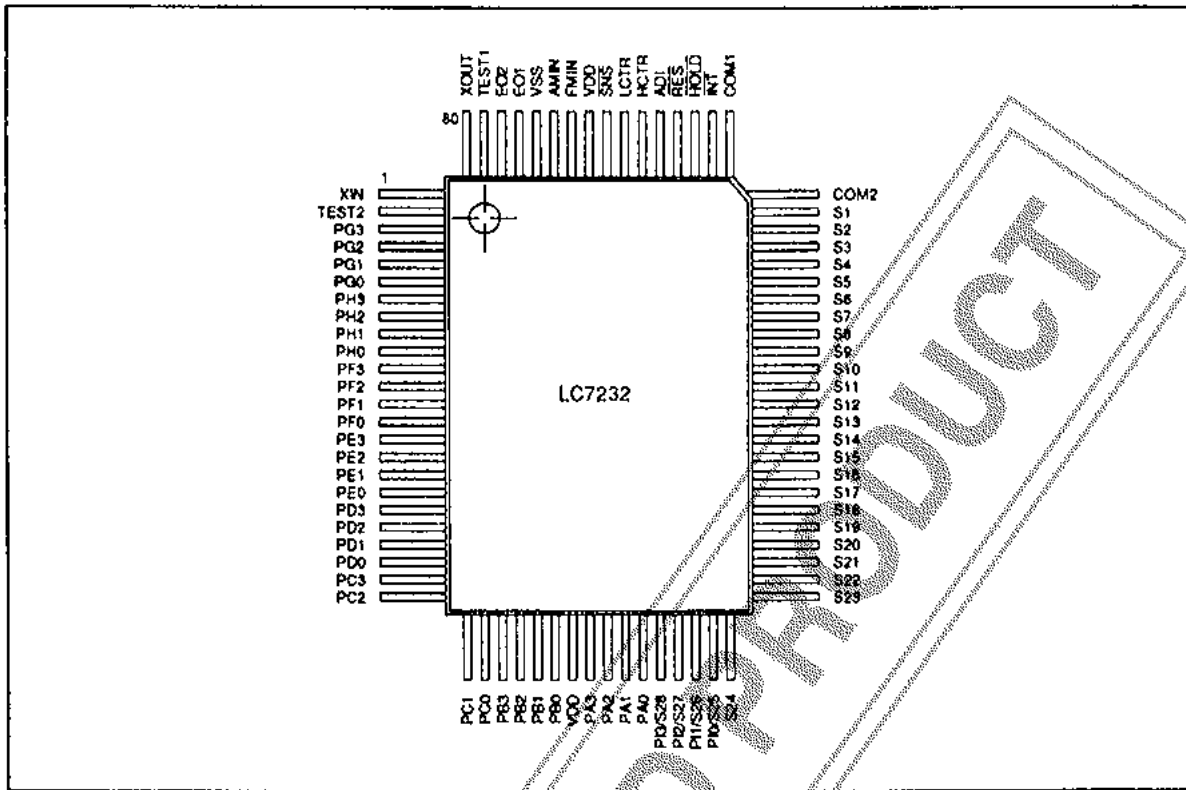
- 150 MHz phase-locked loop
- LCD driver
- 6-bit analog-to-digital converter
- Two 8-bit PWM digital-to-analog converters
- Two 4-bit input/output ports
- Two 4-bit input ports
- One 4-bit output port
- 8-bit keypad matrix scan output
- 4-bit open-drain, high-voltage output
- 28 mask-selectable output drivers
- 20-bit universal counter
- 4096 × 16-bit program ROM (000H to FFEH user-addressable memory)
- 256 × 4-bit data RAM
- Low-voltage detection reset circuit
- Programmable high-speed divider
- Single-word instructions
- Four-level stack
- PLL-unlocked flip-flop
- Timer flip-flop
- External interrupt
- Programmable watchdog interrupt address
- Standby mode
- CPU operates down to 3.5 V, with data retention down to 1.3 V
- Single 5 V supply
- 80-pin QIP

Specifications and information herein are subject to change without notice.

SANYO Electric Co., Ltd. Semiconductor Division
Natsume Bldg., 18-6, 2-chome, Yushima, Bunkyo-ku, TOKYO 113 JAPAN

LC7232

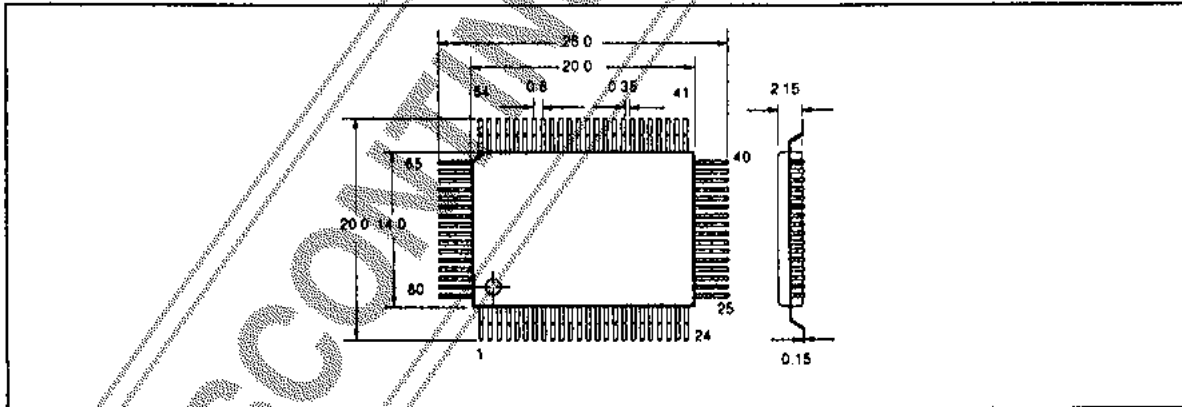
PINOUT



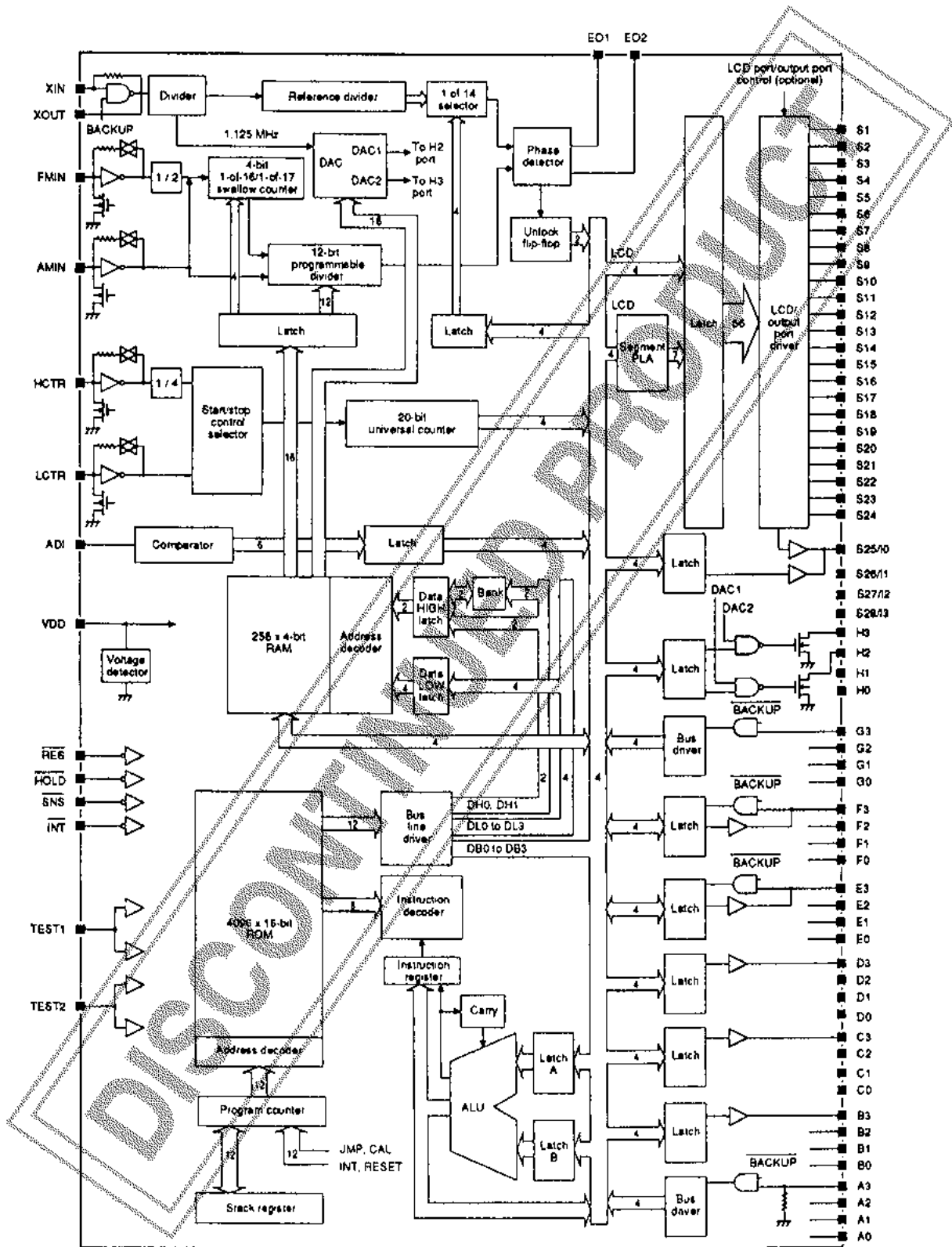
PACKAGE DIMENSIONS

Unit: mm

3044B-QIP80A



BLOCK DIAGRAM

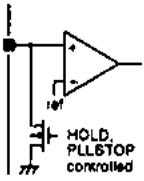
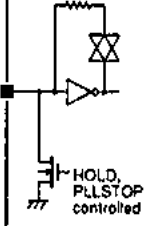
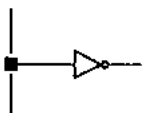
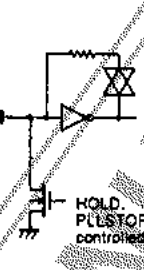



PIN DESCRIPTION

Number	Name	Equivalent Circuit	Description
1	XIN		Crystal oscillator connections
80	XOUT		
2	TEST2		Test pins
79	TEST1		
3 to 6	PG3 to PG0		Input port G
7 to 10	PH3 to PH0		Output port H
11 to 14	PF3 to PF0		Input/output port F
15 to 18	PE3 to PE0		Input/output port E
19 to 22	PD3 to PD0		Output port D
23 to 26	PC3 to PC0		Output port C
27 to 30	PB3 to PB0		Output port B
31, 73	VDD		5 V supply

LC7232

Number	Name	Equivalent Circuit	Description
32 to 35	PA3 to PA0		Input port A
36 to 39	PI3/S28 to PI0/S25		Input port I
40 to 63	S24 to S1		LCD segment outputs
64, 65	COM2, COM1		LCD common driver outputs
66	$\overline{\text{INT}}$		Interrupt request input
67	$\overline{\text{HOLD}}$		Hold-mode control input
68	$\overline{\text{RES}}$		Device reset input

Number	Name	Equivalent Circuit	Description
69	ADI		A/D converter input
70	HCTR		Universal counter input 1
71	LCTR		Universal counter input 2
72	$\overline{\text{SNS}}$		Power-fail detect
74	FMIN		FM VCO input
75	AMIN		AM VCO input
76	VSS		Ground
77, 78	E01 and E02		Phase comparator outputs

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	$V_{DD \text{ max}}$	-0.3 to 6.5	V
Port G, HOLD, ADI, INT, RES and SNS input voltage range	V_{IN1}	-0.3 to 13	V
Input voltage range (other inputs)	V_{IN2}	-0.3 to $V_{DD} + 0.3$	V
Port H output voltage range	V_{OUT1}	-0.3 to 15	V
Output voltage range (all other outputs)	V_{OUT2}	-0.3 to $V_{DD} + 0.3$	V
Ports D and H output current range	I_{OUT1}	0 to 5	mA

Parameter	Symbol	Rating	Unit
Ports E, F and I output current range	I_{OUT2}	0 to 3	mA
Ports B and C output current range per pin	I_{OUT3}	0 to 1	mA
Power dissipation	P_D	400	mW
Operating temperature range	T_{OP0}	-40 to 85	deg. C
Storage temperature range	T_{STG}	-45 to 125	deg. C

Recommended Operating Conditions

$T_a = 25$ deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range (PLL and CPU)	V_{DD1}	4.5 to 5.5	V
Supply voltage range (CPU)	V_{DD2}	3.5 to 5.5	V
Supply voltage range for data retention	V_{DD3}	1.3 to 5.5	V

Electrical Characteristics

$T_a = -40$ to 85 deg. C, $V_{DD} = 3.5$ to 5.5 V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Port G HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	-	8.0	V
RES, INT and HOLD HIGH-level input voltage	V_{IH2}		$0.8V_{DD}$	-	8.0	V
SNS HIGH-level input voltage	V_{IH3}		2.5	-	8.0	V
Port A HIGH-level input voltage	V_{IH4}		$0.6V_{DD}$	-	V_{DD}	V
Ports E and F HIGH-level input voltage	V_{IH5}		$0.7V_{DD}$	-	V_{DD}	V
LCTR HIGH-level input voltage	V_{IH6}	$V_{DD} = 4.5$ to 5.5 V	$0.8V_{DD}$	-	V_{DD}	V
Port G LOW-level input voltage	V_{IL1}		0	-	$0.3V_{DD}$	V
RES and INT LOW-level input voltage	V_{IL2}		0	-	$0.2V_{DD}$	V
SNS LOW-level input voltage	V_{IL3}		0	-	1.3	V
Port A LOW-level input voltage	V_{IL4}		0	-	$0.2V_{DD}$	V
Ports E and F LOW-level input voltage	V_{IL5}		0	-	$0.3V_{DD}$	V
LCTR LOW-level input voltage	V_{IL6}	$V_{DD} = 4.5$ to 5.5 V	0	-	$0.2V_{DD}$	V
HOLD LOW-level input voltage	V_{IL7}		0	-	$0.4V_{DD}$	V
XIN input frequency	f_{IN1}	$V_{IN} = 0.5$ to 1.5 V	4.0	4.5	5.0	MHz
FMIN input frequency	f_{IN2}	$V_{IN} = 0.1$ to 1.5 V, $V_{DD} = 4.5$ to 5.5 V	10	-	130	MHz
		$V_{IN} = 0.15$ to 1.5 V, $V_{DD} = 4.5$ to 5.5 V	10	-	150	
AMIN input frequency (low range)	f_{IN3}	$V_{IN} = 0.1$ to 1.5 V, $V_{DD} = 4.5$ to 5.5 V	0.5	-	10	MHz

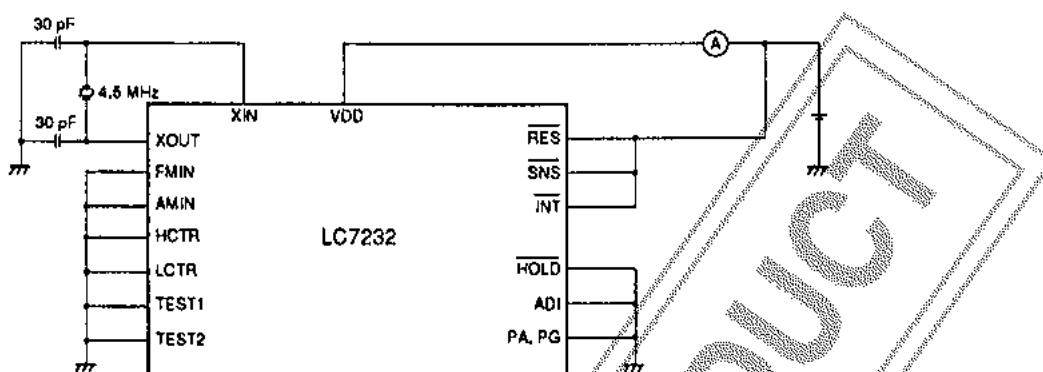
LC7232

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
AMIN input frequency (high range)	f_{IN4}	$V_{IN} = 0.1$ to 1.5 V, $V_{DD} = 4.5$ to 5.5 V	2.0	-	40	MHz
HCTR input frequency	f_{IN6}	$V_{IN} = 0.1$ to 1.5 V, $V_{DD} = 4.5$ to 5.5 V	0.4	-	12	MHz
LCTR input frequency	f_{IN7}	$V_{IN} = 0.1$ to 1.5 V, $V_{DD} = 4.5$ to 5.5 V	100	-	500	kHz
		$V_{IL} = 0$ V to $0.2V_{DD}$, $V_{IH} = 0.8V_{DD}$ to V_{DD}	0.001	-	20	
XIN rms input amplitude	V_{IN1}		0.5	-	1.5	V
FMIN rms input amplitude	V_{IN2}		0.1	-	1.5	V
AMIN rms input amplitude	V_{IN3}		0.1	-	1.5	V
LCTR and HCTR rms input amplitude	V_{IN4}		0.1	-	1.5	V
ADI input voltage range	V_{IN5}		0	-	V_{DD}	V
LCTR, \overline{RES} and \overline{INT} input hysteresis width	V_{HYS}		$0.1V_{DD}$	-	-	V
SNS reject pulsewidth	P_{rej}		-	-	50	μ s
Standby threshold voltage	V_{DET}		2.7	3.0	3.3	V
\overline{INT} , \overline{RES} , \overline{HOLD} , ADI, SNS and port G HIGH-level input current	I_{IH1}	$V_{IN} = 5.5$ V	-	-	3.0	μ A
Ports A, E and F HIGH-level input current	I_{IH2}	Ports E and F are high impedance, port A has no R_{PD} , $V_{IN} = V_{DD}$	-	-	3.0	μ A
XIN HIGH-level input current	I_{IH3}	$V_{IN} = V_{DD} = 5.0$ V	2	5	15	μ A
LCTR, FMIN, AMIN and HCTR HIGH-level input current	I_{IH4}	$V_{IN} = V_{DD} = 5.0$ V	4	10	30	μ A
Port A HIGH-level input current	I_{IH5}	$V_{IN} = V_{DD} = 5.0$ V, port A has R_P	-	50	-	μ A
\overline{INT} , \overline{RES} , \overline{HOLD} , ADI, SNS and port G LOW-level input current	I_{IL1}	$V_{IN} = V_{SS}$	-	-	3.0	μ A
Ports A, E and F LOW-level input current	I_{IL2}	Ports E and F are high impedance, port A has no R_{PD} , $V_{IN} = V_{SS}$	-	-	3.0	μ A
XIN LOW-level input current	I_{IL3}	$V_{IN} = V_{SS}$	2	5	15	μ A
LCTR, FMIN, AMIN and HCTR LOW-level input current	I_{IL4}	$V_{IN} = V_{SS}$	4	10	30	μ A
Port A input voltage	V_{IF}	Port A is high impedance.	-	-	$0.05V_{DD}$	V
Port A pull-down resistance	R_{PD}	$V_{DD} = 5$ V	75	100	200	k Ω
EO1 and EO2 output leakage current	I_{OFFH1}	$V_O = V_{DD}$	-	0.01	10.0	nA
Ports B, C, E, F and Y output leakage current	I_{OFFH2}	$V_O = V_{DD}$	-	-	3.0	μ A
Port H output leakage current	I_{OFFH3}	$V_O = 13$ V	-	-	5.0	μ A
EO1 and EO2 output leakage current	I_{OFFL1}	$V_O = V_{SS}$	-	0.01	10.0	nA

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Ports B, C, E, F and I output leakage current	I_{OFFL2}	$V_0 = V_{SS}$	-	-	3.0	μA
Ports B and C HIGH-level output voltage	V_{OH1}	$I_0 = 1 \text{ mA}$	$V_{DD} - 2.0$	$V_{DD} - 1.0$	$V_{DD} - 0.5$	V
Ports E, F and I HIGH-level output voltage	V_{OH2}	$I_0 = 1 \text{ mA}$	$V_{DD} - 1.0$	-	-	V
E01 and E02 HIGH-level output voltage	V_{OH3}	$I_0 = 500 \mu A$	$V_{DD} - 1.0$	-	-	V
XOUT HIGH-level output voltage	V_{OH4}	$I_0 = 200 \mu A$	$V_{DD} - 1.0$	-	-	V
S1 to S28 HIGH-level output voltage	V_{OH5}	$I_0 = -0.1 \text{ mA}$	$V_{DD} - 1.0$	-	-	V
Port D HIGH-level output voltage	V_{OH6}	$I_0 = 5 \text{ mA}$	$V_{DD} - 1.0$	-	-	V
COM1 and COM2 HIGH-level output voltage	V_{OH7}	$I_0 = 25 \mu A$	$V_{DD} - 0.75$	-	-	V
Ports B and C LOW-level output voltage	V_{OL1}	$I_0 = 50 \mu A$	0.5	1.0	2.0	V
Ports E, F and I LOW-level output voltage	V_{OL2}	$I_0 = 1 \text{ mA}$	-	-	1.0	V
E01 and E02 LOW-level output voltage	V_{OL3}	$I_0 = 500 \mu A$	-	-	1.0	V
XOUT LOW-level output voltage	V_{OL4}	$I_0 = 200 \mu A$	-	-	1.0	V
S1 to S28 LOW-level output voltage	V_{OL5}	$I_0 = 0.1 \text{ mA}$	-	-	1.0	V
Port D LOW-level output voltage	V_{OL6}	$I_0 = 5 \text{ mA}$	-	-	1.0	V
COM1 and COM2 LOW-level output voltage	V_{OL7}	$I_0 = 25 \mu A$	0.3	0.5	0.75	V
Port H LOW-level output voltage	V_{OL8}	$I_0 = 5 \text{ mA}$	0.75	-	2.0	V
COM1 and COM2 mid-level output voltage	V_{M1}	$V_{DD} = 5 \text{ V}, I_0 = 20 \mu A$	2.0	2.5	3.0	V
A/D converter error	ϵ	$V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	$-\frac{1}{2}$	-	$\frac{1}{2}$	lsb
Supply current	I_{DD1}	$f_n = 130 \text{ MHz}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$	-	15	20	mA
Hold-mode supply current	I_{DD2}	PLL halted, $t_{cyc} = 2.67 \mu s$	-	1.5	-	mA
		PLL halted, $t_{cyc} = 13.33 \mu s, V_{DD} = 3.5 \text{ to } 5.5 \text{ V}$	-	1.0	-	
		PLL halted, $t_{cyc} = 40.00 \mu s, V_{DD} = 3.5 \text{ to } 5.5 \text{ V}$	-	0.7	-	
Standby mode supply current	I_{DD3}	$V_{DD} = 5.5 \text{ V}, \text{ oscillator halted}, T_a = 25 \text{ deg. C}$	-	-	5	μA
		$V_{DD} = 2.5 \text{ V}, \text{ oscillator halted}, T_a = 25 \text{ deg. C}$	-	-	1	

Measurement Circuits

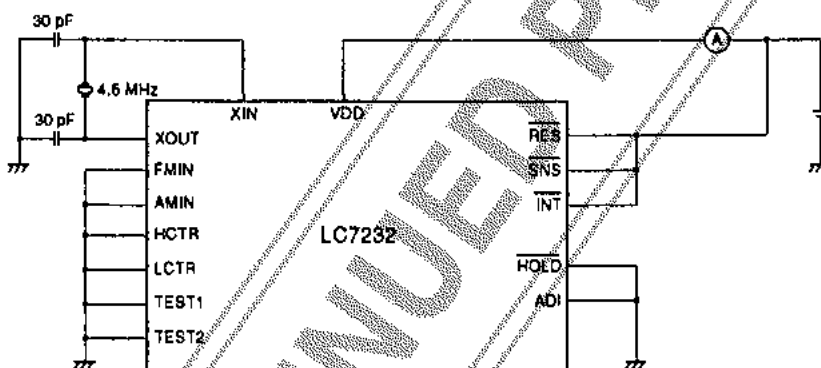
Hold mode



Notes

1. Ports E and F are selected as output ports.
2. Ports B to H are open.

Standby mode



Note

Ports A to I, S1 to S24, COM1 and COM2 are open.

FUNCTIONAL DESCRIPTION

LCD Driver

The LC7232 can drive LCD segments. The LCP and LCD instructions transfer data to the LCD outputs. The LCD instruction transfers data directly to the LCD outputs whereas the LCP instruction converts data to 7-segment format before transfer to the outputs.

S1 to S28 are the driver outputs. The LCD frame rate is 100 Hz with a 50% duty cycle. After reset or power-up, a blank signal is present on all outputs. In standby mode, all outputs are LOW. They can be used as general-purpose outputs if the appropriate mask option is selected.

COM1 and COM2 are the LCD common driver outputs. Output drive is 50% duty with 50% bias. Upon reset or after power-up, the normal drive signals are present on these outputs. In standby mode, all outputs are LOW.

Frequency and Period Measurement

AM IF frequencies are measured at HCTR and LCTR by the 20-bit universal counter using an input frequency range of 0.4 to 12 MHz. FM IF frequencies are measured at HCTR only. Capacitive coupling should be used at HCTR for all input frequencies, and at LCTR, for input frequencies in the range 100 to 500 KHz.

Period measurement is performed at LCTR by the 20-bit universal counter using an input frequency range of 1 Hz to 20 KHz. Capacitive coupling is not required.

Phase-locked Loop

The FMIN or AMIN input signal is divided down by a programmable divider, and then compared with the crystal frequency, which is also divided down using 14 selectable ratios. The phase difference between the two signals is measured using a phase detector and output on EO1 and EO2.

FMIN is the input pin for the FM VCO input signal. The input frequency range is 10 to 130 MHz. Capacitive coupling should be used.

AMIN is the AM VCO input. The bandwidth is adjustable in two ranges by using the PLL instruction—HIGH (2 to 40 MHz) for the SW band, and LOW (0.5 to 10 MHz), for the LW and MW bands. Capacitive coupling should be used.

Input/Output Ports

Port A

This input port has a low switching threshold, which is used for keypad matrix inputs. Pull-down resistors for all pins are available as a mask option. Note that either all or none of the pins should have pull-down resistors. In standby mode, inputs are ignored.

Ports B and C

These output ports have unbalanced CMOS outputs which are used as keypad matrix scan outputs. Upon reset, outputs are set LOW, and in standby mode, outputs are high impedance. The outputs can be short-circuited.

Port D

Port D is an output port only. Upon reset, outputs are LOW, and in standby mode, outputs are high impedance.

Port E

The transfer direction of this input/output port is selected automatically under software control. When an input instruction (IN, IPT, or TPE) is executed, port E is configured for input operation, and an output instruction (OUT, SPB or RPB), for output operation. Upon reset, all pins become inputs. In standby mode, the output drivers are high impedance and the input signals are ignored. All bits should either be inputs or outputs.

Port F

The transfer direction of this input/output port is selected by the FPC instruction. Each pin of this port can be set independently to be an input or output. Upon reset, all pins become inputs. In standby mode, the output drivers are high impedance and the input signals are ignored.

Port G

This is an input port only. In standby mode, inputs are ignored.

Port H

These output ports are high-voltage, n-channel open-drain drivers, which are used for switching power supplies. Upon reset and in standby mode, outputs are high impedance.

Port I

Port I is a 4-bit general purpose output port. The outputs PI0 to PI3 are multiplexed with four of the LCD driver outputs, S25 to S28. The bits can be configured as either standard outputs or LCD driver outputs by using the SS and RS instructions. Upon power-on or after reset, they are configured as LCD drivers and output a blank display signal. In standby mode these pins are LOW.

A/D Converter

The A/D converter is a 6-bit successive approximation type. The conversion cycle time is 1.28 ms. Full-scale output data is 3FH for an input of $V_{DD} \times (63/96)$.

PWM Outputs

Bits 2 and 3 of port H are the outputs of DAC1 and DAC2, respectively. The outputs are pulsewidth modulation (PWM) encoded, with the width of the output pulse determined by the value loaded into the 8-bit register for the corresponding DAC. The output frequency is 4394.5 Hz for a cycle time of 2.67 μ s.

Power-fail Detection

When connected to the supply, \overline{SNS} is used as a power-fail detector. \overline{SNS} can also be used as a standard input port.

Interrupt Request

This input generates a device interrupt when a HIGH-to-LOW transition occurs. The corresponding INTEN flag should be set by the SS instruction before an interrupt can be generated.

Reset

This input can be used to re-initialize the LC7232. Upon power-up, this pin should be held LOW for at least 75 ms after the supply stabilizes. Thereafter, it should be held LOW for at least six clock cycles to reset the device.

Crystal Oscillator

The master crystal oscillator, which has a feedback resistor on-chip, requires only the connection of a 4.5 MHz crystal.

Low-power Modes

Hold mode

When the hold mode control pin, \overline{HOLD} , is driven LOW and the HOLDEN (hold enable) flip-flop has previously been set by an SS instruction, the LC7232 enters hold mode.

\overline{HOLD} has a high-voltage input ($V_{IH(max)} = 8.0$ V) which can be connected directly to the power supply.

Standby mode

When the LC7232 is in hold mode and \overline{HOLD} is LOW, standby mode can be set by the CKSTP instruction.

Test Pins

Two device test pins are provided—TEST1 and TEST2. These should either be tied to V_{SS} or left open.

INSTRUCTION SET

ADDR	Program memory address [12 bits]
b	Borrow
B	Bank number [2 bits]
C	Carry
DH	Data memory address high-order bits (row address) [2 bits]
DL	Data memory address low-order bits (column address) [4 bits]
I	Immediate data [4 bits]
M	Data memory address
N	Bit position [4 bits]
Pn	Port number [4 bits]
r	General register (Bank 00H to 0FH)
Rn	Register number [4 bits]
()	Contents of register or memory
()n	Contents of bit N of register or memory

DISCONTINUED PRODUCT

Mnemonic	Operands		Operation	Instruction Format																Relation	Description	Stack condition									
	1st	2nd		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0												
IN	M	Ph	Move port data to M	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$M \leftarrow \text{port}(Ph)$	Moves the data from input port Ph to M.			
OUT	M	Ph	Move data to port	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{port}(Ph) \leftarrow M$	Moves the contents of memory location M to port Ph			
SPB	Ph	N	Set port bits	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{port}(Ph) \leftarrow N$	Sets the bits of port Ph, indicated by N to logic 1			
RPB	Ph	N	Reset port bits	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{port}(Ph) \leftarrow 0$	Sets the bits of port Ph, indicated by N to logic 0			
TPT	Ph	N	Test bits of port and stop if true	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{Stop if } \text{port}(Ph) \text{ and } N = \text{all } 1$	Tests the bits of port Ph, specified by N. Stops if all bits are logic 1.	All bits specified = 1		
TPF	Ph	N	Test bits of port and stop if false	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{Stop if } \text{port}(Ph) \text{ and } N = \text{all } 0$	Tests the bits of port Ph, specified by N. Stops if all bits are logic 0.	All bits specified = 0		
Universal counter instructions																															
UCS	I		Set UCCW1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{UCCW1} \leftarrow 1$	Sets the universal counter flag 1.		
UCC	I		Set UCCW2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{UCCW2} \leftarrow 1$	Sets the universal counter flag 2.		
Miscellaneous instructions																															
FPC	N		Port F direction control	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{FPC latch} \leftarrow N$	Defines the direction of individual pins of port F. If a bit in the port F direction register is set by FPC, the corresponding pin of port F becomes an output.		
CKSTP			Stop clock	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{Stop clock if } \text{HOLD} = 0$	Stops the processor clock if $\text{HOLD} = 0$.		
DAC	I		Move data to DAC registers	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	$\text{DAC} \leftarrow I$	Loads the immediate data to the DAC registers.		
NOP			No operation	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	No operation	No operation		

MASK OPTIONS

Parameter	Options
Watchdog timer (WDT)	Yes
	No
Pull-down resistors on port A (the keypad matrix input port)	Yes
	No
Instruction cycle time	2.67 μ s
	13.33 μ s
	40.00 μ s
S1 to S23 configuration	LCD driver output port
	General-purpose output port

DEVELOPMENT SYSTEM

The LC7232 development environment is shown in figure 1. It uses an LC72EV32 evaluation chip mounted on a TB-72EV32 target board and a multifunctional emulator (RE32), which is controlled by a personal computer, to provide full debugging facilities.

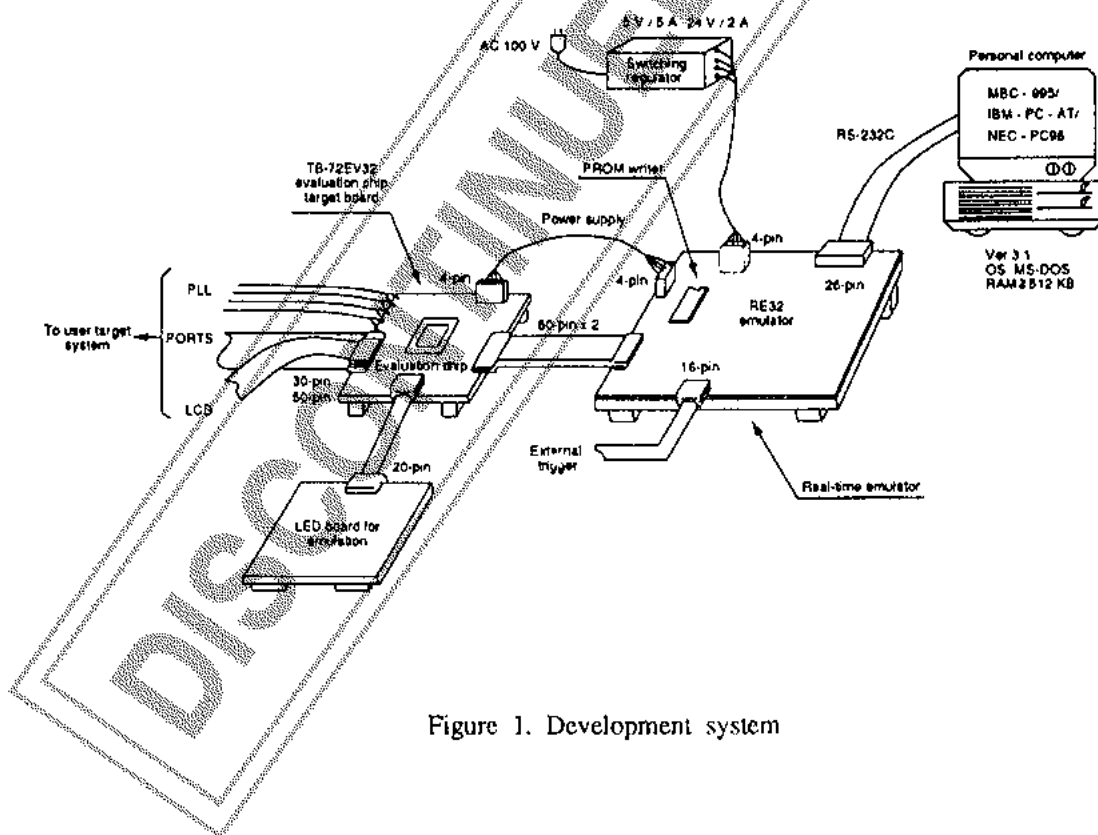


Figure 1. Development system

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