



# Single Channel, 12-/16-Bit, Serial Input, Current Source and Voltage Output DACs

## AD5412/AD5422

### FEATURES

**12-/16-bit resolution and monotonicity**

**Current output ranges: 4 mA to 20 mA, 0 mA to 20 mA,**

**0 mA to 24 mA**

**±0.01 % FSR typical total unadjusted error (TUE)**

**±3 ppm/°C output drift**

**Voltage output ranges: 0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V**

**10% overrange**

**±0.01 % FSR typical total unadjusted error (TUE)**

**±2 ppm/°C output drift**

**Flexible serial digital interface**

**On-chip output fault detection**

**On-chip reference: 10 ppm/°C maximum**

**Asynchronous clear function**

**Power supply range**

**AV<sub>DD</sub>: 10.8 V to 40 V**

**AV<sub>SS</sub>: -26.4 V to -3 V/0 V**

**Output loop compliance: AV<sub>DD</sub> - 2.5 V**

**Temperature range: -40°C to +85°C**

**TSSOP and LFCSP packages**

### APPLICATIONS

**Process control**

**Actuator control**

**PLC**

### GENERAL DESCRIPTION

The AD5412/AD5422 are low-cost, precision, fully integrated 12-/16-bit digital-to-analog converters (DAC) offering a programmable current source and programmable voltage output designed to meet the requirements of industrial process control applications.

The output current range is programmable at 4 mA to 20 mA, 0 mA to 20 mA, or an overrange function of 0 mA to 24 mA.

Voltage output is provided from a separate pin that can be configured to provide 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V output ranges; an overrange of 10% is available on all ranges.

Analog outputs are short and open-circuit protected and can drive capacitive loads of 1 μF.

The device operates with an AV<sub>DD</sub> power supply range from 10.8 V to 40 V. Output loop compliance is 0 V to AV<sub>DD</sub> - 2.5 V.

The flexible serial interface is SPI- and MICROWIRE™-compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on-reset function, ensuring that the device powers up in a known state. The part also includes an asynchronous clear pin (CLEAR) that sets the outputs to zero-scale/midscale voltage output or the low end of the selected current range.

The total output error is typically ±0.01% in current mode and ±0.01% in voltage mode.

**Table 1. Pin-Compatible Devices**

| Part Number | Description   |
|-------------|---|
| AD5410      | Single channel, 12-bit, serial input current source DAC |
| AD5420      | Single channel, 16-bit, serial input current source DAC |

Rev. C

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## TABLE OF CONTENTS

|  |    |   |    |
|--|----|---|----|
| Features .....                                     | 1  | AD5412/AD5422 Features .....                                | 31 |
| Applications .....                                 | 1  | Fault Alert .....   | 31 |
| General Description .....                          | 1  | Voltage Output Short Circuit Protection .....               | 31 |
| Revision History .....                             | 2  | Voltage Output Overrange .....                              | 31 |
| Functional Block Diagram .....                     | 3  | Voltage Output Force-Sense .....                            | 31 |
| Specifications .....                               | 4  | Asynchronous Clear (CLEAR) .....                            | 31 |
| AC Performance Characteristics .....               | 7  | Internal Reference .....                                    | 31 |
| Timing Characteristics .....                       | 8  | External Current Setting Resistor .....                     | 31 |
| Absolute Maximum Ratings .....                     | 10 | Digital Power Supply .....                                  | 32 |
| ESD Caution .....                                  | 10 | External Boost Function .....                               | 32 |
| Pin Configurations and Function Descriptions ..... | 11 | External Compensation Capacitor .....                       | 32 |
| Typical Performance Characteristics .....          | 13 | Digital Slew Rate Control .....                             | 32 |
| General .....                                      | 13 | I <sub>OUT</sub> Filtering Capacitors (LFCSP Package) ..... | 33 |
| Voltage Output .....                               | 15 | Applications Information .....                              | 35 |
| Current Output .....                               | 20 | Driving Inductive Loads .....                               | 35 |
| Terminology .....                                  | 24 | Transient Voltage Protection .....                          | 35 |
| Theory of Operation .....                          | 26 | Galvanically Isolated Interface .....                       | 35 |
| Architecture .....                                 | 26 | Microprocessor Interfacing .....                            | 35 |
| Serial Interface .....                             | 27 | Layout Guidelines .....                                     | 35 |
| Power-On State .....                               | 28 | Thermal and Supply Considerations .....                     | 36 |
| Data Register .....                                | 29 | Industrial Analog Output Module .....                       | 37 |
| Control Register .....                             | 29 | Outline Dimensions .....                                    | 38 |
| Reset Register .....                               | 30 | Ordering Guide .....  | 39 |
| Status Register .....                              | 30 |   |    |

## REVISION HISTORY

### 3/10—Rev. B to Rev. C

|   |    |
|---|----|
| Changes to AVSS to GND Parameter in Table 5 ..... | 10 |
|---|----|

### 2/10—Rev. A to Rev. B

|   |    |
|---|----|
| Changes to Thermal and Supply Considerations Section and Table 25 ..... | 36 |
|---|----|

### 8/09—Rev. 0 to Rev. A

|   |    |
|---|----|
| Changes to Table 2 .....                                | 4  |
| Changes to Table 3 .....                                | 7  |
| Changes to Introduction to Table 4 .....                | 8  |
| Changes to Introduction to Table 5 and to Table 5 ..... | 10 |

### Changes to Pin Configurations and Function Descriptions

|  |    |
|--|----|
| Section, Added Figure 6, Renumbered Subsequent Figures .....   | 11 |
| Changes to Theory of Operation Section .....   | 26 |
| Changes to Architecture Section .....  | 26 |
| Changes to AD5412/AD5422 Features Section .....  | 31 |
| Added IOUT Filtering Capacitors (LFCSP Package) Section, Including Figure 69 to Figure 72 and Table 24 ..... | 33 |
| Changes to Thermal and Supply Considerations Section .....   | 36 |
| Updated Outline Dimensions .....   | 38 |
| Changes to Ordering Guide .....  | 39 |

### 5/09—Revision 0: Initial Version

## FUNCTIONAL BLOCK DIAGRAM

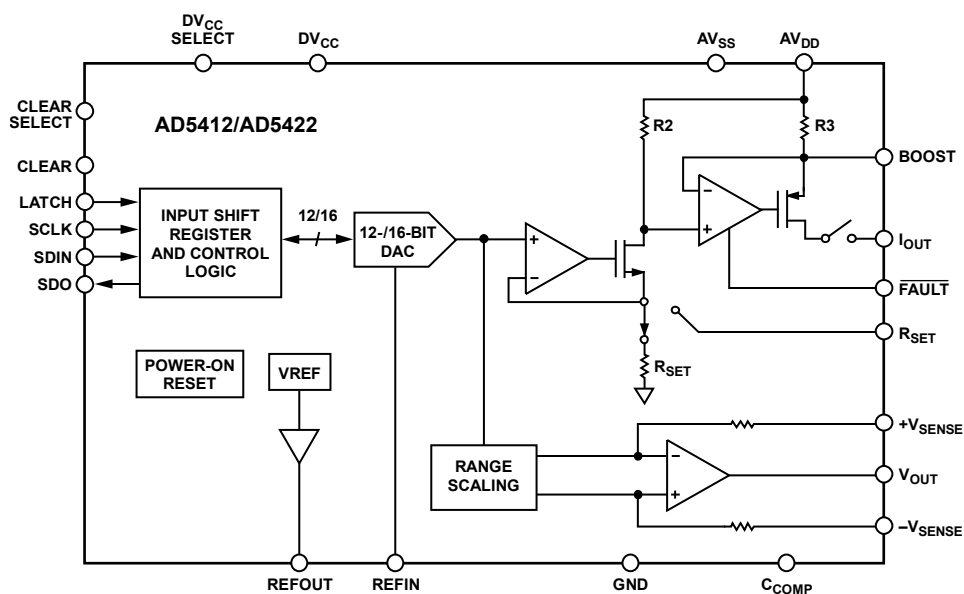


Figure 1.

# AD5412/AD5422

## SPECIFICATIONS

$AV_{DD} = 10.8\text{ V to }26.4\text{ V}$ ,  $AV_{SS} = -26.4\text{ V to }-3\text{ V/0 V}$ ,  $AV_{DD} + |AV_{SS}| < 52.8\text{ V}$ ,  $GND = 0\text{ V}$ ,  $REFIN = 5\text{ V external}$ ;  $DV_{CC} = 2.7\text{ V to }5.5\text{ V}$ .  
 $V_{OUT}$ :  $R_{LOAD} = 1\text{ k}\Omega$ ,  $C_L = 200\text{ pF}$ ,  $I_{OUT}$ :  $R_{LOAD} = 350\text{ }\Omega$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

| Parameter <sup>1</sup>                                       | Min    | Typ         | Max    | Unit                      | Test Conditions/Comments                          |
|--|--------|-------------|--------|---------------------------|---|
| <b>VOLTAGE OUTPUT</b>  |        |             |        |                           |   |
| Output Voltage Ranges  | 0      |             | 5      | V                         |   |
|  | 0      |             | 10     | V                         |   |
|  | -5     |             | +5     | V                         |   |
|  | -10    |             | +10    | V                         |   |
| Accuracy   |        |             |        |                           | Output unloaded                                   |
| Resolution   | 16     |             |        | Bits                      | AD5422  |
|  | 12     |             |        | Bits                      | AD5412  |
| Total Unadjusted Error (TUE)                                 |        |             |        |                           |   |
| B Version  | -0.1   |             | +0.1   | % FSR                     |   |
|  | -0.05  | $\pm 0.01$  | +0.05  | % FSR                     | $T_A = 25^\circ\text{C}$                          |
| A Version  | -0.3   |             | +0.3   | % FSR                     |   |
|  | -0.1   | $\pm 0.05$  | +0.1   | % FSR                     | $T_A = 25^\circ\text{C}$                          |
| Relative Accuracy (INL) <sup>2</sup>                         | -0.008 |             | +0.008 | % FSR                     | AD5422  |
|  | -0.032 |             | +0.032 | % FSR                     | AD5412  |
| Differential Nonlinearity (DNL)                              | -1     |             | +1     | LSB                       | Guaranteed monotonic                              |
| Bipolar Zero Error   | -6     |             | +6     | mV                        | Bipolar output range                              |
|  | -1.5   | $\pm 0.2$   | +1.5   | mV                        | $T_A = 25^\circ\text{C}$ , bipolar output range   |
| Bipolar Zero Error Temperature Coefficient (TC) <sup>3</sup> |        | $\pm 3$     |        | ppm FSR/ $^\circ\text{C}$ | Bipolar output range                              |
| Zero-Scale Error   | -5     |             | +5     | mV                        |   |
|  | -3.5   | $\pm 0.3$   | +3.5   | mV                        | $T_A = 25^\circ\text{C}$                          |
| Zero-Scale Error Temperature Coefficient (TC) <sup>3</sup>   |        | $\pm 2$     |        | ppm FSR/ $^\circ\text{C}$ |   |
| Offset Error   | -4     |             | +4     | mV                        | Unipolar output range                             |
|  | -1.5   | $\pm 0.2$   | +1.5   | mV                        | $T_A = 25^\circ\text{C}$ , unipolar output range  |
| Offset Error Temperature Coefficient (TC) <sup>3</sup>       |        | $\pm 2$     |        | ppm FSR/ $^\circ\text{C}$ | Unipolar output range                             |
| Gain Error   | -0.07  |             | +0.07  | % FSR                     |   |
|  | -0.05  | $\pm 0.004$ | +0.05  | % FSR                     | $T_A = 25^\circ\text{C}$                          |
| Gain Error Temperature Coefficient (TC) <sup>3</sup>         |        | $\pm 1$     |        | ppm FSR/ $^\circ\text{C}$ |   |
| Full-Scale Error   | -0.07  |             | +0.07  | % FSR                     |   |
|  | -0.05  | $\pm 0.001$ | +0.05  | % FSR                     | $T_A = 25^\circ\text{C}$                          |
| Full-Scale Error Temperature Coefficient (TC) <sup>3</sup>   |        | $\pm 1$     |        | ppm FSR/ $^\circ\text{C}$ |   |
| <b>OUTPUT CHARACTERISTICS<sup>3</sup></b>                    |        |             |        |                           |   |
| Headroom   |        | 0.5         | 0.8    | V                         | Output unloaded                                   |
| Output Voltage Drift vs. Time                                |        | 90          |        | ppm FSR                   | Drift after 1000 hours, $T_A = 125^\circ\text{C}$ |
| Short-Circuit Current  |        | 20          |        | mA                        |   |
| Load   | 1      |             |        | k $\Omega$                |   |
| Capacitive Load Stability                                    |        |             |        |                           | $T_A = 25^\circ\text{C}$                          |
| $R_{LOAD} = \infty$  |        |             | 20     | nF                        |   |
| $R_{LOAD} = 1\text{ k}\Omega$                                |        |             | 5      | nF                        |   |
| $R_{LOAD} = \infty$  |        |             | 1      | $\mu\text{F}$             | External compensation capacitor of 4 nF connected |
| DC Output Impedance  |        | 0.3         |        | $\Omega$                  |   |
| Power-On Time  |        | 10          |        | $\mu\text{s}$             |   |

| Parameter <sup>1</sup>                                 | Min    | Typ         | Max    | Unit                         | Test Conditions/Comments         |
|--|--------|-------------|--------|------------------------------|----------------------------------|
| DC PSRR  |        | 90          | 130    | $\mu\text{V/V}$              |                                  |
|  |        | 3           | 12     | $\mu\text{V/V}$              | Output unloaded                  |
| <b>CURRENT OUTPUT</b>                                  |        |             |        |                              |                                  |
| Output Current Ranges                                  | 0      |             | 24     | mA                           |                                  |
|  | 0      |             | 20     | mA                           |                                  |
|  | 4      |             | 20     | mA                           |                                  |
| Accuracy (Internal $R_{\text{SET}}$ )                  |        |             |        |                              |                                  |
| Resolution   | 16     |             |        | Bits                         | AD5422                           |
|  | 12     |             |        | Bits                         | AD5412                           |
| Total Unadjusted Error (TUE)                           |        |             |        |                              |                                  |
| B Version  | -0.3   |             | +0.3   | % FSR                        |                                  |
|  | -0.13  | $\pm 0.08$  | +0.13  | % FSR                        | $T_A = 25^\circ\text{C}$         |
| A Version  | -0.5   |             | +0.5   | % FSR                        |                                  |
|  | -0.3   | $\pm 0.15$  | +0.3   | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Relative Accuracy (INL) <sup>4</sup>                   | -0.024 |             | +0.024 | % FSR                        | AD5422                           |
|  | -0.032 |             | +0.032 | % FSR                        | AD5412                           |
| Differential Nonlinearity (DNL)                        | -1     |             | +1     | LSB                          | Guaranteed monotonic             |
| Offset Error   | -0.27  |             | +0.27  | % FSR                        |                                  |
|  | -0.12  | $\pm 0.08$  | +0.12  | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Offset Error Temperature Coefficient (TC) <sup>3</sup> |        | $\pm 16$    |        | ppm FSR/ $^\circ\text{C}$    |                                  |
| Gain Error   | -0.18  |             | +0.18  | % FSR                        | AD5422                           |
|  | -0.03  | $\pm 0.006$ | +0.03  | % FSR                        | AD5422, $T_A = 25^\circ\text{C}$ |
|  | -0.22  |             | +0.22  | % FSR                        | AD5412                           |
|  | -0.06  | $\pm 0.006$ | +0.06  | % FSR                        | AD5412, $T_A = 25^\circ\text{C}$ |
| Gain Temperature Coefficient (TC) <sup>3</sup>         |        | $\pm 10$    |        | ppm FSR/ $^\circ\text{C}$    |                                  |
| Full-Scale Error                                       | -0.2   |             | +0.2   | % FSR                        |                                  |
|  | -0.1   | $\pm 0.08$  | +0.1   | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Full-Scale Temperature Coefficient (TC) <sup>3</sup>   |        | $\pm 6$     |        | ppm FSR/ $^\circ\text{C}$    |                                  |
| Accuracy (External $R_{\text{SET}}$ )                  |        |             |        |                              |                                  |
| Resolution   | 16     |             |        | Bits                         | AD5422                           |
|  | 12     |             |        | Bits                         | AD5412                           |
| Total Unadjusted Error (TUE)                           |        |             |        |                              |                                  |
| B Version  | -0.15  |             | +0.15  | % FSR                        |                                  |
|  | -0.06  | $\pm 0.01$  | +0.06  | % FSR                        | $T_A = 25^\circ\text{C}$         |
| A Version  | -0.3   |             | +0.3   | % FSR                        |                                  |
|  | -0.1   | $\pm 0.02$  | +0.1   | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Relative Accuracy (INL) <sup>4</sup>                   | -0.012 |             | +0.012 | % FSR                        | AD5422                           |
|  | -0.032 |             | +0.032 | % FSR                        | AD5412                           |
| Differential Nonlinearity (DNL)                        | -1     |             | +1     | LSB                          | Guaranteed monotonic             |
| Offset Error   | -0.1   |             | +0.1   | % FSR                        |                                  |
|  | -0.03  | $\pm 0.006$ | +0.03  | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Offset Error Temperature Coefficient (TC) <sup>3</sup> |        | $\pm 3$     |        | $\mu\text{A}/^\circ\text{C}$ |                                  |
| Gain Error   | -0.08  |             | +0.08  | % FSR                        |                                  |
|  | -0.05  | $\pm 0.003$ | +0.05  | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Gain Temperature Coefficient (TC) <sup>3</sup>         |        | $\pm 4$     |        | ppm FSR/ $^\circ\text{C}$    |                                  |
| Full-Scale Error                                       | -0.15  |             | +0.15  | % FSR                        |                                  |
|  | -0.06  | $\pm 0.01$  | +0.06  | % FSR                        | $T_A = 25^\circ\text{C}$         |
| Full-Scale Temperature Coefficient (TC) <sup>3</sup>   |        | $\pm 7$     |        | ppm FSR/ $^\circ\text{C}$    |                                  |

# AD5412/AD5422

| Parameter <sup>1</sup>                                 | Min             | Typ | Max             | Unit                   | Test Conditions/Comments                          |
|--|-----------------|-----|-----------------|------------------------|---|
| <b>OUTPUT CHARACTERISTICS<sup>3</sup></b>              |                 |     |                 |                        |   |
| Current Loop Compliance Voltage                        | 0               |     | $AV_{DD} - 2.5$ | V                      | Drift after 1000 hours, $T_A = 125^\circ\text{C}$ |
| Output Current Drift vs. Time                          |                 | 50  |                 | ppm FSR                | Internal $R_{SET}$                                |
|  |                 | 20  |                 | ppm FSR                | External $R_{SET}$                                |
| Resistive Load   |                 |     | 1200            | $\Omega$               | $T_A = 25^\circ\text{C}$                          |
| Inductive Load   |                 | 50  |                 | mH                     |   |
| DC PSRR  |                 |     | 1               | $\mu\text{A/V}$        |   |
| Output Impedance                                       |                 | 50  |                 | M $\Omega$             |   |
| Output Current Leakage When Output Is Disabled         |                 | 60  |                 | pA                     |   |
| <b>REFERENCE INPUT/OUTPUT</b>                          |                 |     |                 |                        |   |
| Reference Input <sup>3</sup>                           |                 |     |                 |                        |   |
| Reference Input Voltage                                | 4.95            | 5   | 5.05            | V                      | For specified performance                         |
| DC Input Impedance                                     | 27              | 40  |                 | k $\Omega$             |   |
| Reference Output                                       |                 |     |                 |                        |   |
| Output Voltage   | 4.995           | 5   | 5.005           |                        | $T_A = 25^\circ\text{C}$                          |
| Reference Temperature Coefficient (TC) <sup>3, 5</sup> |                 | 1.8 | 10              | ppm/ $^\circ\text{C}$  |   |
| Output Noise (0.1 Hz to 10 Hz) <sup>3</sup>            |                 | 10  |                 | $\mu\text{V p-p}$      |   |
| Noise Spectral Density <sup>3</sup>                    |                 | 100 |                 | nV/ $\sqrt{\text{Hz}}$ | At 10 kHz   |
| Output Voltage Drift vs. Time <sup>3</sup>             |                 | 50  |                 | ppm                    | Drift after 1000 hours, $T_A = 125^\circ\text{C}$ |
| Capacitive Load <sup>3</sup>                           |                 | 600 |                 | nF                     |   |
| Load Current <sup>3</sup>                              |                 | 5   |                 | mA                     |   |
| Short-Circuit Current <sup>3</sup>                     |                 | 7   |                 | mA                     |   |
| Load Regulation <sup>3</sup>                           |                 | 95  |                 | ppm/mA                 |   |
| <b>DIGITAL INPUTS<sup>3</sup></b>                      |                 |     |                 |                        |   |
| Input High Voltage, $V_{IH}$                           | 2               |     |                 | V                      | JEDEC compliant                                   |
| Input Low Voltage, $V_{IL}$                            |                 |     | 0.8             | V                      |   |
| Input Current  | -1              |     | +1              | $\mu\text{A}$          | Per pin   |
| Pin Capacitance  |                 | 10  |                 | pF                     | Per pin   |
| <b>DIGITAL OUTPUTS<sup>3</sup></b>                     |                 |     |                 |                        |   |
| SDO  |                 |     |                 |                        |   |
| Output Low Voltage, $V_{OL}$                           |                 |     | 0.4             | V                      | Sinking 200 $\mu\text{A}$                         |
| Output High Voltage, $V_{OH}$                          | $DV_{CC} - 0.5$ |     |                 | V                      | Sourcing 200 $\mu\text{A}$                        |
| High Impedance Leakage Current                         | -1              |     | +1              | $\mu\text{A}$          |   |
| High Impedance Output Capacitance                      |                 | 5   |                 | pF                     |   |
| <b>FAULT</b>   |                 |     |                 |                        |   |
| Output Low Voltage, $V_{OL}$                           |                 |     | 0.4             | V                      | 10 k $\Omega$ pull-up resistor to $DV_{CC}$       |
| Output Low Voltage, $V_{OL}$                           |                 | 0.6 |                 | V                      | At 2.5 mA   |
| Output High Voltage, $V_{OH}$                          | 3.6             |     |                 | V                      | 10 k $\Omega$ pull-up resistor to $DV_{CC}$       |
| <b>POWER REQUIREMENTS</b>                              |                 |     |                 |                        |   |
| $AV_{DD}$  | 10.8            |     | 40              | V                      |   |
| $AV_{SS}$  | -26.4           |     | 0               | V                      |   |
| $ AV_{SS}  + AV_{DD}$                                  | 10.8            |     | 52.8            | V                      |   |
| $DV_{CC}$  |                 |     |                 |                        |   |
| Input Voltage  | 2.7             |     | 5.5             | V                      | Internal supply disabled                          |
| Output Voltage   |                 | 4.5 |                 | V                      | $DV_{CC}$ , which can be overdriven up to 5.5 V   |
| Output Load Current <sup>3</sup>                       |                 | 5   |                 | mA                     |   |
| Short-Circuit Current <sup>3</sup>                     |                 | 20  |                 | mA                     |   |

| Parameter <sup>1</sup>      | Min | Typ  | Max | Unit | Test Conditions/Comments   |
|-----------------------------|-----|------|-----|------|--|
| I <sub>DD</sub>             |     | 2.5  | 3   | mA   | Outputs unloaded   |
|                             |     | 3.4  | 4   | mA   | Outputs disabled   |
|                             |     | 3.9  | 4.4 | mA   | Current output enabled   |
| I <sub>SS</sub>             |     |      |     |      | Voltage output enabled   |
|                             |     | 0.24 | 0.3 | mA   | Outputs unloaded   |
|                             |     | 0.5  | 0.6 | mA   | Outputs disabled   |
| D <sub>I<sub>CC</sub></sub> |     | 1.1  | 1.4 | mA   | Current output enabled   |
|                             |     |      | 1   | mA   | Voltage output enabled   |
|                             |     |      |     | mA   | V <sub>IH</sub> = DV <sub>CC</sub> , V <sub>IL</sub> = GND           |
| Power Dissipation           |     | 128  |     | mW   | AV <sub>DD</sub> = 40 V, AV <sub>SS</sub> = 0 V, outputs unloaded    |
|                             |     | 120  |     | mW   | AV <sub>DD</sub> = +24 V, AV <sub>SS</sub> = -24 V, outputs unloaded |

<sup>1</sup> Temperature range: -40°C to +85°C; typical at +25°C.

<sup>2</sup> When the AD5412/AD5422 is powered with AV<sub>SS</sub> = 0 V, INL for the 0 V to 5 V and 0 V to 10 V ranges is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.

<sup>3</sup> Guaranteed by design and characterization; not production tested.

<sup>4</sup> For 0 mA to 20 mA and 0 mA to 24 mA ranges, INL is measured beginning from Code 256 for the AD5422 and Code 16 for the AD5412.

<sup>5</sup> The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from -40°C to +85°C.

## AC PERFORMANCE CHARACTERISTICS

AV<sub>DD</sub> = 10.8 V to 26.4 V, AV<sub>SS</sub> = -26.4 V to -3 V/0 V, AV<sub>DD</sub> + |AV<sub>SS</sub>| < 52.8 V, GND = 0 V, REFIN = +5 V external; DV<sub>CC</sub> = 2.7 V to 5.5 V. V<sub>OUT</sub>: R<sub>LOAD</sub> = 1 kΩ, C<sub>L</sub> = 200 pF, I<sub>OUT</sub>: R<sub>LOAD</sub> = 350 Ω; all specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 3.

| Parameter <sup>1</sup>                   | Min | Typ | Max | Unit    | Test Conditions/Comments  |
|--|-----|-----|-----|---------|---|
| DYNAMIC PERFORMANCE                      |     |     |     |         |   |
| Voltage Output                           |     |     |     |         |   |
| Output Voltage Settling Time             |     |     | 25  | μs      | 10 V step to ±0.03 % FSR  |
|  |     | 32  |     | μs      | 20 V step to ±0.03 % FSR  |
|  |     |     | 18  | μs      | 5 V step to ±0.03 % FSR   |
|  |     | 8   |     | μs      | 512 LSB step to ±0.03 % FSR (16-Bit LSB)                          |
| Slew Rate                                |     | 0.8 |     | V/μs    |   |
| Power-On Glitch Energy                   |     | 10  |     | nV-sec  |   |
| Digital-to-Analog Glitch Energy          |     | 10  |     | nV-sec  |   |
| Glitch Impulse Peak Amplitude            |     | 20  |     | mV      |   |
| Digital Feedthrough                      |     | 1   |     | nV-sec  |   |
| Output Noise (0.1 Hz to 10 Hz Bandwidth) |     | 0.1 |     | LSB p-p | 16-bit LSB  |
| Output Noise (100 kHz Bandwidth)         |     | 200 |     | μV rms  |   |
| 1/f Corner Frequency                     |     | 1   |     | kHz     |   |
| Output Noise Spectral Density            |     | 150 |     | nV/√Hz  | Measured at 10 kHz, midscale output, 10 V range                   |
| AC PSRR                                  |     | -75 |     | dB      | 200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage |
| Current Output                           |     |     |     |         |   |
| Output Current Settling Time             |     | 10  |     | μs      | 16 mA step to 0.1% FSR  |
|  |     | 40  |     | μs      | 16 mA step to 0.1% FSR, L = 1 mH                                  |
| AC PSRR                                  |     | -75 |     | dB      | 200 mV 50 Hz/60 Hz sine wave superimposed on power supply voltage |

<sup>1</sup> Guaranteed by characterization, not production tested.

# AD5412/AD5422

## TIMING CHARACTERISTICS

$AV_{DD} = 10.8 \text{ V to } 26.4 \text{ V}$ ,  $AV_{SS} = -26.4 \text{ V to } -3 \text{ V/0 V}$ ,  $AV_{DD} + |AV_{SS}| < 52.8 \text{ V}$ ,  $GND = 0 \text{ V}$ ,  $REFIN = +5 \text{ V external}$ ;  $DV_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$ .  
 $V_{OUT}$ :  $R_{LOAD} = 1 \text{ k}\Omega$ ,  $C_L = 200 \text{ pF}$ ,  $I_{OUT}$ :  $R_{LOAD} = 300 \Omega$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

**Table 4.**

| Parameter <sup>1, 2, 3</sup> | Limit at $T_{MIN}$ , $T_{MAX}$ | Unit              | Description  |
|------------------------------|--------------------------------|-------------------|--|
| <b>WRITE MODE</b>            |                                |                   |  |
| $t_1$                        | 33                             | ns min            | SCLK cycle time  |
| $t_2$                        | 13                             | ns min            | SCLK low time  |
| $t_3$                        | 13                             | ns min            | SCLK high time   |
| $t_4$                        | 13                             | ns min            | LATCH delay time   |
| $t_5$                        | 40                             | ns min            | LATCH high time  |
| $t_5$                        | 5                              | $\mu\text{s min}$ | LATCH high time (after a write to the control register)            |
| $t_6$                        | 5                              | ns min            | Data setup time  |
| $t_7$                        | 5                              | ns min            | Data hold time   |
| $t_8$                        | 40                             | ns min            | LATCH low time   |
| $t_9$                        | 20                             | ns min            | CLEAR pulse width  |
| $t_{10}$                     | 5                              | $\mu\text{s max}$ | CLEAR activation time  |
| <b>READBACK MODE</b>         |                                |                   |  |
| $t_{11}$                     | 90                             | ns min            | SCLK cycle time  |
| $t_{12}$                     | 40                             | ns min            | SCLK low time  |
| $t_{13}$                     | 40                             | ns min            | SCLK high time   |
| $t_{14}$                     | 13                             | ns min            | LATCH delay time   |
| $t_{15}$                     | 40                             | ns min            | LATCH high time  |
| $t_{16}$                     | 5                              | ns min            | Data setup time  |
| $t_{17}$                     | 5                              | ns min            | Data hold time   |
| $t_{18}$                     | 40                             | ns min            | LATCH low time   |
| $t_{19}$                     | 35                             | ns max            | Serial output delay time ( $C_{LSDO}^4 = 15 \text{ pF}$ )          |
| $t_{20}$                     | 35                             | ns max            | LATCH rising edge to SDO tristate ( $C_{LSDO}^4 = 15 \text{ pF}$ ) |
| <b>DAISY-CHAIN MODE</b>      |                                |                   |  |
| $t_{21}$                     | 90                             | ns min            | SCLK cycle time  |
| $t_{22}$                     | 40                             | ns min            | SCLK low time  |
| $t_{23}$                     | 40                             | ns min            | SCLK high time   |
| $t_{24}$                     | 13                             | ns min            | LATCH delay time   |
| $t_{25}$                     | 40                             | ns min            | LATCH high time  |
| $t_{26}$                     | 5                              | ns min            | Data setup time  |
| $t_{27}$                     | 5                              | ns min            | Data hold time   |
| $t_{28}$                     | 40                             | ns min            | LATCH low time   |
| $t_{29}$                     | 35                             | ns max            | Serial output delay time ( $C_{LSDO}^4 = 15 \text{ pF}$ )          |

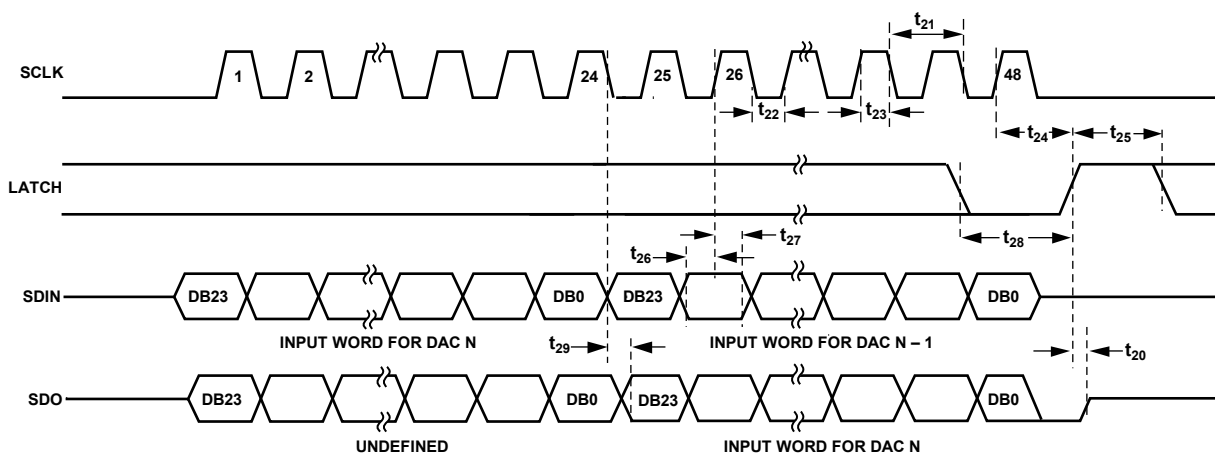
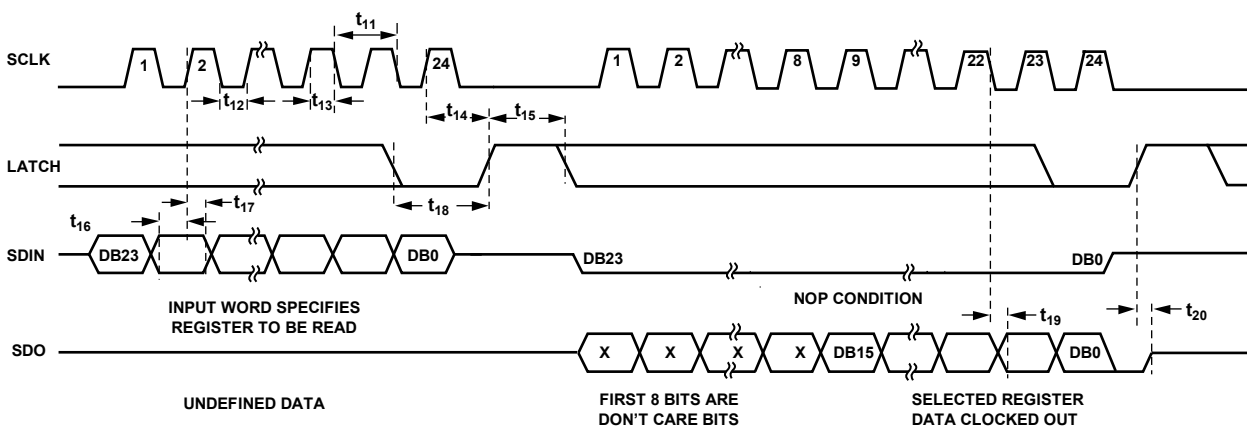
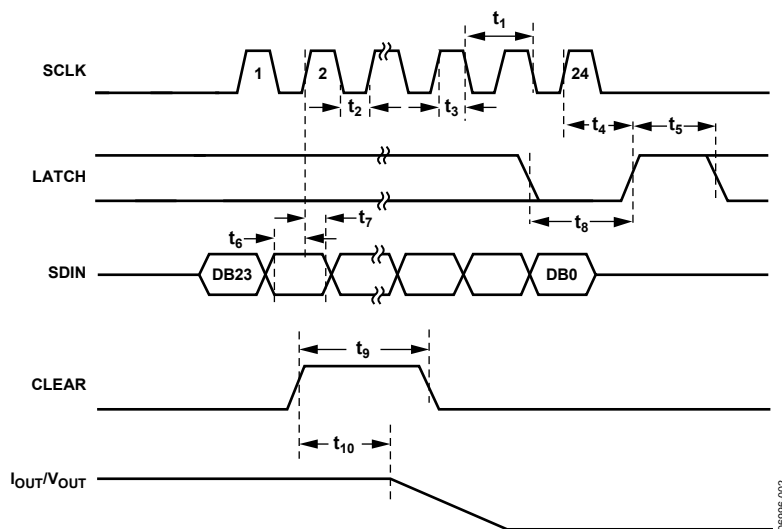
<sup>1</sup> Guaranteed by characterization; not production tested.

<sup>2</sup> All input signals are specified with  $t_R = t_F = 5 \text{ ns}$  (10% to 90% of  $DV_{CC}$ ) and timed from a voltage level of 1.2 V.

<sup>3</sup> See Figure 2, Figure 3, and Figure 4.

<sup>4</sup>  $C_{LSDO}$  = capacitive load on SDO output.





## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. Transient currents of up to 80 mA do not cause SCR latch-up.

Table 5.

| Parameter  | Rating   |
|--|--|
| $AV_{DD}$ to GND   | $-0.3\text{ V to }+48\text{ V}$  |
| $AV_{SS}$ to GND   | $+0.3\text{ V to }-28\text{ V}$  |
| $AV_{DD}$ to $AV_{SS}$   | $-0.3\text{ V to }+60\text{ V}$  |
| $DV_{CC}$ to GND   | $-0.3\text{ V to }+7\text{ V}$   |
| Digital Inputs to GND  | $-0.3\text{ V to }DV_{CC} + 0.3\text{ V or }7\text{ V}$<br>(whichever is less) |
| Digital Outputs to GND   | $-0.3\text{ V to }DV_{CC} + 0.3\text{ V or }7\text{ V}$<br>(whichever is less) |
| REFIN/REFOUT to GND  | $-0.3\text{ V to }+7\text{ V}$   |
| $V_{OUT}$ to GND   | $AV_{SS}$ to $AV_{DD}$   |
| $I_{OUT}$ to GND   | $-0.3\text{ V to }AV_{DD}$   |
| Operating Temperature Range ( $T_A$ )<br>Industrial <sup>1</sup> | $-40^\circ\text{C to }+85^\circ\text{C}$                                       |
| Storage Temperature Range  | $-65^\circ\text{C to }+150^\circ\text{C}$                                      |
| Junction Temperature ( $T_J$ max)                                | $125^\circ\text{C}$  |
| 24-Lead TSSOP Package<br>$\theta_{JA}$ Thermal Impedance         | $42^\circ\text{C/W}$   |
| 40-Lead LFCSP Package<br>$\theta_{JA}$ Thermal Impedance         | $28^\circ\text{C/W}$   |
| Power Dissipation  | $(T_J \text{ max} - T_A)/\theta_{JA}$  |
| Lead Temperature<br>Soldering                                    | JEDEC industry standard<br>J-STD-020   |
| ESD (Human Body Model)   | 2 kV   |

<sup>1</sup> Power dissipated on chip must be derated to keep the junction temperature below  $125^\circ\text{C}$ , assuming that the maximum power dissipation condition is sourcing 24 mA into GND from  $I_{OUT}$  with a 4 mA on-chip current.

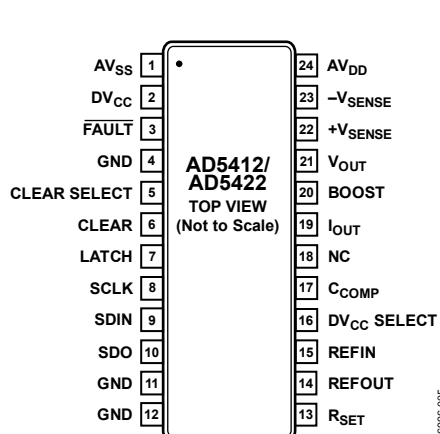
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

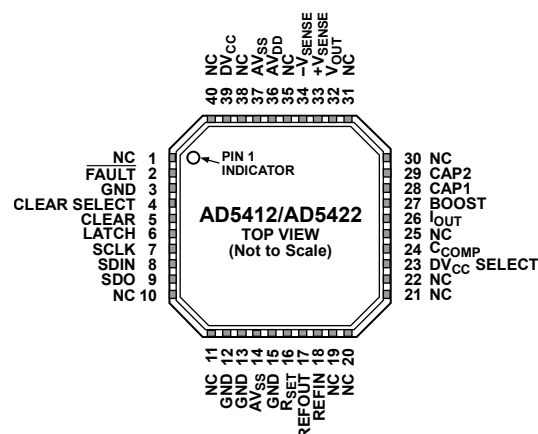
## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



## NOTES

1. NC = NO CONNECT
2. THE PADDLE CAN BE CONNECTED TO 0V IF THE OUTPUT VOLTAGE RANGE IS UNIPOLAR. THE PADDLE CAN BE LEFT ELECTRICALLY UNCONNECTED PROVIDED THAT A SUPPLY CONNECTION IS MADE AT THE AV<sub>SS</sub> PIN. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 5. TSSOP Pin Configuration



## NOTES

1. NC = NO CONNECT.
2. THE EXPOSED PADDLE CAN BE CONNECTED TO 0V IF THE OUTPUT VOLTAGE RANGE IS UNIPOLAR. THE EXPOSED PADDLE CAN BE LEFT ELECTRICALLY UNCONNECTED PROVIDED THAT A SUPPLY CONNECTION IS MADE AT THE AV<sub>SS</sub> PIN. IT IS RECOMMENDED THAT THE PADDLE BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE.

Figure 6. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. |   | Mnemonic         | Description  |
|---------|---|------------------|--|
| TSSOP   | LFCSP   |                  |  |
| 1       | 14, 37  | AV <sub>SS</sub> | Negative Analog Supply Pin. Voltage ranges from -3 V to -24 V. This pin can be connected to 0 V if the output voltage range is unipolar.   |
| 2       | 39  | DV <sub>CC</sub> | Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.  |
| 3       | 2   | FAULT            | Fault Alert. This pin is asserted low when an open circuit is detected in current mode or an overtemperature is detected. Open drain output must be connected to a pull-up resistor.                 |
| 4, 12   | 3, 15   | GND              | These pins must be connected to 0 V.   |
| 18      | 1, 10, 11, 19, 20, 21, 22, 25, 30, 31, 35, 38, 40 | NC               | No Connection. Do not connect to these pins.   |
| 5       | 4   | CLEAR SELECT     | Selects the voltage output clear value, either zero-scale or midscale code (see Table 21).   |
| 6       | 5   | CLEAR            | Active High Input. Asserting this pin sets the current output to the bottom of the selected range or sets the voltage output to the user selected value (zero-scale or midscale).                    |
| 7       | 6   | LATCH            | Positive Edge Sensitive Latch. A rising LATCH edge parallel loads the input shift register data into the DAC register, also updating the output.   |
| 8       | 7   | SCLK             | Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.   |
| 9       | 8   | SDIN             | Serial Data Input. Data must be valid on the rising edge of SCLK.  |
| 10      | 9   | SDO              | Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is valid on the rising edge of SCLK (see Figure 3 and Figure 4).                               |
| 11      | 12, 13  | GND              | Ground Reference Pin.  |
| 13      | 16  | R <sub>SET</sub> | An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I <sub>OUT</sub> temperature drift performance. See the AD5412/AD5422 Features section. |
| 14      | 17  | REFOUT           | Internal Reference Voltage Output. REFOUT = 5 V ± 2 mV.  |
| 15      | 18  | REFIN            | External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for a specified performance.  |

# AD5412/AD5422

| Pin No.   |           | Mnemonic                   | Description   |
|-----------|-----------|----------------------------|---|
| TSSOP     | LFCSP     |                            |   |
| 16        | 23        | DV <sub>CC</sub><br>SELECT | When connected to GND, this pin disables the internal supply, and an external supply must be connected to the DV <sub>CC</sub> pin. Leave this pin unconnected to enable the internal supply. See the AD5412/AD5422 Features section.   |
| 17        | 24        | C <sub>COMP</sub>          | Optional compensation capacitor connection for the voltage output buffer. Connecting a 4 nF capacitor between this pin and the V <sub>OUT</sub> pin allows the voltage output to drive up to 1 $\mu$ F. It should be noted that the addition of this capacitor reduces the bandwidth of the output amplifier, increasing the settling time.                                     |
| 19        | 26        | I <sub>OUT</sub>           | Current Output Pin.   |
| 20        | 27        | BOOST                      | Optional External Transistor Connection. Connecting an external transistor reduces the power dissipated in the AD5412/AD5422. See the AD5412/AD5422 Features section.   |
| N/A       | 28, 29    | CAP1, CAP2                 | Connection for Optional Output Filtering Capacitor. See the AD5412/AD5422 Features section.   |
| 21        | 32        | V <sub>OUT</sub>           | Buffered Analog Output Voltage. The output amplifier is capable of directly driving a 1 k $\Omega$ , 2000 pF load.  |
| 22        | 33        | +V <sub>SENSE</sub>        | Sense connection for the positive voltage output load connection.   |
| 23        | 34        | -V <sub>SENSE</sub>        | Sense connection for the negative voltage output load connection.   |
| 24        | 36        | AV <sub>DD</sub>           | Positive Analog Supply Pin. Voltage ranges from 10.8 V to 60 V.   |
| 25 (EPAD) | 41 (EPAD) | Exposed paddle             | Negative Analog Supply Pin. Voltage ranges from -3 V to -24 V. This paddle can be connected to 0 V if the output voltage range is unipolar. The paddle can be left electrically unconnected provided that a supply connection is made at the AV <sub>SS</sub> pin. It is recommended that the paddle be thermally connected to a copper plane for enhanced thermal performance. |

# TYPICAL PERFORMANCE CHARACTERISTICS

## GENERAL

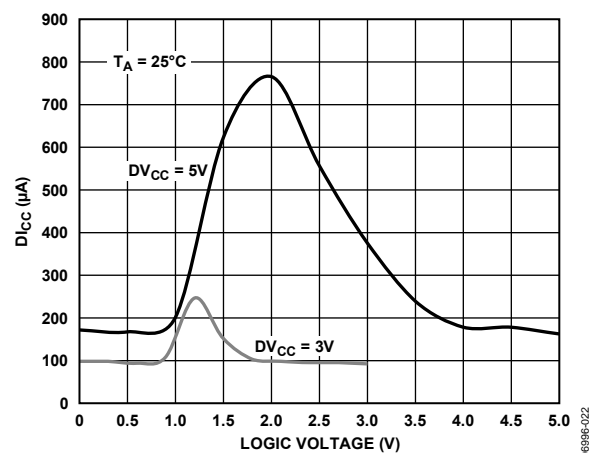
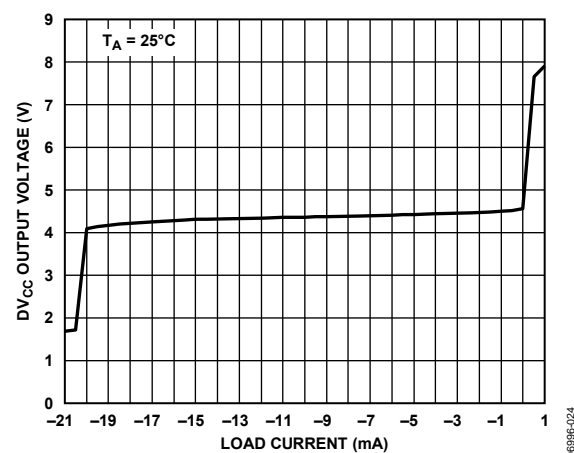
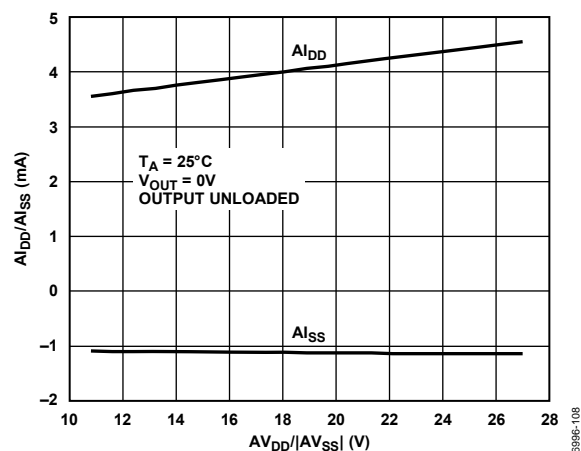
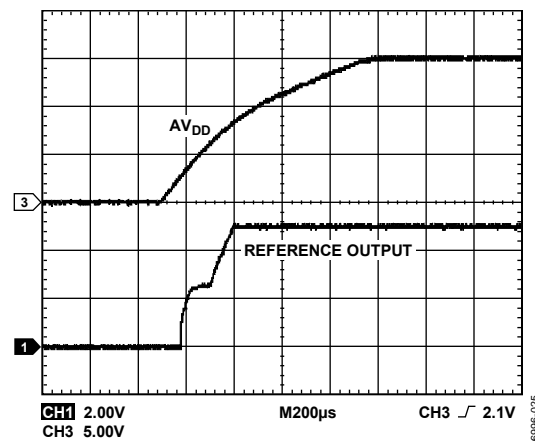
Figure 7.  $D_{Le}$  vs. Logic Input VoltageFigure 10.  $DV_{CC}$  Output Voltage vs. Load CurrentFigure 8.  $A_{Le}/A_{Iss}$  vs.  $AV_{DD}/AV_{Ssl}$ 

Figure 11. REFOUT Turn-on Transient

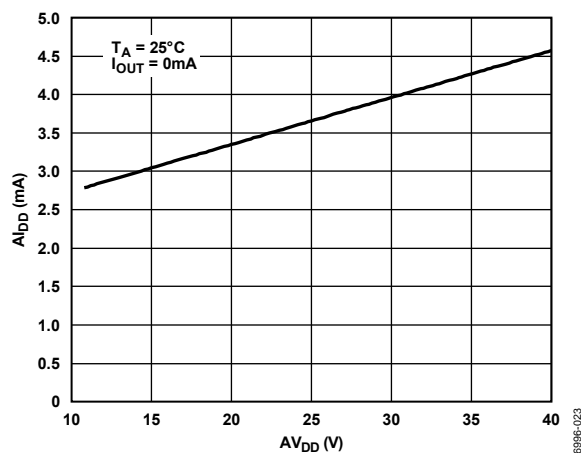
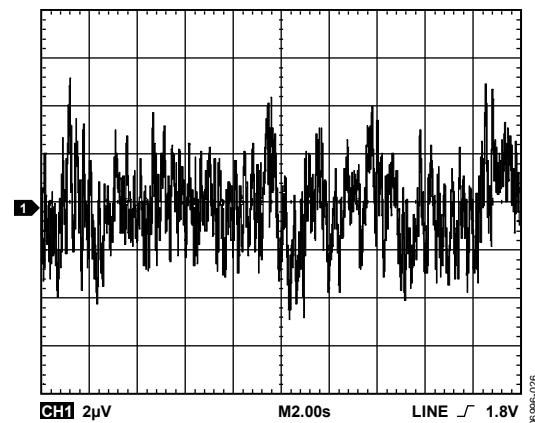
Figure 9.  $A_{Le}$  vs.  $AV_{DD}$ 

Figure 12. REFOUT Output Noise (0.1 Hz to 10 Hz Bandwidth)

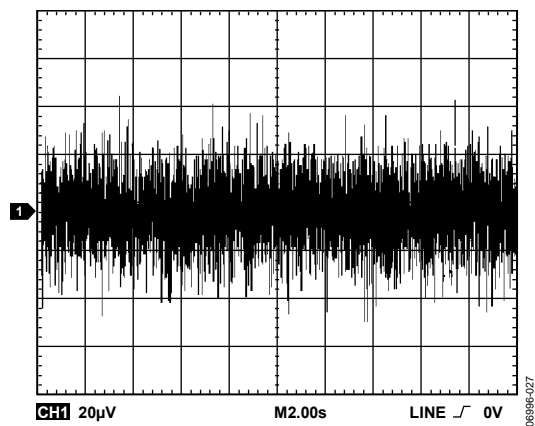


Figure 13. REFOUT Output Noise (100 kHz Bandwidth)

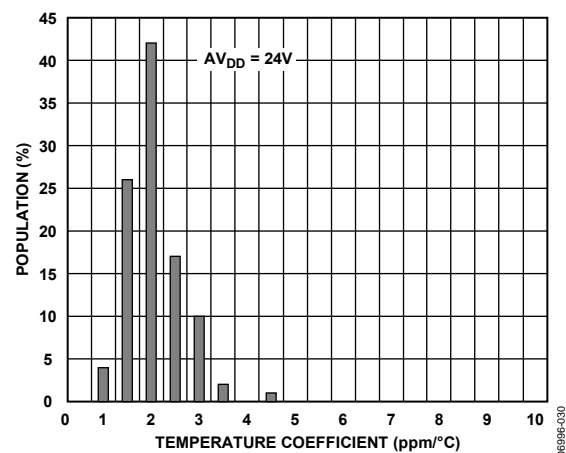


Figure 15. Reference Temperature Coefficient Histogram

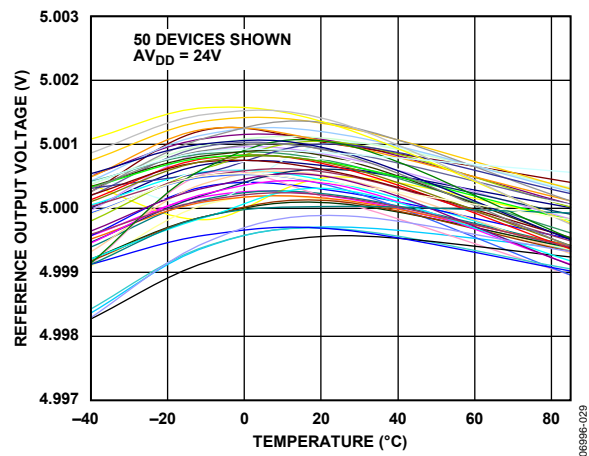


Figure 14. Reference Voltage vs. Temperature

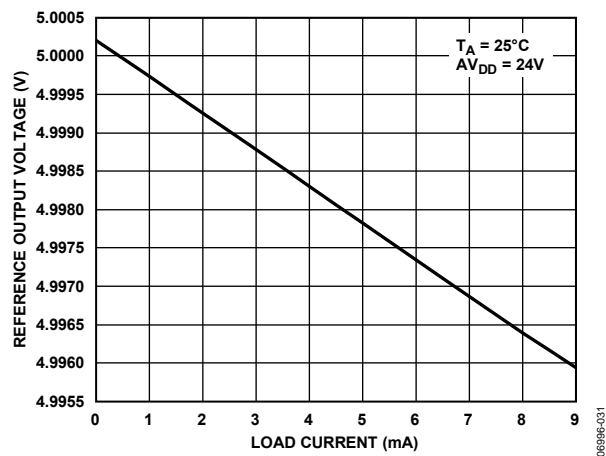


Figure 16. Reference Voltage vs. Load Current

## VOLTAGE OUTPUT

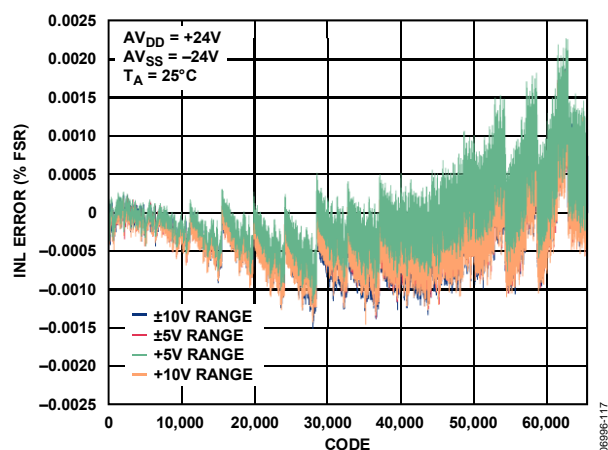


Figure 17. Integral Nonlinearity Error vs. DAC Code, Dual Supply

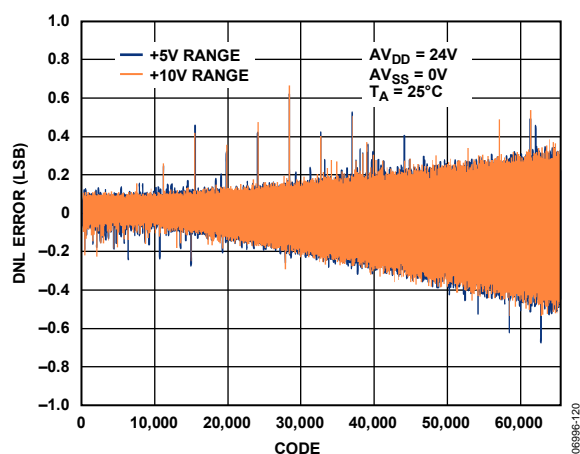


Figure 20. Differential Nonlinearity Error vs. DAC Code, Single Supply

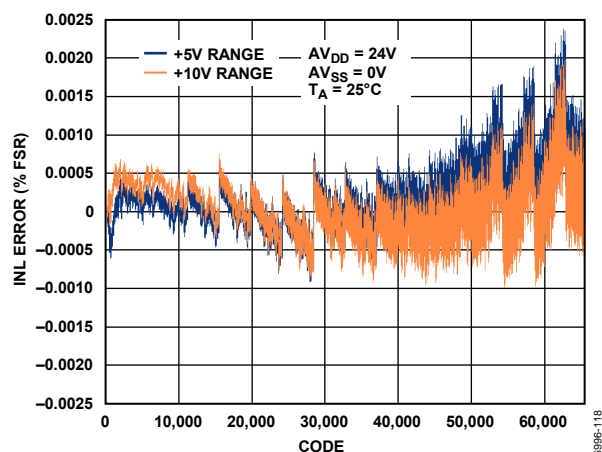


Figure 18. Integral Nonlinearity Error vs. DAC Code, Single Supply

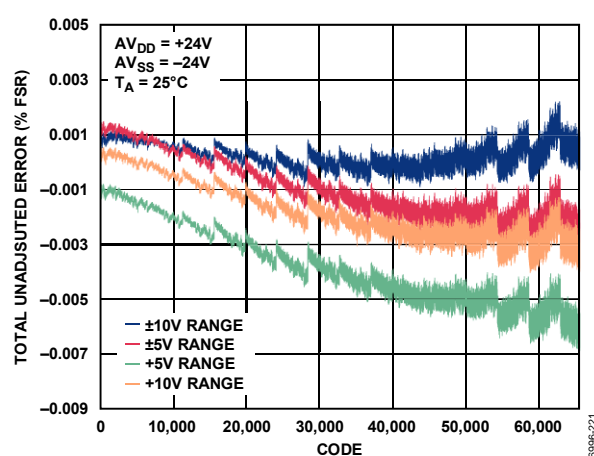


Figure 21. Total Unadjusted Error vs. DAC Code, Dual Supply

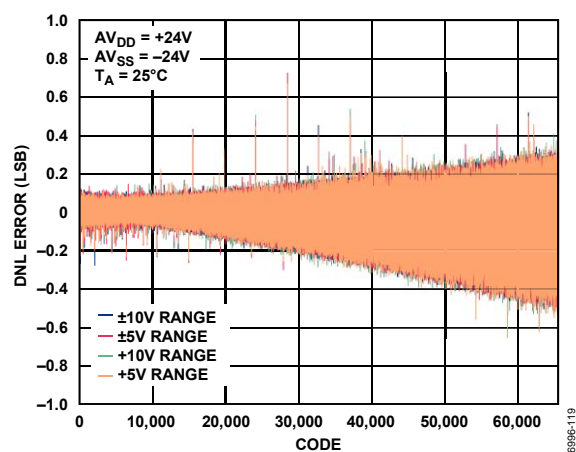


Figure 19. Differential Nonlinearity Error vs. DAC Code, Dual Supply

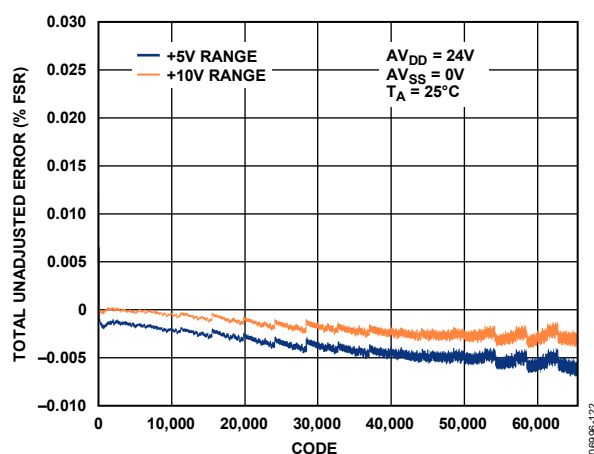


Figure 22. Total Unadjusted Error vs. DAC Code, Single Supply

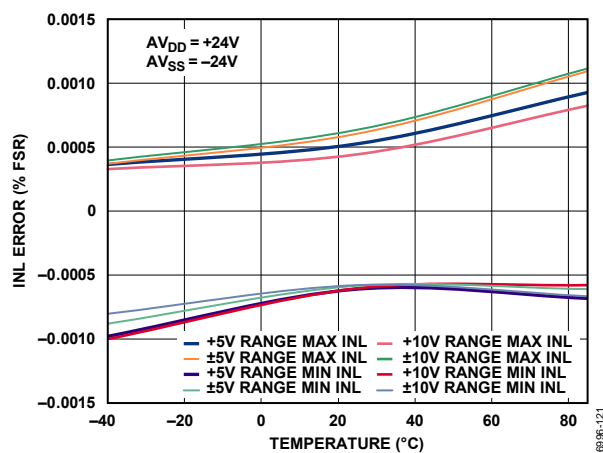


Figure 23. Integral Nonlinearity Error vs. Temperature

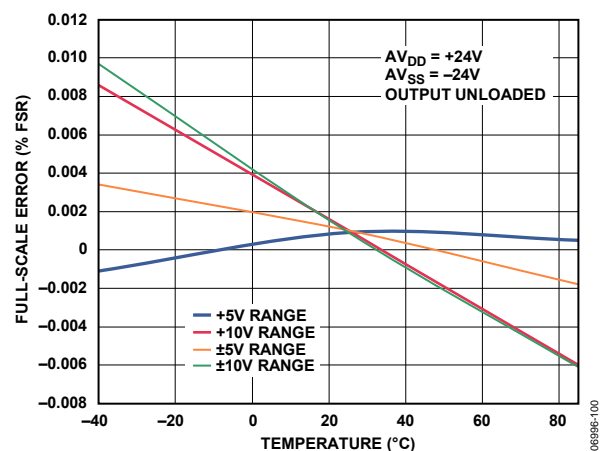


Figure 26. Full-Scale Error vs. Temperature

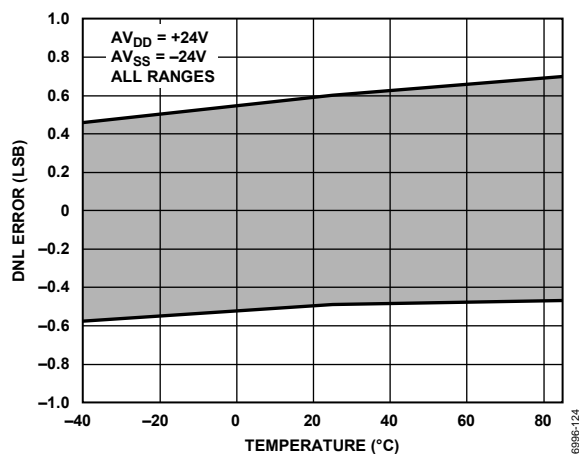


Figure 24. Differential Nonlinearity Error vs. Temperature

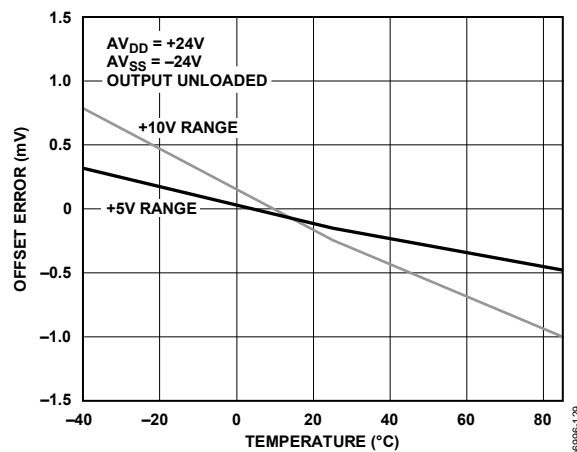


Figure 27. Offset Error vs. Temperature

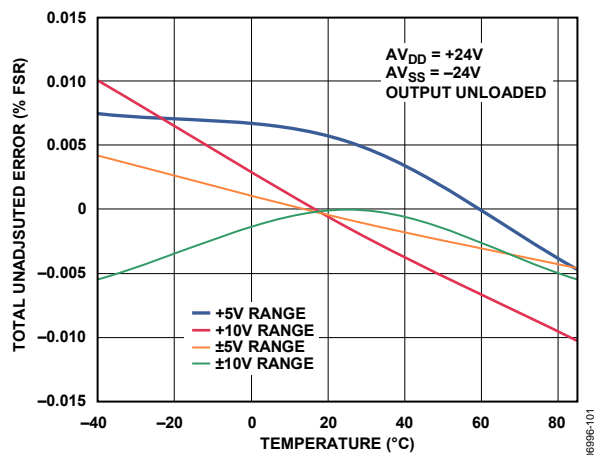


Figure 25. Total Unadjusted Error vs. Temperature

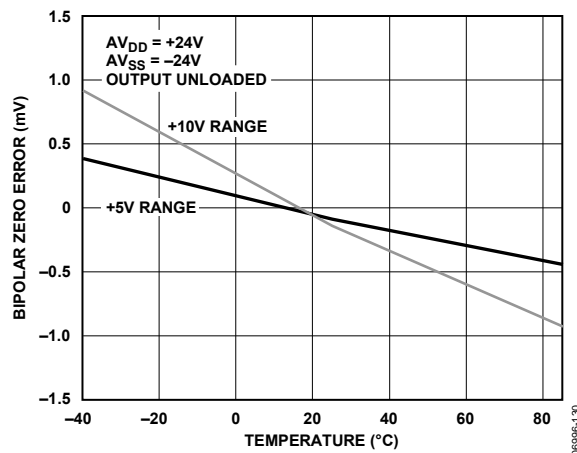


Figure 28. Bipolar Zero Error vs. Temperature



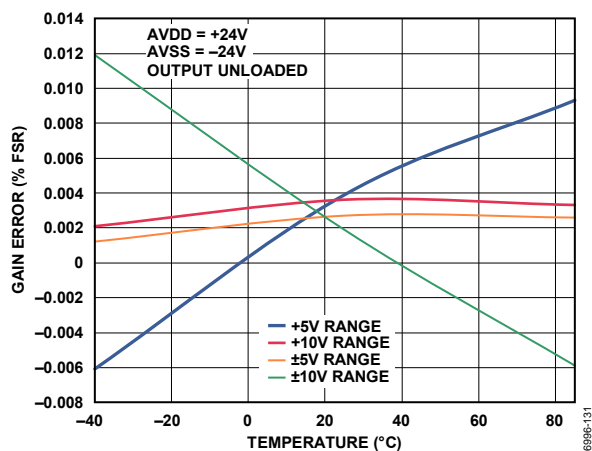


Figure 29. Gain Error vs. Temperature

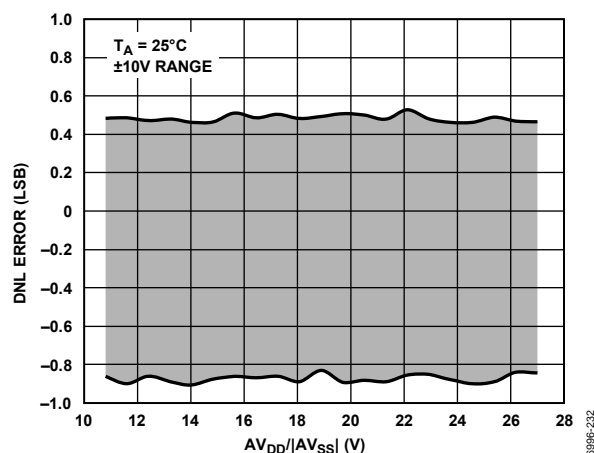


Figure 32. Differential Nonlinearity Error vs.  $AV_{DD}/AV_{SS}$

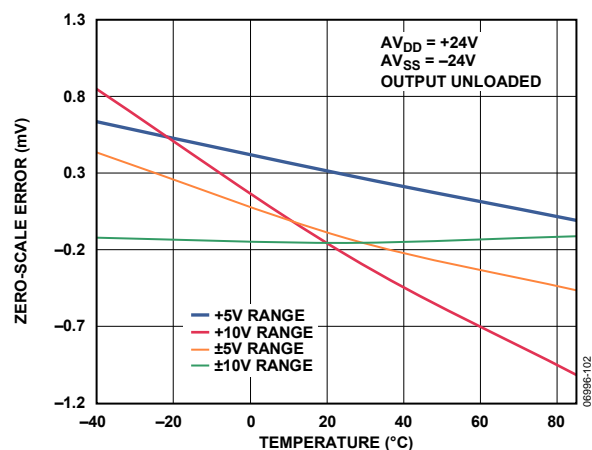


Figure 30. Zero-Scale Error vs. Temperature

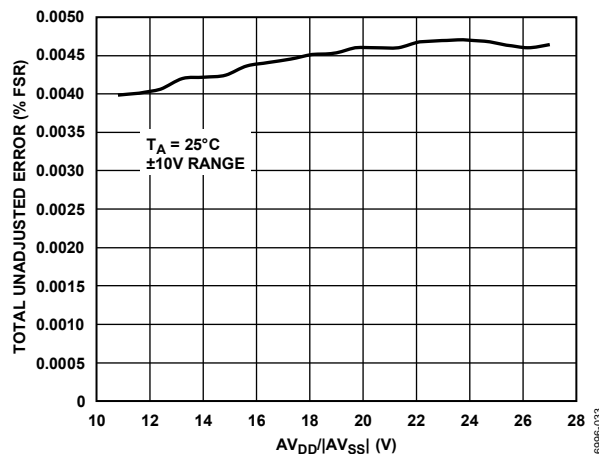


Figure 33. Total Unadjusted Error vs.  $AV_{DD}/AV_{SS}$

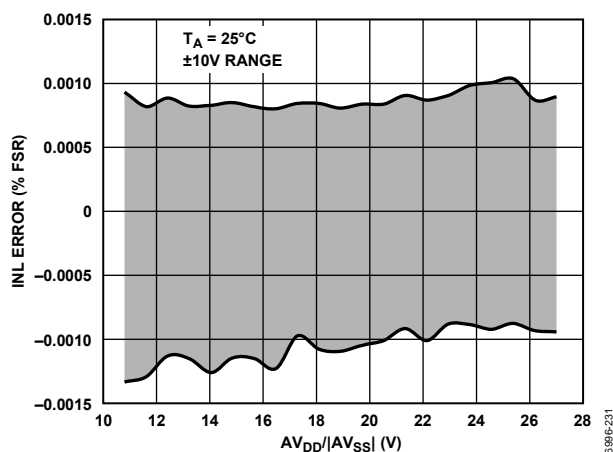


Figure 31. Integral Nonlinearity Error vs.  $AV_{DD}/AV_{SS}$

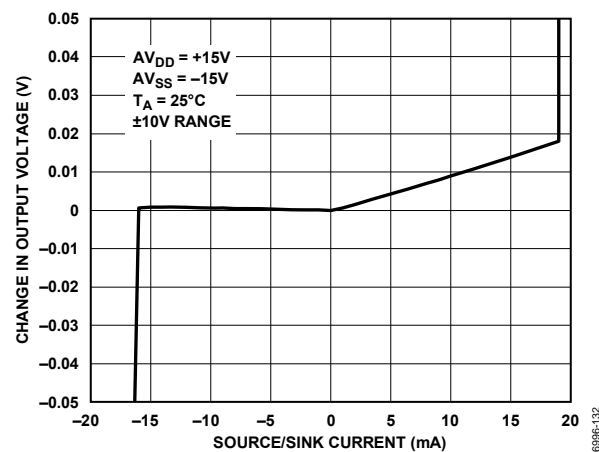


Figure 34. Source and Sink Capability of Output Amplifier, Full-Scale Code Loaded

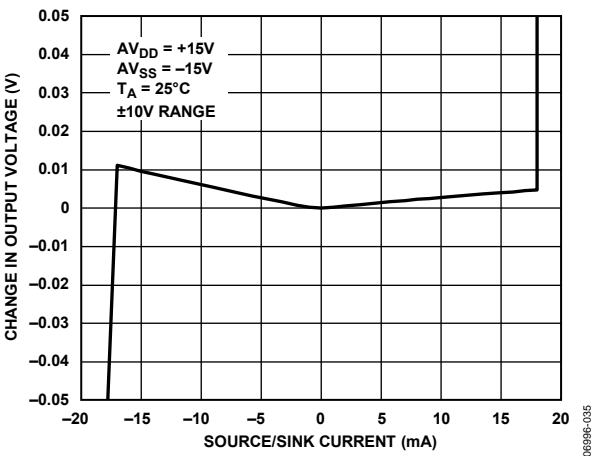


Figure 35. Source and Sink Capability of Output Amplifier, Zero-Scale Loaded

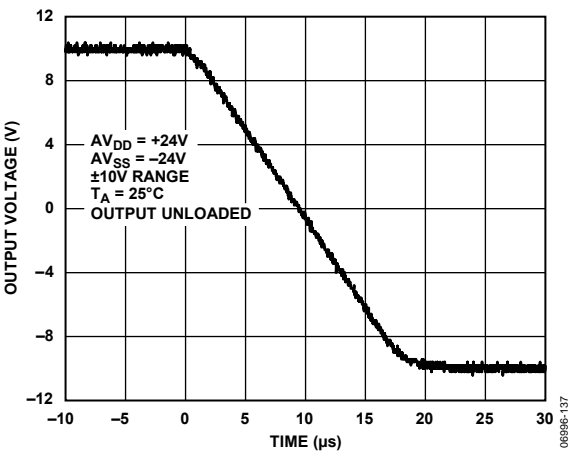


Figure 37. Full-Scale Negative Step

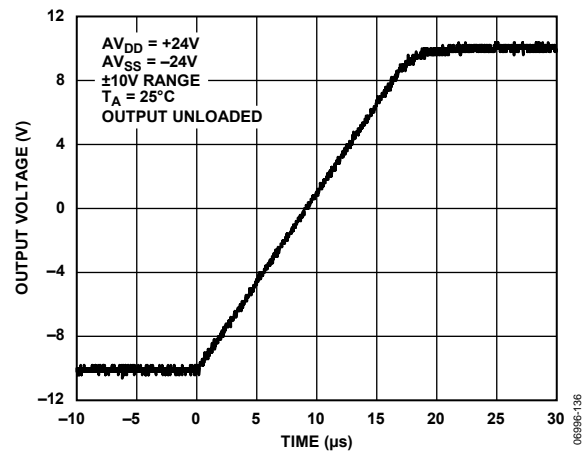


Figure 36. Full-Scale Positive Step

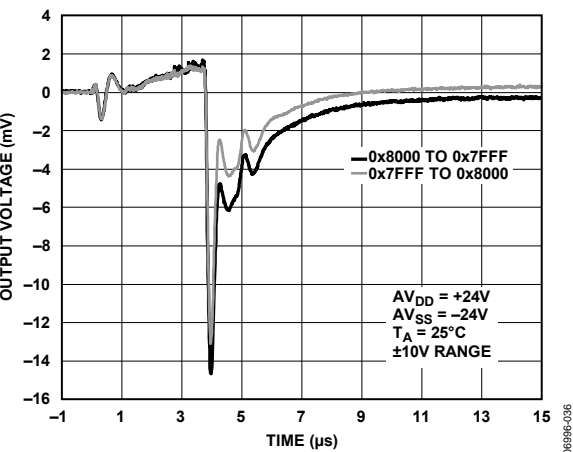


Figure 38. Digital-to-Analog Glitch

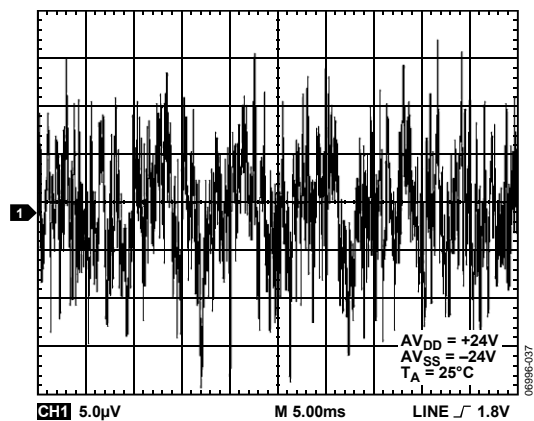


Figure 39. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

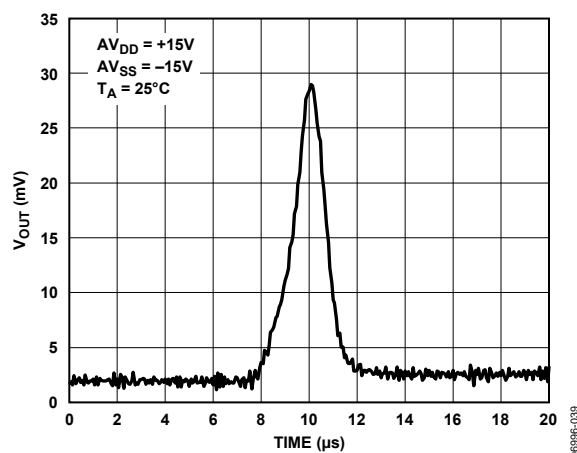
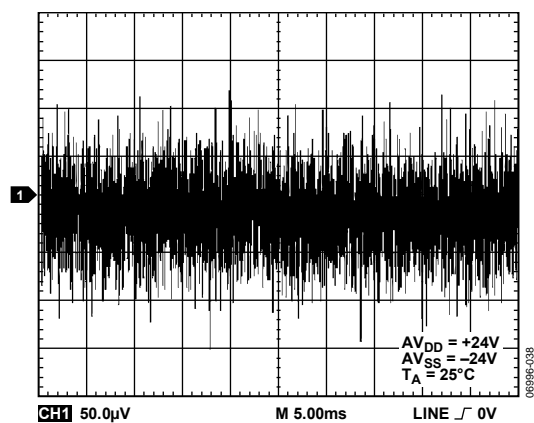
Figure 41. V<sub>OUT</sub> vs. Time on Power-Up

Figure 40. Peak-to-Peak Noise (100 kHz Bandwidth)

## CURRENT OUTPUT

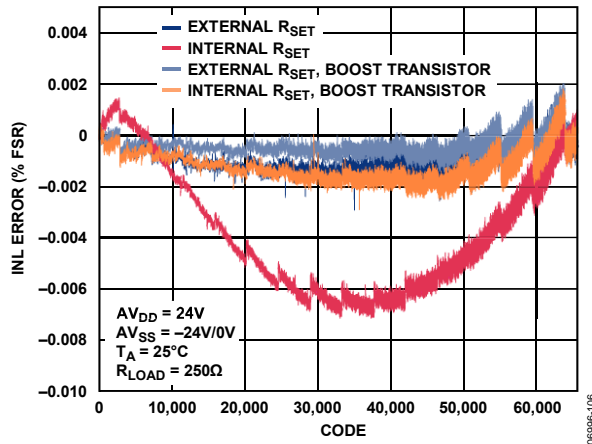


Figure 42. Integral Nonlinearity vs. Code

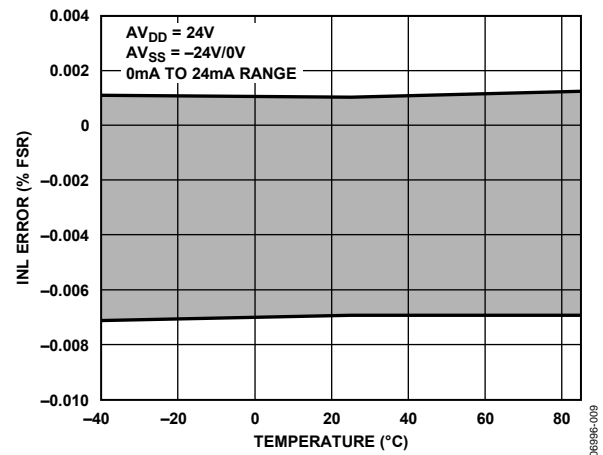


Figure 45. Integral Nonlinearity vs. Temperature, Internal  $R_{SET}$

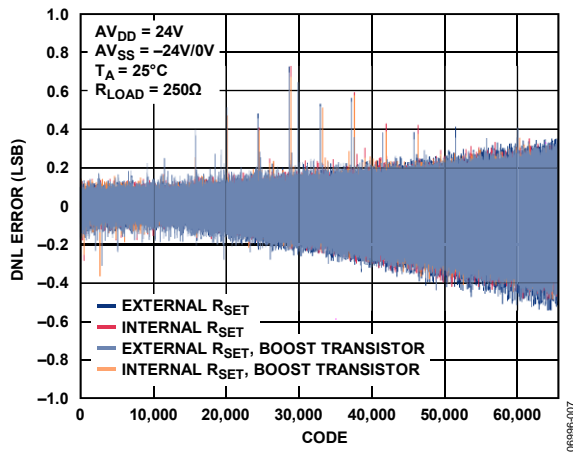


Figure 43. Differential Nonlinearity vs. Code

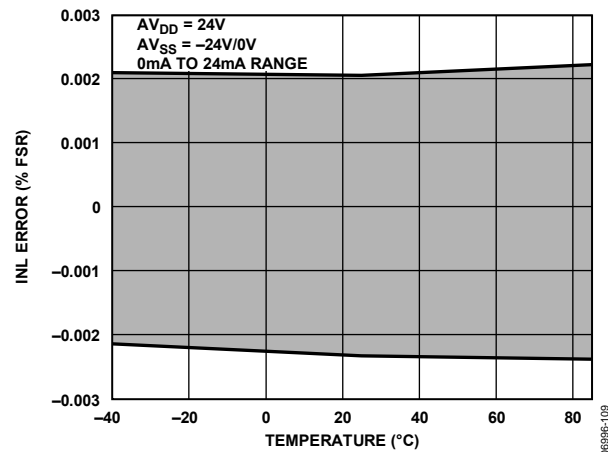


Figure 46. Integral Nonlinearity vs. Temperature, External  $R_{SET}$

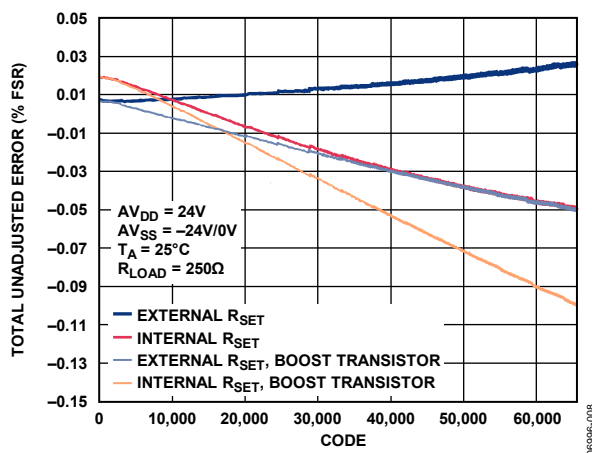


Figure 44. Total Unadjusted Error vs. Code

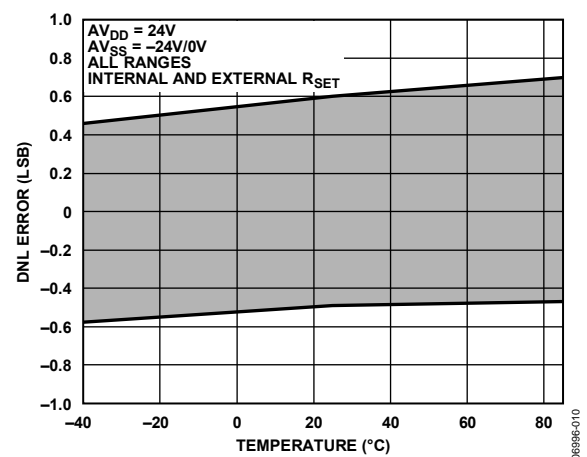


Figure 47. Differential Nonlinearity vs. Temperature

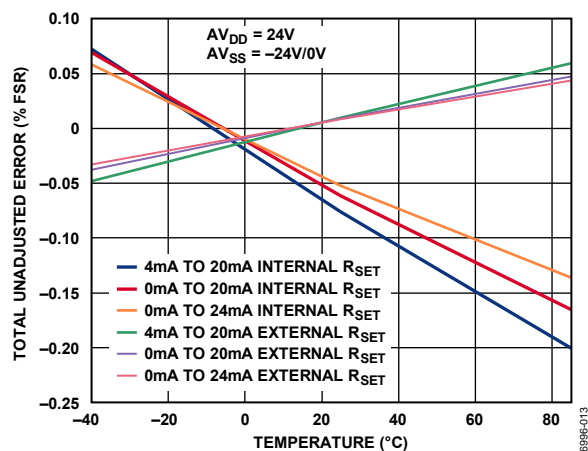


Figure 48. Total Unadjusted Error vs. Temperature

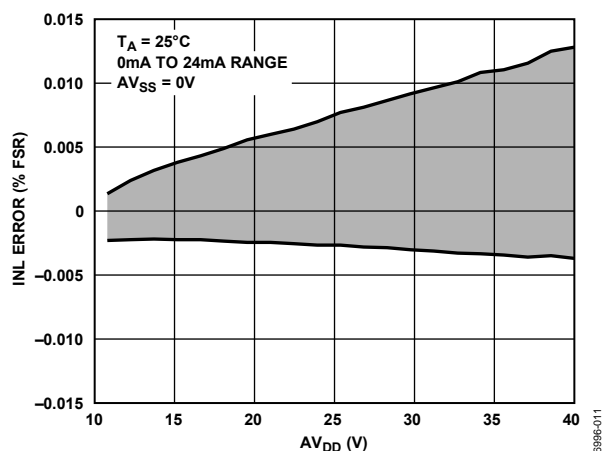
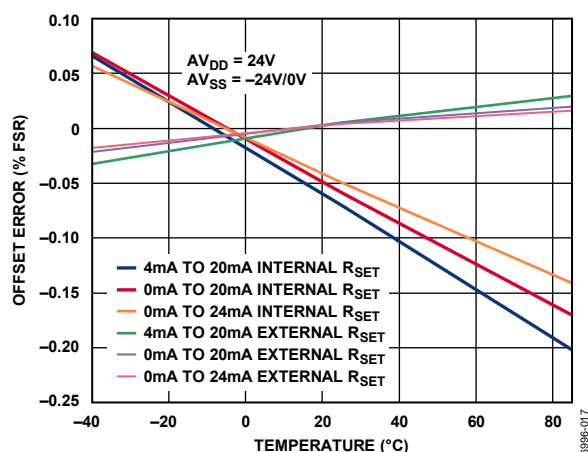
Figure 51. Integral Nonlinearity Error vs.  $AV_{DD}$ , External  $R_{SET}$ 

Figure 49. Offset Error vs. Temperature

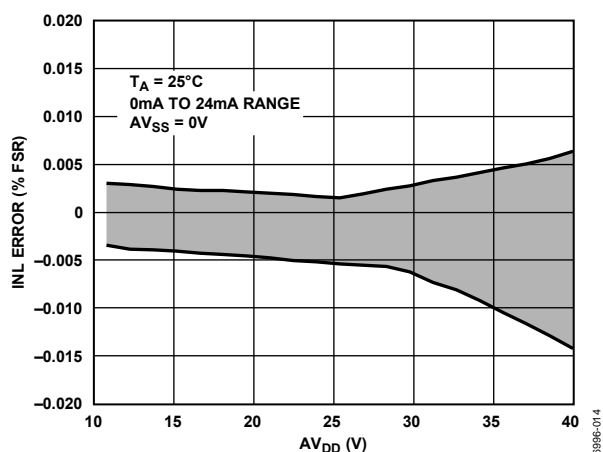
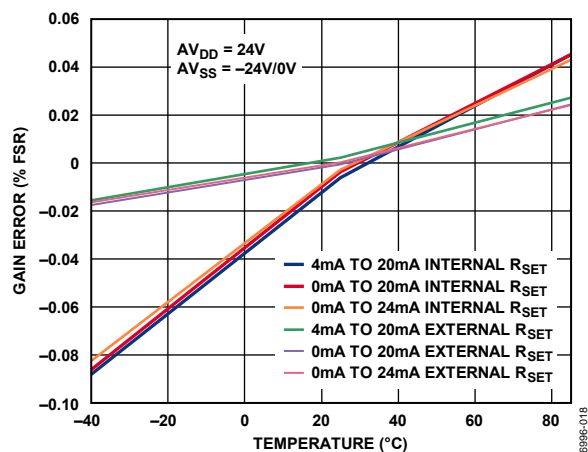
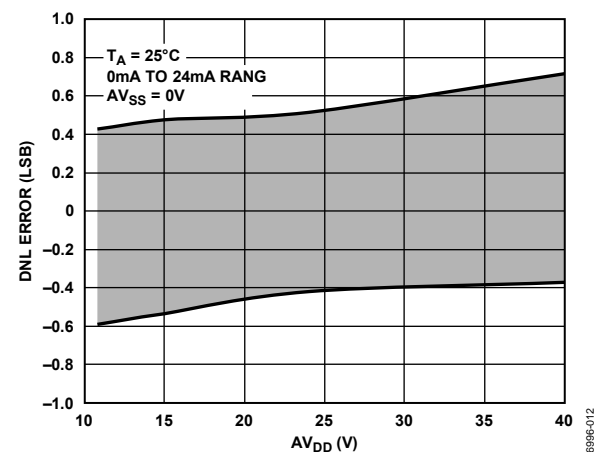
Figure 52. Integral Nonlinearity Error vs.  $AV_{DD}$ , Internal  $R_{SET}$ 

Figure 50. Gain Error vs. Temperature

Figure 53. Differential Nonlinearity Error vs.  $AV_{DD}$ , External  $R_{SET}$

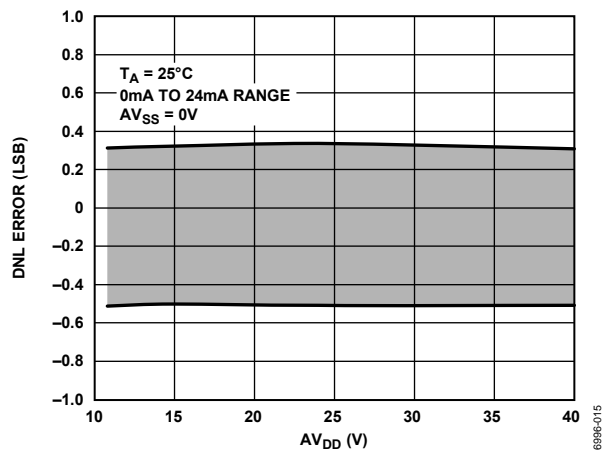


Figure 54. Differential Nonlinearity Error vs.  $AV_{DD}$ , Internal  $R_{SET}$

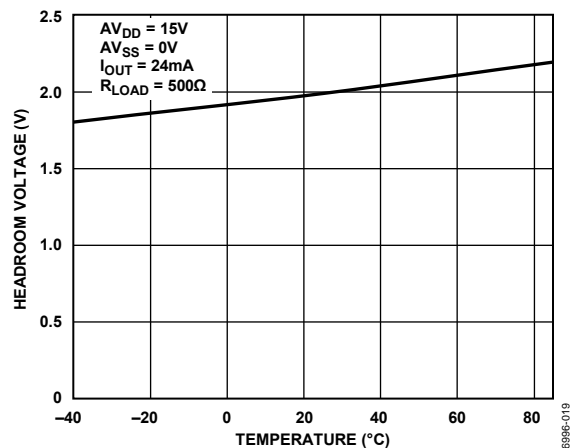


Figure 57. Compliance Voltage Headroom vs. Temperature

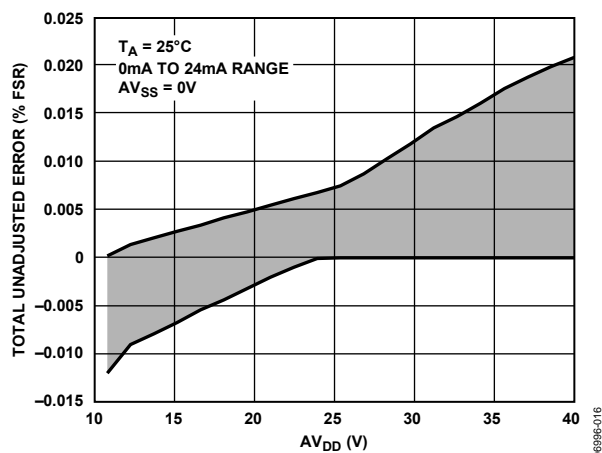


Figure 55. Total Unadjusted Error vs.  $AV_{DD}$ , External  $R_{SET}$

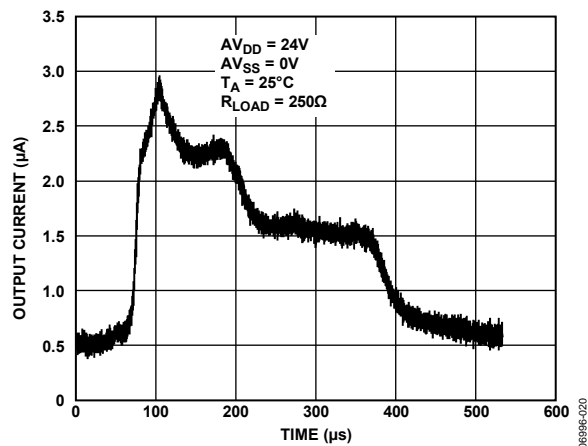


Figure 58. Output Current vs. Time on Power-Up

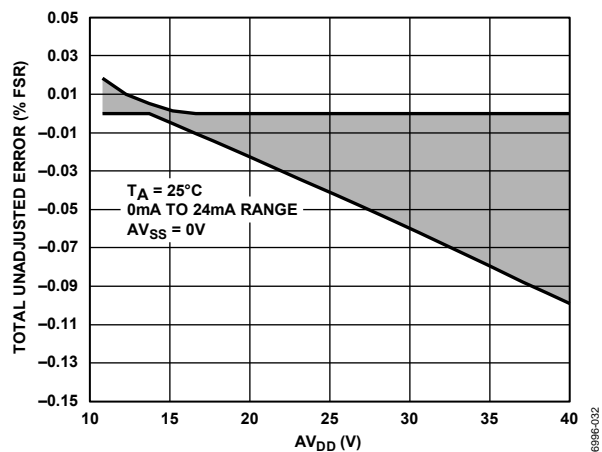


Figure 56. Total Unadjusted Error vs.  $AV_{DD}$ , Internal  $R_{SET}$

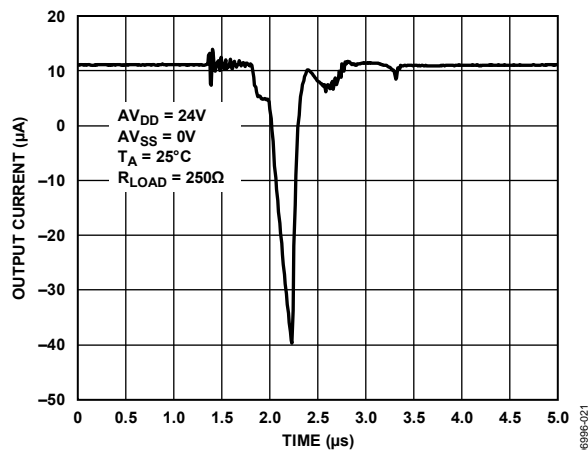


Figure 59. Output Current vs. Time on Output Enable

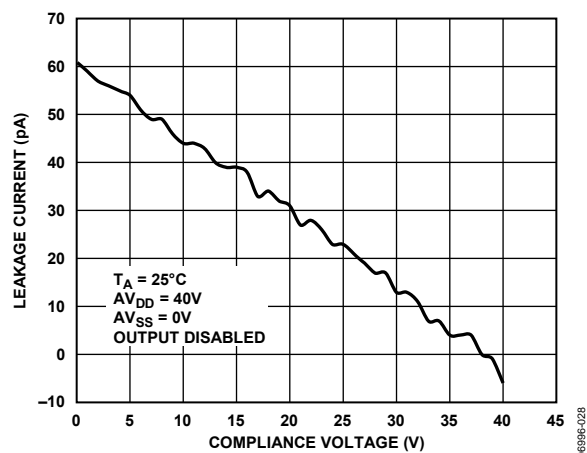


Figure 60. Output Leakage Current vs. Compliance Voltage

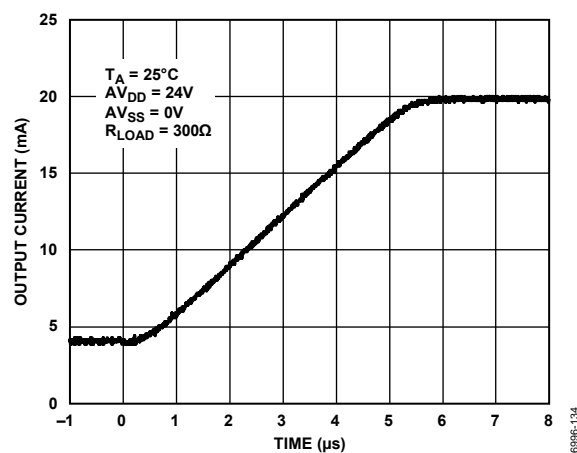


Figure 62. 4 mA to 20 mA Output Current Step

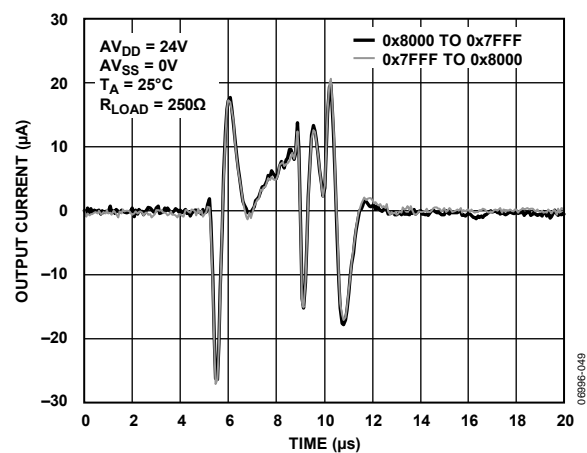


Figure 61. Digital to Analog Glitch

## TERMINOLOGY

### Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy, or INL, is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 17.

### Differential Nonlinearity (DNL)

DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 19.

### Monotonicity

A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5412/AD5422 are monotonic over their full operating temperature range.

### Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding) or 0x0000 (twos complement coding). A plot of bipolar zero error vs. temperature can be seen in Figure 28.

### Bipolar Zero Temperature Coefficient (TC)

Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/ $^{\circ}$ C.

### Full-Scale Error

Full-scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale – 1 LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

### Negative Full-Scale Error/Zero-Scale Error

Negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) or 0x8000 (twos complement coding) is loaded to the DAC register. Ideally, the output voltage should be negative full-scale – 1 LSB. A plot of zero-scale error vs. temperature can be seen in Figure 30.

### Zero-Scale Temperature Coefficient (TC)

Zero-scale TC is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/ $^{\circ}$ C.

### Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

### Slew Rate

The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output DAC is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is expressed in V/ $\mu$ s.

### Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Figure 29.

### Gain Error Temperature Coefficient (TC)

Gain error TC is a measure of the change in gain error with changes in temperature. Gain error TC is expressed in ppm FSR/ $^{\circ}$ C.

### Total Unadjusted Error (TUE)

TUE is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

### Current Loop Voltage Compliance

The maximum voltage at the I<sub>OUT</sub> pin for which the output current is equal to the programmed value.

### Power-On Glitch Energy

Power-on glitch energy is the impulse injected into the analog output when the AD5412/AD5422 is powered on. It is specified as the area of the glitch in nV-sec. See Figure 41 and Figure 58.

### Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 38 and Figure 61.

### Glitch Impulse Peak Amplitude

Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in millivolt and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). See Figure 38 and Figure 61.

### Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.



**Power Supply Rejection Ratio (PSRR)**

PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

**Voltage Reference TC**

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[ \frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:

$V_{REFmax}$  is the maximum reference output measured over the total temperature range.

$V_{REFmin}$  is the minimum reference output measured over the total temperature range.

$V_{REFnom}$  is the nominal reference output voltage, 5 V.

$TempRange$  is the specified temperature range, -40°C to +85°C.

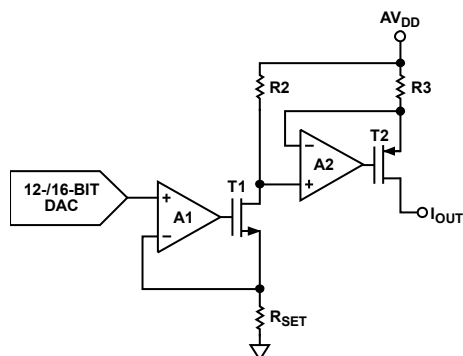
**Load Regulation**

Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

## ARCHITECTURE

8-12 BIT R-2R LADDER      FOUR MSBs DECODED INTO 15 EQUAL SEGMENTS

The voltage output from the DAC core is either converted to a current (see Figure 64) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground or it is buffered and scaled to output a software selectable unipolar or bipolar voltage range (see Figure 65). The current and voltage are output on separate pins and cannot be output simultaneously.



### ***Voltage Output Amplifier***

## Driving Large Capacitive Loads

Rev. C | Page 26 of 40

## SERIAL INTERFACE

The AD5412/AD5422 are controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz. It is compatible with SPI, QSPI™, MICROWIRE, and DSP standards.

### Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the rising edge of SCLK. The input register consists of eight address bits and 16 data bits, as shown in Table 7. The 24-bit word is unconditionally latched on the rising edge of the LATCH pin. Data continues to be clocked in irrespective of the state of LATCH. On the rising edge of LATCH, the data that is present in the input register is latched; in other words, the last 24 bits to be clocked in before the rising edge of LATCH is the data that is latched. The timing diagram for this operation is shown in Figure 2.

**Table 7. Input Shift Register Format**

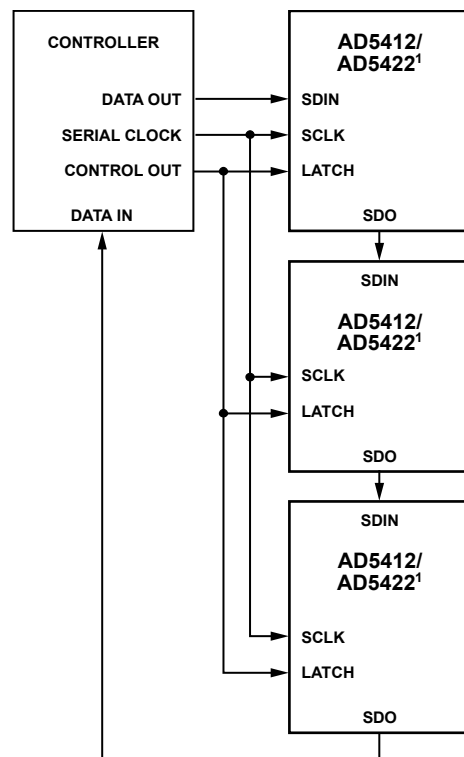
| MSB          | LSB       |
|--------------|-----------|
| D23 to D16   | D15 to D0 |
| Address byte | Data-word |

**Table 8. Address Byte Functions**

| Address Word | Function  |
|--------------|---|
| 00000000     | No operation (NOP)  |
| 00000001     | Data register   |
| 00000010     | Readback register value as per read address (see Table 9) |
| 01010101     | Control register  |
| 01010110     | Reset register  |

### Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can be used only if LATCH is taken high after the correct number of data bits have been clocked in. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. The rising edge of SCLK that clocks in the MSB of the data-word marks the beginning of the write cycle. Exactly 24 rising clock edges must be applied to SCLK before LATCH is brought high. If LATCH is brought high before the 24<sup>th</sup> rising SCLK edge, the data written is invalid. If more than 24 rising SCLK edges are applied before LATCH is brought high, the input data is also invalid.



<sup>1</sup>ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 66. Daisy Chaining the AD5412/AD5422

### Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain the devices together as shown in Figure 66. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. Daisy-chain mode is enabled by setting the DCEN bit of the control register to 1. The first rising edge of SCLK that clocks in the MSB of the data-word marks the beginning of the write cycle. SCLK is continuously applied to the input shift register. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is valid on the rising edge of SCLK, having been clocked out on the previous falling SCLK edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal  $24 \times n$ , where  $n$  is the total number of AD5412/AD5422 devices in the chain. When the serial transfer to all devices is complete, LATCH is taken high. This latches the input data in each device in the daisy chain. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can be used only if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data (see Figure 4 for a timing diagram).

# AD5412/AD5422

## Readback Operation

Readback mode is invoked by setting the address byte and read address when writing to the input register (see Table 9 and Table 11). The next write to the AD5412/AD5422 should be a NOP command, which clocks out the data from the previously addressed register as shown in Figure 3.

By default the SDO pin is disabled after having addressed the AD5412/AD5422 for a read operation; a rising edge on LATCH enables the SDO pin in anticipation of data being clocked out. After the data has been clocked out on SDO, a rising edge on LATCH disables (tristate) the SDO pin. To read back the data register, for example, implement the following sequence:

1. Write 0x020001 to the input register. This configures the part for read mode with the data register selected.
2. Follow this with a second write: a NOP condition, which is 0x000000. During this write, the data from the register is clocked out on the SDO line.

**Table 9. Read Address Decoding**

| Read Address | Function              |
|--------------|-----------------------|
| 00           | Read status register  |
| 01           | Read data register    |
| 10           | Read control register |

## POWER-ON STATE

During power-on of the AD5412/AD5422, the power-on-reset circuit ensures that all registers are loaded with zero-code. As such, both outputs are disabled; that is, the  $V_{OUT}$  and  $I_{OUT}$  pins are in tristate. The  $+V_{SENSE}$  pin is internally connected to ground through a 40 k $\Omega$  resistor. Therefore, if the  $V_{OUT}$  and  $+V_{SENSE}$  pins are connected together,  $V_{OUT}$  is effectively clamped to ground through a 40 k $\Omega$  resistor. Also upon power-on, internal calibration registers are read, and the data is applied to internal calibration circuitry. For a reliable read operation, there must be sufficient voltage on the  $AV_{DD}$  supply when the read event is triggered by the  $DV_{CC}$  power supply powering up. Powering up the  $DV_{CC}$  supply after the  $AV_{DD}$  supply ensures this. If  $DV_{CC}$  and  $AV_{DD}$  are powered up simultaneously or the internal  $DV_{CC}$  is enabled, the supplies should be powered up at a rate greater than, typically, 500 V/sec or 24 V/50 ms. If this cannot be achieved, issue a reset command to the AD5412/AD5422 after power-on; this performs a power-on-reset event, reading the

**Table 11. Input Shift Register Contents for a Read Operation**

| MSB |     |     |     |     |     |     |     | LSB            |              |
|-----|-----|-----|-----|-----|-----|-----|-----|----------------|--------------|
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 to D2      | D1 D0        |
| 0   | 0   | 0   | 0   | 0   | 0   | 1   | 0   | X <sup>1</sup> | Read address |

<sup>1</sup> X = don't care.

calibration registers and ensures specified operation of the AD5412/AD5422.

## Voltage Output

For a unipolar voltage output range, the output voltage can be expressed as

$$V_{OUT} = V_{REFIN} \times Gain \left[ \frac{D}{2^N} \right]$$

For a bipolar voltage output range, the output voltage can be expressed as

$$V_{OUT} = V_{REFIN} \times Gain \left[ \frac{D}{2^N} \right] - \frac{Gain \times V_{REFIN}}{2}$$

where:

$D$  is the decimal equivalent of the code loaded to the DAC.

$N$  is the bit resolution of the DAC.

$V_{REFIN}$  is the reference voltage applied at the REFIN pin.

$Gain$  is an internal gain whose value depends on the output range selected by the user as shown in Table 10.

**Table 10. Internal Gain Value**

| Output Range | Gain Value |
|--------------|------------|
| +5 V         | 1          |
| +10 V        | 2          |
| ±5 V         | 2          |
| ±10 V        | 4          |

## Current Output

For the 0 mA to 20 mA, 0 mA to 24 mA, and 4 mA to 20 mA current output ranges, the output current is respectively expressed as

$$I_{OUT} = \left[ \frac{20 \text{ mA}}{2^N} \right] \times D$$

$$I_{OUT} = \left[ \frac{24 \text{ mA}}{2^N} \right] \times D$$

$$I_{OUT} = \left[ \frac{16 \text{ mA}}{2^N} \right] \times D + 4 \text{ mA}$$

where:

$D$  is the decimal equivalent of the code loaded to the DAC.

$N$  is the bit resolution of the DAC.

## DATA REGISTER

The data register is addressed by setting the address word of the input shift register to 0x01. The data to be written to the data register is entered in the D15 to D4 positions for the AD5412 and the D15 to D0 positions for the AD5422, as shown in Table 12 and Table 13.

**Table 12. Programming the AD5412 Data Register**

| MSB              |     |     |     |     |     |    |    |    |    |    |    | LSB |    |    |    |
|------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|-----|----|----|----|
| D15              | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3  | D2 | D1 | D0 |
| 12-bit data-word |     |     |     |     |     |    |    |    |    |    |    | X   | X  | X  | X  |

**Table 13. Programming the AD5422 Data Register**

| MSB              |     |     |     |     |     |    |    |    |    |    |    |    |    |    | LSB |
|------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|-----|
| D15              | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0  |
| 16-bit data-word |     |     |     |     |     |    |    |    |    |    |    |    |    |    |     |

## CONTROL REGISTER

The control register is addressed by setting the address word of the input shift register to 0x55. The data to be written to the control register is entered in the D15 to D0 positions, as shown in Table 14. The control register functions are shown in Table 15.

**Table 14. Programming the Control Register**

| MSB    |        |      |       |          |     |    |    |         |    |    |      |      |    |    | LSB |  |
|--------|--------|------|-------|----------|-----|----|----|---------|----|----|------|------|----|----|-----|--|
| D15    | D14    | D13  | D12   | D11      | D10 | D9 | D8 | D7      | D6 | D5 | D4   | D3   | D2 | D1 | D0  |  |
| CLRSEL | OVRRNG | REXT | OUTEN | SR clock |     |    |    | SR step |    |    | SREN | DCEN | R2 | R1 | R0  |  |

**Table 15. Control Register Functions**

| Option     | Description  |
|------------|--|
| CLRSEL     | See Table 21 for a description of the CLRSEL operation.  |
| OVRRNG     | Setting this bit increases the voltage output range by 10% (see the AD5412/AD5422 Features section).         |
| REXT       | Setting this bit selects the external current setting resistor (see the AD5412/AD5422 Features section).     |
| OUTEN      | Output enable. This bit must be set to enable the outputs. The range bits select which output is functional. |
| SR clock   | Digital slew rate control (see the AD5412/AD5422 Features section).  |
| SR step    | Digital slew rate control (see the AD5412/AD5422 Features section).  |
| SREN       | Digital slew rate control enable.  |
| DCEN       | Daisy chain enable.  |
| R2, R1, R0 | Output range select (see Table 16).  |

**Table 16. Output Range Options**

| R2 | R1 | R0 | Output Range Selected       |
|----|----|----|-----------------------------|
| 0  | 0  | 0  | 0 V to 5 V voltage range    |
| 0  | 0  | 1  | 0 V to 10 V voltage range   |
| 0  | 1  | 0  | ±5 V voltage range          |
| 0  | 1  | 1  | ±10 V voltage range         |
| 1  | 0  | 1  | 4 mA to 20 mA current range |
| 1  | 1  | 0  | 0 mA to 20 mA current range |
| 1  | 1  | 1  | 0 mA to 24 mA current range |

# AD5412/AD5422

## RESET REGISTER

The reset register is addressed by setting the address word of the input shift register to 0x56. The data to be written to the reset register is entered in the D0 position as shown in Table 17. The reset register options are shown in Table 17 and Table 18.

Table 17. Programming the Reset Register

| MSB      |     |     |     |     |     |    |    |    |    |    |    |    |    | LSB   |    |
|----------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|-------|----|
| D15      | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1    | D0 |
| Reserved |     |     |     |     |     |    |    |    |    |    |    |    |    | Reset |    |

Table 18. Reset Register Functions

| Option | Description   |
|--------|---|
| Reset  | Setting this bit performs a reset operation, restoring the AD5412/AD5422 to its power-on state. |

## STATUS REGISTER

The status register is a read-only register. The status register functionality is shown in Table 19 and Table 20.

Table 19. Decoding the Status Register

| MSB      |     |     |     |     |     |    |    |    |    |    |    |    | LSB                    |             |           |
|----------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|------------------------|-------------|-----------|
| D15      | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2                     | D1          | D0        |
| Reserved |     |     |     |     |     |    |    |    |    |    |    |    | I <sub>OUT</sub> fault | Slew active | Over temp |

Table 20. Status Register Functions

| Option                 | Description  |
|------------------------|--|
| I <sub>OUT</sub> Fault | This bit is set if a fault is detected on the I <sub>OUT</sub> pin.            |
| Slew Active            | This bit is set while the output value is slewing (slew rate control enabled). |
| Over Temp              | This bit is set if the AD5412/AD5422 core temperature exceeds ~150°C.          |

## AD5412/AD5422 FEATURES

### FAULT ALERT

The AD5412/AD5422 are equipped with a  $\overline{\text{FAULT}}$  pin, which is an open-drain output allowing several AD5412/AD5422 devices to be connected together to one pull-up resistor for global fault detection. The  $\overline{\text{FAULT}}$  pin is forced active by one of the following fault scenarios:

- The voltage at  $I_{\text{OUT}}$  attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The  $I_{\text{OUT}}$  current is controlled by a PMOS transistor and internal amplifier, as shown in Figure 64. The internal circuitry that develops the fault output avoids using a comparator with window limits because this would require an actual output error before the  $\overline{\text{FAULT}}$  output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than  $\sim 1$  V of remaining drive capability (when the gate of the output PMOS transistor nearly reaches ground). Thus, the  $\overline{\text{FAULT}}$  output activates slightly before the compliance limit is reached. Because the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain, and an output error does not occur before the  $\overline{\text{FAULT}}$  output becomes active.
- If the core temperature of the AD5412/AD5422 exceeds approximately  $150^{\circ}\text{C}$ .

The  $I_{\text{OUT}}$  fault and over temp bits of the status register are used in conjunction with the  $\overline{\text{FAULT}}$  pin to inform the user which one of the fault conditions caused the  $\overline{\text{FAULT}}$  pin to be asserted (see Table 19 and Table 20).

### VOLTAGE OUTPUT SHORT CIRCUIT PROTECTION

Under normal operation, the voltage output sinks/sources 10 mA. The maximum current that the voltage output delivers is  $\sim 20$  mA; this is the short-circuit current.

### VOLTAGE OUTPUT OVERRANGE

An overrange facility is provided on the voltage output. When enabled via the control register, the selected output range is overranged by, typically, 10%.

### VOLTAGE OUTPUT FORCE-SENSE

The  $+V_{\text{SENSE}}$  and  $-V_{\text{SENSE}}$  pins are provided to facilitate remote sensing of the load connected to the voltage output. If the load is connected at the end of a long or high impedance cable, sensing the voltage at the load allows the output amplifier to compensate and ensure that the correct voltage is applied across the load. This function is limited only by the available power supply headroom.

### ASYNCHRONOUS CLEAR (CLEAR)

The CLEAR pin is an active high clear that allows the voltage output to be cleared to either zero-scale code or midscale code, user selectable via the CLEAR SELECT pin, or the CLRSEL bit of the control register, as described in Table 21. (The clear select feature is a logical OR function of the CLEAR SELECT pin and the CLRSEL bit.) The current output clears to the bottom of its programmed range. It is necessary for CLEAR to be high for a minimum amount of time to complete the operation (see Figure 2). When the CLEAR signal is returned low, the output remains at the cleared value. The preclear value can be restored by pulsing the LATCH signal low without clocking any data. A new value cannot be programmed until the CLEAR pin is returned low.

Table 21. CLRSEL Options

| CLRSEL | Output Value          |                      |
|--------|-----------------------|----------------------|
|        | Unipolar Output Range | Bipolar Output Range |
| 0      | 0 V                   | 0 V                  |
| 1      | Midscale              | Negative full scale  |

In addition to defining the output value for a clear operation, the CLRSEL bit and CLEAR SELECT pin also define the default output value. During selection of a new voltage range, the output value is as defined in Table 21. To avoid glitches on the output, it is recommended that, before changing voltage ranges, the user disable the output by setting the OUTEN bit of the control register to logic low. When OUTEN is set to logic high, the output goes to the default value as defined by CLRSEL and CLEAR SELECT.

### INTERNAL REFERENCE

The AD5412/AD5422 contain an integrated 5 V voltage reference with initial accuracy of  $\pm 5$  mV maximum and a temperature drift coefficient of  $\pm 10$  ppm/ $^{\circ}\text{C}$  maximum. The reference voltage is buffered and externally available for use elsewhere within the system. See Figure 16 for a load regulation graph of the integrated reference.

### EXTERNAL CURRENT SETTING RESISTOR

$R_{\text{SET}}$  is an internal sense resistor as part of the voltage-to-current conversion circuitry (see Figure 64). The stability of the output current over temperature is dependent on the stability of the value of  $R_{\text{SET}}$ . As a method of improving the stability of the output current over temperature, an external precision 15 k $\Omega$  low drift resistor can be connected to the  $R_{\text{SET}}$  pin of the AD5412/AD5422 to be used instead of the internal resistor ( $R_{\text{SET}}$ ). The external resistor is selected via the control register (see Table 14).

# AD5412/AD5422

## DIGITAL POWER SUPPLY

By default, the DV<sub>CC</sub> pin accepts a power supply of 2.7 V to 5.5 V. Alternatively, via the DV<sub>CC</sub> SELECT pin, an internal 4.5 V power supply can be output on the DV<sub>CC</sub> pin for use as a digital power supply for other devices in the system or as a termination for pull-up resistors. This facility offers the advantage of not having to bring a digital supply across an isolation barrier. The internal power supply is enabled by leaving the DV<sub>CC</sub> SELECT pin unconnected. To disable the internal supply, tie DV<sub>CC</sub> SELECT to 0 V. DV<sub>CC</sub> is capable of supplying up to 5 mA of current (for a load regulation graph, see Figure 10).

## EXTERNAL BOOST FUNCTION

The addition of an external boost transistor, as shown in Figure 67, reduces the power dissipated in the AD5412/AD5422 by reducing the current flowing in the on-chip output transistor (dividing it by the current gain of the external circuit). A discrete NPN transistor with a breakdown voltage, BV<sub>CEO</sub>, greater than 40 V can be used. The external boost capability has been developed for users who may wish to use the AD5412/AD5422 at the extremes of the supply voltage, load current, and temperature range. The boost transistor can also be used to reduce the amount of temperature-induced drift in the part. This minimizes the temperature-induced drift of the on-chip voltage reference, which improves on drift and linearity.

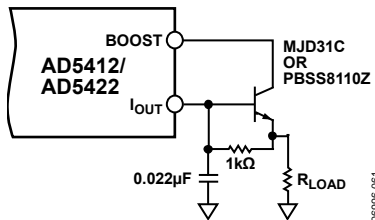


Figure 67. External Boost Configuration

## EXTERNAL COMPENSATION CAPACITOR

The voltage output can ordinarily drive capacitive loads of up to 20 nF; if there is a requirement to drive greater capacitive loads, of up to 1 µF, an external compensation capacitor can be connected between the C<sub>COMP</sub> and V<sub>OUT</sub> pins. The addition of the capacitor keeps the output voltage stable but also reduces the bandwidth and increases the settling time of the voltage output.

## DIGITAL SLEW RATE CONTROL

The slew rate control feature of the AD5412/AD5422 allows the user to control the rate at which the output voltage or current changes. With the slew rate control feature disabled, the output changes at a rate limited by the output drive circuitry and the attached load. See Figure 62 for current output step and Figure 36 for voltage output step. To reduce the slew rate, enable the slew rate control feature. With the feature enabled via the SREN bit of the control register (see Table 14), the output, instead of slewing directly between two values, steps digitally at a rate defined by two parameters accessible via the control register, as shown in Table 14. The parameters are set by the SR clock and

SR step bits. SR clock defines the rate at which the digital slew is updated; SR step defines by how much the output value changes at each update. Both parameters together define the rate of change of the output voltage or current. Table 22 and Table 23 outline the range of values for both the SR clock and SR step parameters. Figure 68 shows the output current changing for ramp times of 10 ms, 50 ms, and 100 ms.

Table 22. Slew Rate Step Size Options

| SR Step | AD5412 Step Size (LSB) | AD5422 Step Size (LSB) |
|---------|------------------------|------------------------|
| 000     | 1/16                   | 1                      |
| 001     | 1/8                    | 2                      |
| 010     | 1/4                    | 4                      |
| 011     | 1/2                    | 8                      |
| 100     | 1                      | 16                     |
| 101     | 2                      | 32                     |
| 110     | 4                      | 64                     |
| 111     | 8                      | 128                    |

Table 23. Slew Rate Update Clock Options

| SR Clock | Update Clock Frequency (Hz) |
|----------|-----------------------------|
| 0000     | 257,730                     |
| 0001     | 198,410                     |
| 0010     | 152,440                     |
| 0011     | 131,580                     |
| 0100     | 115,740                     |
| 0101     | 69,440                      |
| 0110     | 37,590                      |
| 0111     | 25,770                      |
| 1000     | 20,160                      |
| 1001     | 16,030                      |
| 1010     | 10,290                      |
| 1011     | 8280                        |
| 1100     | 6900                        |
| 1101     | 5530                        |
| 1110     | 4240                        |
| 1111     | 3300                        |

The time it takes for the output to slew over a given output range can be expressed as follows:

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size} \times \text{Update Clock Frequency} \times \text{LSB Size}} \quad (1)$$

where:

Slew Time is expressed in seconds.

Output Change is expressed in amps for I<sub>OUT</sub> or volts for V<sub>OUT</sub>.

When the slew rate control feature is enabled, all output changes change at the programmed slew rate; if the CLEAR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. The output can be halted at its current value with a write to the control register. To avoid halting the output slew, the slew active bit (see Table 19) can be read to check that the slew has completed before writing to any of the



AD5410/AD5420 registers. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. Table 24 shows the range of programmable slew times for a full-scale change on any of the output ranges. The values in Table 24 were obtained using Equation 1.

The digital slew rate control feature results in a staircase formation on the current output, as shown in Figure 72. This figure also shows how the staircase can be removed by connecting capacitors to the CAP1 and CAP2 pins, as described in the  $I_{OUT}$  Filtering Capacitors (LFCSP Package) section.

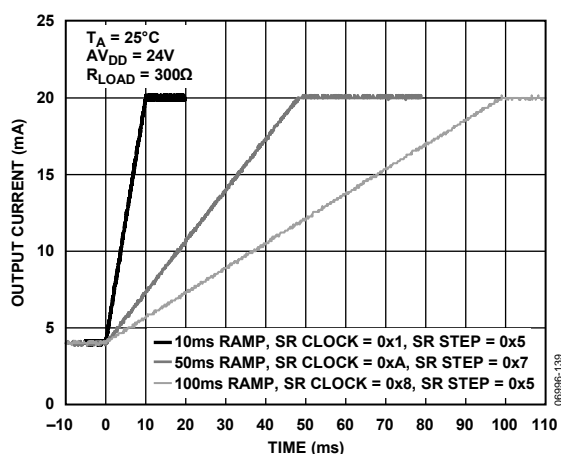


Figure 68. Output Current Slew Rate Under Control of the Digital Slew Rate Control Feature

### $I_{OUT}$ FILTERING CAPACITORS (LFCSP PACKAGE)

Capacitors can be placed between CAP1 and  $AV_{DD}$ , and CAP2 and  $AV_{DD}$ , as shown in Figure 69.

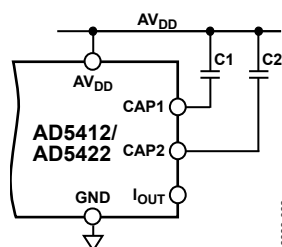


Figure 69.  $I_{OUT}$  Filtering Capacitors

The CAP1 and CAP2 pins are available only on the LFCSP package. The capacitors form a filter on the current output circuitry, as shown in Figure 70, reducing the bandwidth and the slew rate of the output current. Figure 71 shows the effect the capacitors have on the slew rate of the output current. To achieve significant reductions in the rate of change, very large capacitor values are required, which may not be suitable in some applications. In this case, the digital slew rate control

feature can be used. The capacitors can be used in conjunction with the digital slew rate control feature as a means of smoothing out the steps caused by the digital code increments, as shown in Figure 72.

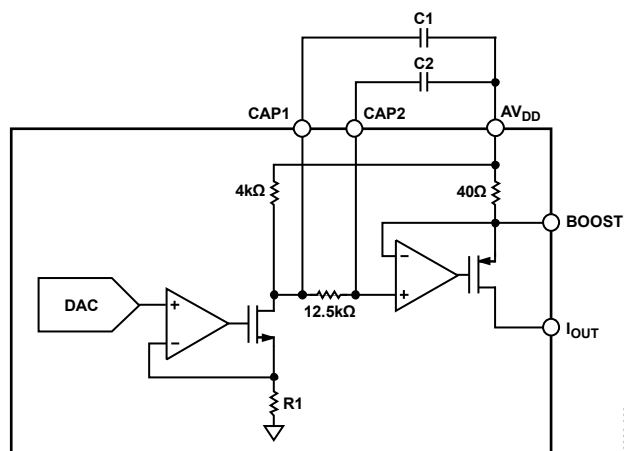


Figure 70.  $I_{OUT}$  Filter Circuitry

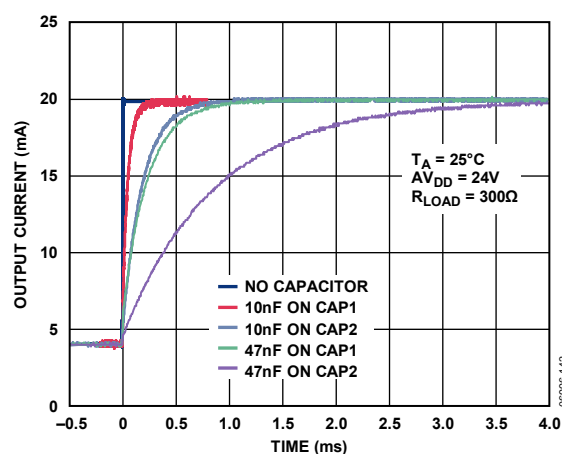


Figure 71. Slew Controlled 4 mA to 20 mA Output Current Step Using External Capacitors on the CAP1 and CAP2 Pins

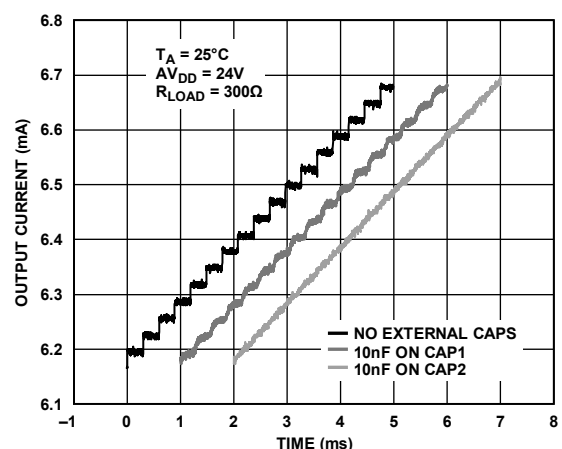


Figure 72. Smoothing Out the Steps Caused by the Digital Slew Rate Control Feature

# AD5412/AD5422

Table 24. Programmable Slew Time Values in Seconds for a Full-Scale Change on Any Output Range

| Update Clock<br>Frequency (Hz) | Step Size (LSB) |      |      |      |       |       |       |        |
|--------------------------------|-----------------|------|------|------|-------|-------|-------|--------|
|                                | 1               | 2    | 4    | 8    | 16    | 32    | 64    | 128    |
| 257,730                        | 0.25            | 0.13 | 0.06 | 0.03 | 0.016 | 0.008 | 0.004 | 0.0020 |
| 198,410                        | 0.33            | 0.17 | 0.08 | 0.04 | 0.021 | 0.010 | 0.005 | 0.0026 |
| 152,440                        | 0.43            | 0.21 | 0.11 | 0.05 | 0.027 | 0.013 | 0.007 | 0.0034 |
| 131,580                        | 0.50            | 0.25 | 0.12 | 0.06 | 0.031 | 0.016 | 0.008 | 0.0039 |
| 115,740                        | 0.57            | 0.28 | 0.14 | 0.07 | 0.035 | 0.018 | 0.009 | 0.0044 |
| 69,440                         | 0.9             | 0.47 | 0.24 | 0.12 | 0.06  | 0.03  | 0.015 | 0.007  |
| 37,590                         | 1.7             | 0.87 | 0.44 | 0.22 | 0.11  | 0.05  | 0.03  | 0.014  |
| 25,770                         | 2.5             | 1.3  | 0.64 | 0.32 | 0.16  | 0.08  | 0.04  | 0.020  |
| 20,160                         | 3.3             | 1.6  | 0.81 | 0.41 | 0.20  | 0.10  | 0.05  | 0.025  |
| 16,030                         | 4.1             | 2.0  | 1.0  | 0.51 | 0.26  | 0.13  | 0.06  | 0.03   |
| 10,290                         | 6.4             | 3.2  | 1.6  | 0.80 | 0.40  | 0.20  | 0.10  | 0.05   |
| 8280                           | 7.9             | 4.0  | 2.0  | 1.0  | 0.49  | 0.25  | 0.12  | 0.06   |
| 6900                           | 9.5             | 4.8  | 2.4  | 1.2  | 0.59  | 0.30  | 0.15  | 0.07   |
| 5530                           | 12              | 5.9  | 3.0  | 1.5  | 0.74  | 0.37  | 0.19  | 0.09   |
| 4240                           | 15              | 7.7  | 3.9  | 1.9  | 0.97  | 0.48  | 0.24  | 0.12   |
| 3300                           | 20              | 9.9  | 5.0  | 2.5  | 1.24  | 0.62  | 0.31  | 0.16   |

## APPLICATIONS INFORMATION

### DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, connect a  $0.01\ \mu\text{F}$  capacitor between  $\text{I}_{\text{OUT}}$  and GND. This ensures stability with loads above  $50\ \text{mH}$ . There is no maximum capacitance limit. The capacitive component of the load may cause slower settling. The digital slew rate control feature may also prove useful in this situation.

### TRANSIENT VOLTAGE PROTECTION

The AD5412/AD5422 contain ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5412/AD5422 from excessively high voltage transients, external power diodes and a surge current limiting resistor are required, as shown in Figure 73. The constraint on the resistor value is that, during normal operation, the output level at  $\text{I}_{\text{OUT}}$  must remain within its voltage compliance limit of  $\text{AV}_{\text{DD}} - 2.5\ \text{V}$ , and the two protection diodes and resistor must have appropriate power ratings. Further protection can be provided with transient voltage suppressors or transorbs; these are available as both unidirectional suppressors (protect against positive high voltage transients) and bidirectional suppressors (protect against both positive and negative high voltage transients) and are available in a wide range of standoff and breakdown voltage ratings. It is recommended that all field connected nodes be protected.

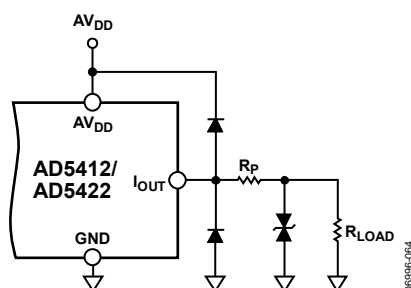
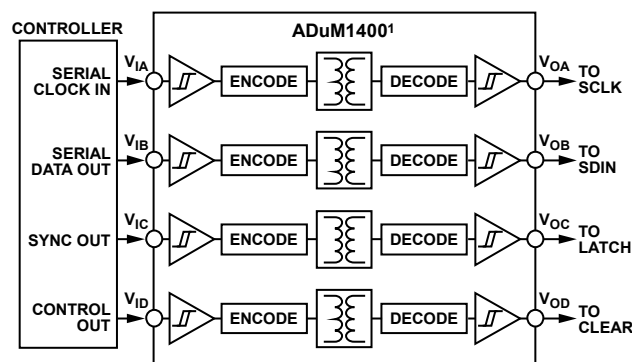


Figure 73. Output Transient Voltage Protection

### GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. The iCoupler® products from Analog Devices, Inc., provide voltage isolation in excess of  $2.5\ \text{kV}$ . The serial loading structure of the AD5412/AD5422 makes the parts ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 74 shows a 4-channel isolated interface to the AD5412/AD5422 using an ADuM1400. For further information, visit <http://www.analog.com/icouplers>.



<sup>1</sup>ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 74. Isolated Interface

### MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5412/AD5422 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5412/AD5422 require a 24-bit data-word with data valid on the rising edge of SCLK.

For all interfaces, the DAC output update is initiated on the rising edge of LATCH. The contents of the registers can be read using the readback function.

### LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the printed circuit board (PCB) on which the AD5412/AD5422 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5412/AD5422 is in a system where multiple devices require an analog ground-to-digital ground connection, make the connection at one point only. Establish the star ground point as close as possible to the device.

The AD5412/AD5422 should have ample supply bypassing of  $10\ \mu\text{F}$  in parallel with  $0.1\ \mu\text{F}$  on each supply located as close to the package as possible, ideally right up against the device. The  $10\ \mu\text{F}$  capacitors are the tantalum bead type. The  $0.1\ \mu\text{F}$  capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

## AD5412/AD5422

The power supply lines of the AD5412/AD5422 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with a digital ground to avoid radiating noise to other parts of the board. Never run these near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (this is not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the PCB should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane, and signal traces are placed on the solder side.

### THERMAL AND SUPPLY CONSIDERATIONS

The AD5412/AD5422 are designed to operate at a maximum junction temperature of 125°C. It is important that the devices not be operated under conditions that cause the junction temperature to exceed this value. Excessive junction temperature can occur if the AD5412/AD5422 are operated from the maximum  $AV_{DD}$  while driving the maximum current (24 mA) directly to ground. In this case, control the ambient temperature or reduce  $AV_{DD}$ . The conditions depend on the device package.

At the maximum ambient temperature of 85°C, the 24-lead TSSOP package can dissipate 950 mW, and the 40-lead LFCSP package can dissipate 1.42 W.

To ensure that the junction temperature does not exceed 125°C while driving the maximum current of 24 mA directly into ground (also adding an on-chip current of 3 mA), reduce  $AV_{DD}$  from the maximum rating to ensure that the package is not required to dissipate more power than previously stated (see Table 25, Figure 75, and Figure 76).

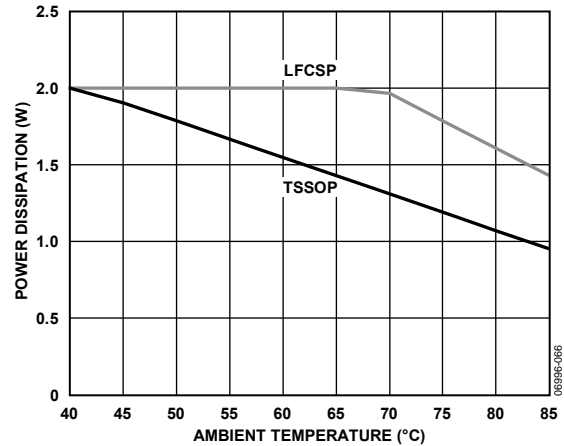


Figure 75. Maximum Power Dissipation vs. Ambient Temperature

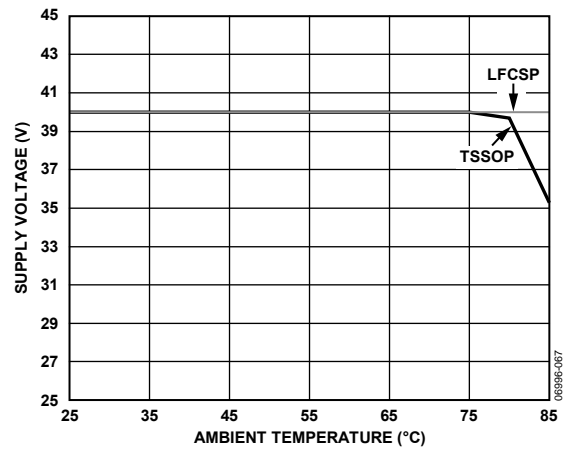


Figure 76. Maximum Supply Voltage vs. Ambient Temperature

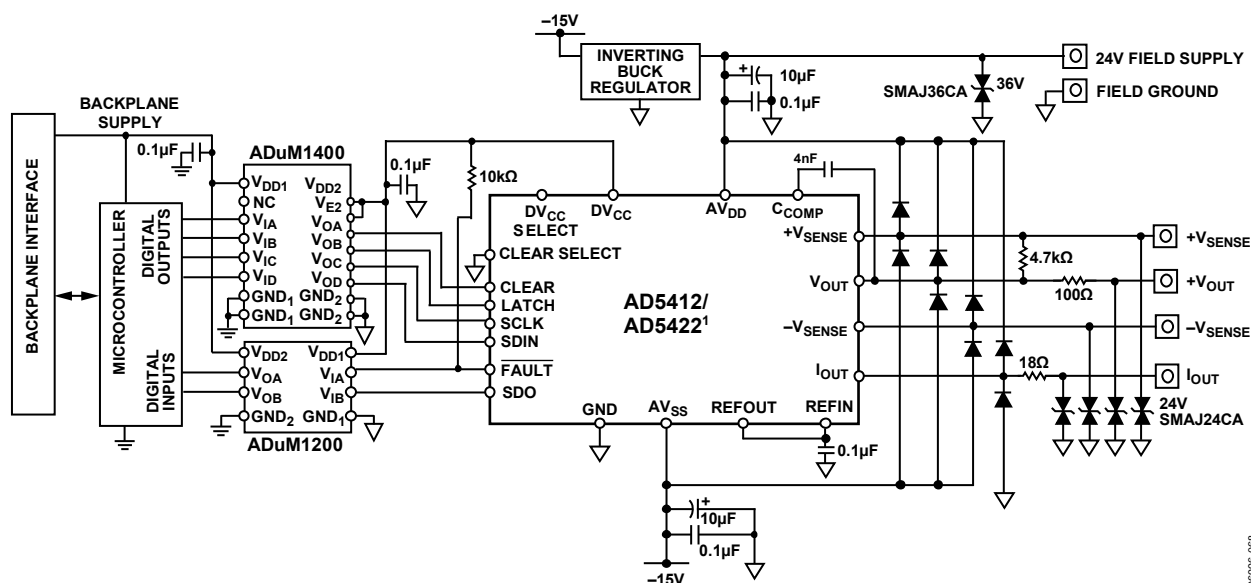
Table 25. Thermal and Supply Considerations for Each Package

| Considerations   | TSSOP  | LFCSP  |
|--|--|--|
| Maximum Allowed Power Dissipation When Operating at an Ambient Temperature of 85°C                                   | $\frac{T_J \text{ max} - T_A}{\theta_{JA}} = \frac{125 - 85}{42} = 950 \text{ mW}$                           | $\frac{T_J \text{ max} - T_A}{\theta_{JA}} = \frac{125 - 85}{28} = 1.42 \text{ W}$                           |
| Maximum Allowed Ambient Temperature When Operating from a Supply of 40 V and Driving 24 mA Directly to Ground        | $T_J \text{ max} - P_D \times \theta_{JA} = 125 - (40 \times 0.028) \times 42 = 78^\circ\text{C}$            | $T_J \text{ max} - P_D \times \theta_{JA} = 125 - (40 \times 0.028) \times 28 = 94^\circ\text{C}$            |
| Maximum Allowed Supply Voltage When Operating at an Ambient Temperature of 85°C and Driving 24 mA Directly to Ground | $\frac{T_J \text{ max} - T_A}{AI_{DD} \times \theta_{JA}} = \frac{125 - 85}{0.028 \times 42} = 34 \text{ V}$ | $\frac{T_J \text{ max} - T_A}{AI_{DD} \times \theta_{JA}} = \frac{125 - 85}{0.028 \times 28} = 51 \text{ V}$ |

## INDUSTRIAL ANALOG OUTPUT MODULE

Many industrial control applications have requirements for accurately controlled current and voltage output signals. The AD5412/AD5422 are ideal for such applications. Figure 77 shows the AD5412/AD5422 in a circuit design for an output module, specifically for use in an industrial control application. The design provides for a current or voltage output. The module is powered from a field supply of 24 V. This supplies  $AV_{DD}$  directly. An inverting buck regulator generates the negative supply for  $AV_{SS}$ . For transient overvoltage protection, transient voltage suppressors (TVS) are placed on all field accessible connections. A 24 V volt TVS is placed on each  $I_{OUT}$ ,  $V_{OUT}$ ,  $+V_{SENSE}$ , and  $-V_{SENSE}$  connection, and a 36 V TVS is placed on the field supply input. For added protection, clamping diodes are connected from the  $I_{OUT}$ ,  $V_{OUT}$ ,  $+V_{SENSE}$ , and  $-V_{SENSE}$  pins to the  $AV_{DD}$  and  $AV_{SS}$  power supply pins. If remote voltage load sensing is not required, the  $+V_{SENSE}$  pin can be directly connected to the  $V_{OUT}$  pin and the  $-V_{SENSE}$  pin can be connected to GND.

Isolation between the AD5412/AD5422 and the backplane circuitry is provided with ADuM1400 and ADuM1200 iCoupler digital isolators; further information on iCoupler products is available at [www.analog.com/icouplers](http://www.analog.com/icouplers). The internally generated digital power supply of the AD5412/AD5422 powers the field side of the digital isolators, removing the need to generate a digital power supply on the field side of the isolation barrier. The AD5412/AD5422 digital supply output supplies up to 5 mA, which is more than enough to supply the 2.8 mA requirements of the ADuM1400 and ADuM1200 operating at a logic signal frequency of up to 1 MHz. To reduce the number of isolators required, nonessential signals such as CLEAR can be connected to GND. FAULT and SDO can be left unconnected, reducing the isolation requirements to just three signals.



<sup>1</sup>ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 77. AD5412/AD5422 in an Industrial Analog Output Module Application

## OUTLINE DIMENSIONS

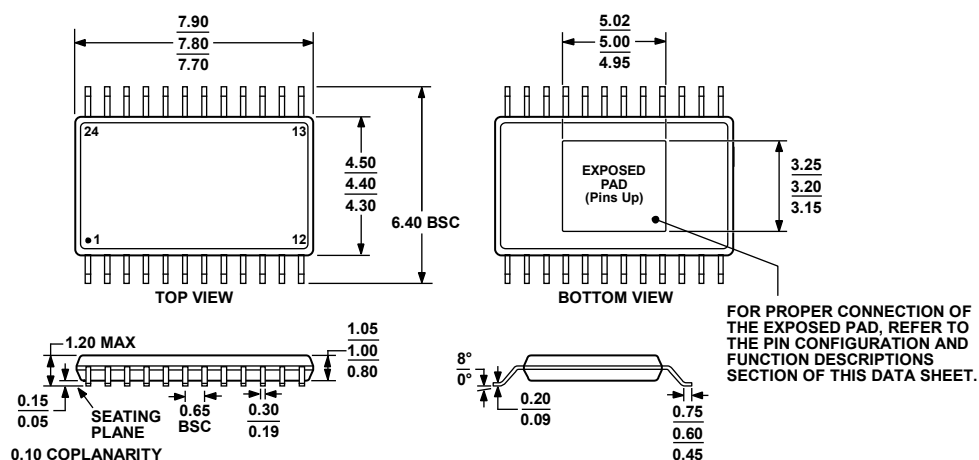


Figure 78. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP\_EP]  
(RE-24)  
Dimensions shown in millimeters

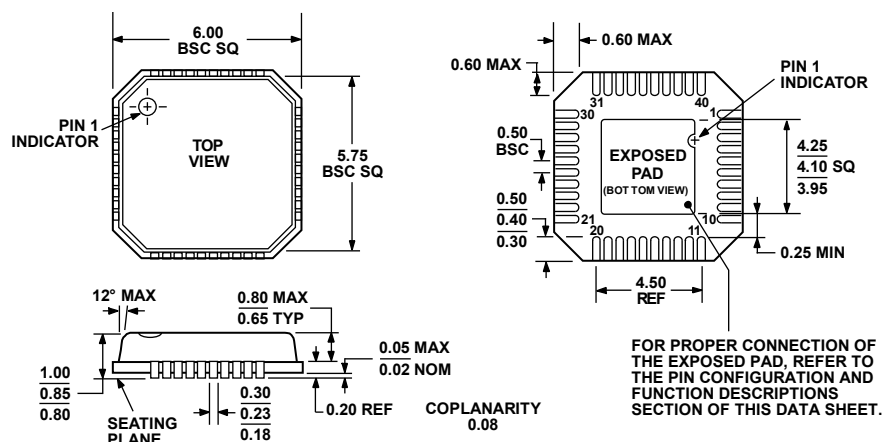


Figure 79. 40-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
6 mm × 6 mm Body, Very Thin Quad  
(CP-40-1)  
Dimensions shown in millimeters

**ORDERING GUIDE**

| Model <sup>1</sup> | Resolution | I <sub>OUT</sub> TUE | V <sub>OUT</sub> TUE | Temperature Range | Package Description | Package Option |
|--------------------|------------|----------------------|----------------------|-------------------|---------------------|----------------|
| AD5412AREZ         | 12 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 24 Lead TSSOP_EP    | RE-24          |
| AD5412AREZ-REEL7   | 12 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 24 Lead TSSOP_EP    | RE-24          |
| AD5412ACPZ-REEL    | 12 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 40 Lead LFCSP_VQ    | CP-40-1        |
| AD5412ACPZ-REEL7   | 12 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 40 Lead LFCSP_VQ    | CP-40-1        |
| AD5422AREZ         | 16 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 24 Lead TSSOP_EP    | RE-24          |
| AD5422AREZ-REEL    | 16 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 24 Lead TSSOP_EP    | RE-24          |
| AD5422BREZ         | 16 Bits    | 0.3% FSR max         | 0.1% FSR max         | −40°C to +85°C    | 24 Lead TSSOP_EP    | RE-24          |
| AD5422BREZ-REEL    | 16 Bits    | 0.3% FSR max         | 0.1% FSR max         | −40°C to +85°C    | 24 Lead TSSOP_EP    | RE-24          |
| AD5422ACPZ-REEL    | 16 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 40 Lead LFCSP_VQ    | CP-40-1        |
| AD5422ACPZ-REEL7   | 16 Bits    | 0.5% FSR max         | 0.3% FSR max         | −40°C to +85°C    | 40 Lead LFCSP_VQ    | CP-40-1        |
| AD5422BCPZ-REEL    | 16 Bits    | 0.3% FSR max         | 0.1% FSR max         | −40°C to +85°C    | 40 Lead LFCSP_VQ    | CP-40-1        |
| AD5422BCPZ-REEL7   | 16 Bits    | 0.3% FSR max         | 0.1% FSR max         | −40°C to +85°C    | 40 Lead LFCSP_VQ    | CP-40-1        |
| EVAL-AD5422EBZ     |            |                      |                      |                   | Evaluation Board    |                |

<sup>1</sup> Z = RoHS Compliant Part.

## **NOTES**