



CV210-3A

Cellular-band Dual-Branch Downconverter

The Communications Edge™

Product Information

Product Features

- High dynamic range downconverter with integrated LO and IF amplifiers
- Dual channels for diversity
- +29 dBm Input IP3
- +10 dBm Input P1dB
- RF: 800 – 960 MHz
- IF: 200 – 350 MHz
- +5V Single supply operation
- Pb-free 6mm 28-pin QFN package
- High-side LO configuration
- Common footprint with other PCS/UMTS/cellular versions

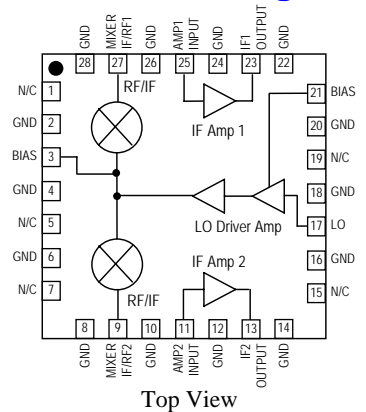
Product Description

The CV210-3A is a dual-channel high-linearity downconverter designed to meet the demanding performance, functionality, and cost goals of current and next generation mobile infrastructure basestations. It provides high dynamic range performance in a low profile lead-free/RoHS-compliant surface-mount leadless package that measures 6x6 mm square.

It is ideally suited for high dynamic range receiver front ends using diversity receive channels. Functionality includes frequency conversion and IF amplification, while an integrated LO driver amplifier powers the passive mixer. The MCM is implemented with reliable and mature GaAs MESFET and InGaP HBT technology.

Typical applications include frequency downconversion used in CDMA/GSM/TDMA, CDMA2000, W-CDMA, and EDGE 2.5G and 3G mobile base transceiver stations.

Functional Diagram



Specifications ⁽¹⁾

| Parameters | Units | Min | Typ | Max | Comments |
|--|--------|------|-------------|------|-------------------------|
| RF Frequency Range | MHz | | 800 – 960 | | |
| LO Frequency Range | MHz | | 1000 – 1310 | | |
| IF Center Frequency Range | MHz | | 200 – 350 | | See note 2 |
| % Bandwidth around IF center frequency | % | | ±7.5 | | See note 3 |
| IF Test Frequency | MHz | | 240 | | |
| SSB Conversion Gain | dB | 8 | 10.3 | 12 | Temp = 25° C |
| Gain Drift over Temp (-40° C to 85° C) | dB | -1.5 | ±0.3 | 1.5 | Referenced to +25° C |
| Input IP3 | dBm | +25 | +29 | | See note 4 |
| Input IP2 | dBm | +33 | +40 | | See note 4 |
| Input 1 dB Compression Point | dBm | | +10 | | See note 4 |
| Noise Figure | dB | | 10.3 | | See note 5 |
| LO Input Drive Level | dBm | -2.5 | 0 | +2.5 | |
| LO-RF Isolation | dB | | 14 | | P _{LO} = 0 dBm |
| LO-IF Isolation | dB | | 34 | | P _{LO} = 0 dBm |
| Branch-Branch Isolation | dB | | 60 | | |
| Return Loss: RF Port | dB | | 17 | | |
| Return Loss: LO Port | dB | | 14 | | |
| Return Loss: IF Port | dB | | 12 | | |
| Operating Supply Voltage | V | | +5 | | |
| Supply Current | mA | 320 | 390 | 475 | |
| Thermal Resistance | °C / W | | | 27 | |
| Junction Temperature | °C | | | 160 | See note 6 |

1. Specifications when using the application specific circuit (shown on page 3) with a low side LO = 0 dBm and IF = 240 MHz in a downconverting application at 25° C.
2. IF matching components affect the center IF frequency. Proper component values for other IF center frequencies than shown can be provided by emailing to applications.engineering@wj.com.
3. The IF bandwidth of the converter is defined as 15% around any center frequency in its operating IF frequency range. The bandwidth is determined with external components. Specifications are valid around the total ±7.5% bandwidth. i.e. with a center frequency of 240 MHz, the specifications are valid from 240 ± 18 MHz.
4. Assumes the supply voltage = +5 V. IIP3 is measured with Δf = 1 MHz with RF_{in} = -5 dBm / tone.
5. Assumes LO injection noise is filtered at the thermal noise floor, -174 dBm/Hz, at the RF, IF, and Image frequencies.
6. The maximum junction temperature ensures a minimum MTTF rating of 1 million hours of usage.

Absolute Maximum Rating

| Parameter | Rating |
|----------------------------|-----------------|
| Operating Case Temperature | -40° to +85° C |
| Storage Temperature | -55° to +150° C |
| DC Voltage | +5.5 V |
| Junction Temperature | +220 °C |

Ordering Information

| Part No. | Description |
|----------------|---|
| CV210-3AF | Cellular-band Dual-Branch Downconverter (lead-free/RoHS-compliant 6x6mm QFN package) |
| CV210-3APCB240 | Fully-Assembled Application Board, IF = 240MHz |

Operation of this device above any of these parameters may cause permanent damage.

Specifications and information are subject to change without notice



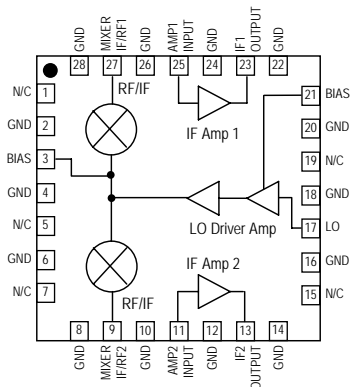
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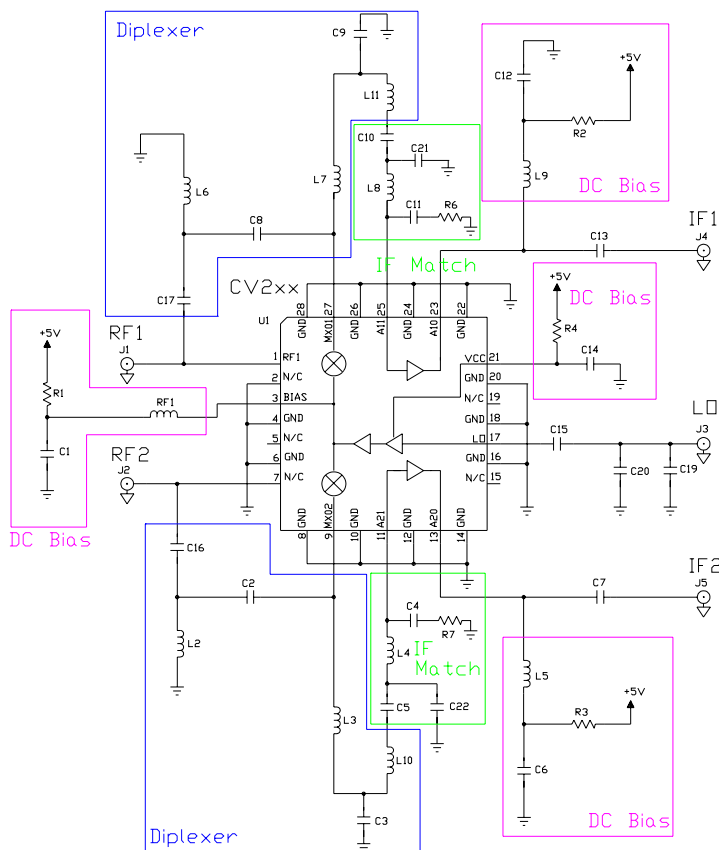
Device Architecture / Application Circuit Information



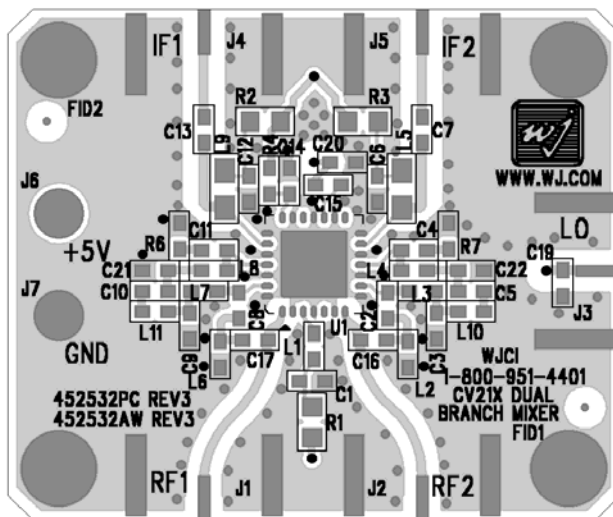
Typical Downconverter Performance Chain Analysis (Each Branch)

| Stage | Gain (dB) | Input P1dB (dBm) | Input IP3 (dBm) | NF (dB) | Current (mA) | Cumulative Performance | | | |
|---------------------|-------------------------------|------------------|-----------------|---------|--------------|------------------------|------------------|-----------------|-------------|
| | | | | | | Gain (dB) | Input P1dB (dBm) | Input IP3 (dBm) | NF (dB) |
| LO Amp / MMIC Mixer | -8.0 | 17.0 | 32.6 | 8.3 | 90 | -8.0 | 17.0 | 32.6 | 8.3 |
| IF Amplifier | 18.3 | 3.0 | 23.5 | 2.1 | 150 | 10.3 | 10.0 | 29.0 | 10.3 |
| CV210-3A | Cumulative Performance | | | | 390* | 10.3 | +10.0 | +29.0 | 10.3 |

* The 2nd branch includes another mixer and IF amplifier, which increases the total current consumption of the MCM to be 390 mA.



Printed Circuit Board Material:
.014" FR-4, 4 layers, .062" total thickness



CV210-3A: The application circuit can be broken up into three main functions as denoted in the colored dotted areas above: RF/IF duplexing (blue), IF amplifier matching (green), and dc biasing (purple). There are various placeholders for chip components in the circuit schematic so that a common PCB can be used for all WJ dual-branch converters. Further details are given in the Application Note located on the website titled "CV2xx Series - PWB Design Guidelines".

External Diplexer: In a downconversion application, the incoming RF signal impinges on the switching elements of the mixer; the interaction with these switches produces a signal at the IF frequency. The two signals (RF and IF) are directed to the appropriate ports by the external diplexer. A four-element diplexer is used in the circuit implementation.

IF Amplifier Matching: The IF amplifier requires matching elements to optimize the performance of the amplifier to the desired IF center frequency. Since IF bandwidths are typically on the order of 5 to 10%, a simple two element matching network, in the form of either a high-pass or low-pass filter structure, is sufficient to match the MMIC IF amplifier over these narrow bandwidths. Proper component values for other IF center frequencies can be provided by emailing to applications.engineering@wj.com.

DC biasing: DC bias must be provided for the LO and IF amplifiers in the converter. R1 sets the operating current for the last stage of the LO amplifier and is chosen to optimize the mixer LO drive level. Proper RF chokes and bypass capacitors are chosen for proper amplifier biasing at the intended frequency of operation. The "+5 V" dc bias should be supplied directly from a voltage regulator.

Specifications and information are subject to change without notice



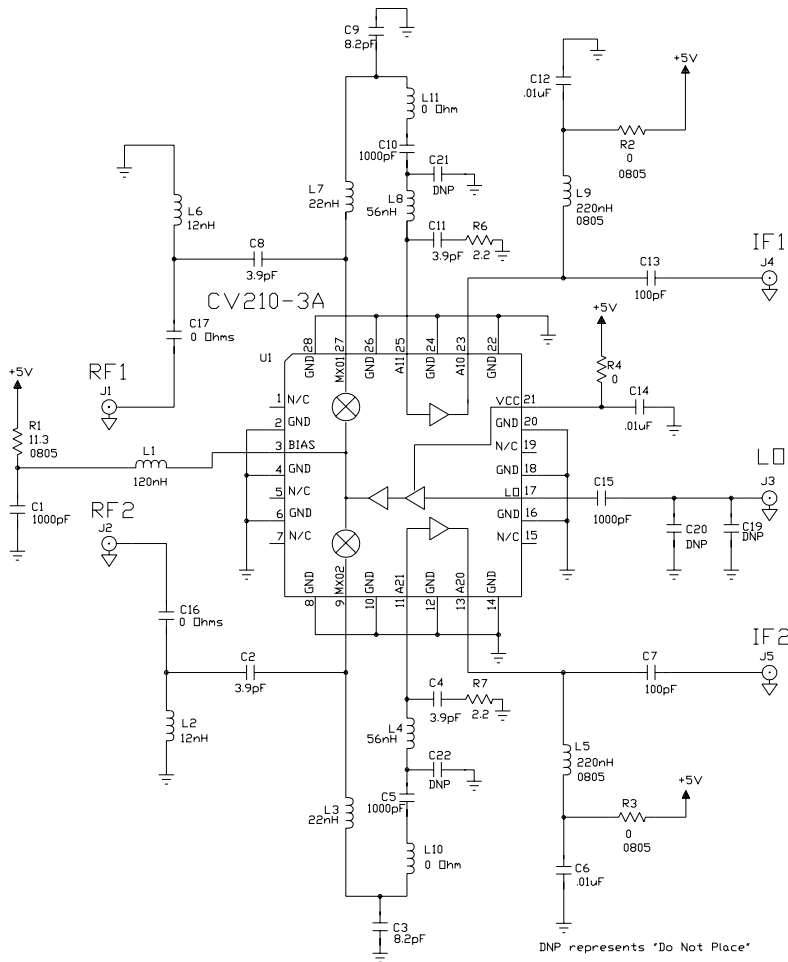
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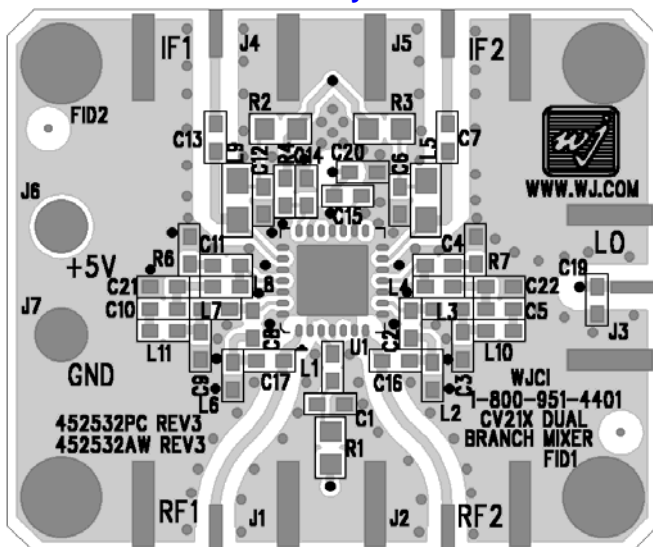
Application Circuit: IF = 240 MHz (CV210-3APCB240)



Bill of Materials

| Ref. Desig. | Component | Size |
|--------------------|------------------------|------|
| R1 | 11.3 Ω chip resistor | 0805 |
| R2, R3, R4, C16 | 0 Ω chip resistor | 0603 |
| C17, L10, L11 | 2.2 Ω chip resistor | 0603 |
| R6, R7 | 2.2 Ω chip resistor | 0603 |
| C1, C5, C10, C15 | 1000 pF chip capacitor | 0603 |
| C2, C4, C8, C11 | 3.9 pF chip capacitor | 0603 |
| C3, C9 | 8.2 pF chip capacitor | 0603 |
| C6, C12, C14 | .01 μF chip capacitor | 0603 |
| C7, C13 | 100 pF chip capacitor | 0603 |
| L1 | 120 nH chip inductor | 0603 |
| L2, L6 | 12 nH chip inductor | 0603 |
| L3, L7 | 22 nH chip inductor | 0603 |
| L4, L8 | 56 nH chip inductor | 0603 |
| L5, L9 | 220 nH chip inductor | 0805 |
| C19, C20, C21, C22 | Do Not Place | |
| U1 | CV210-3A WJ Converter | QFN |

PCB Layout



Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

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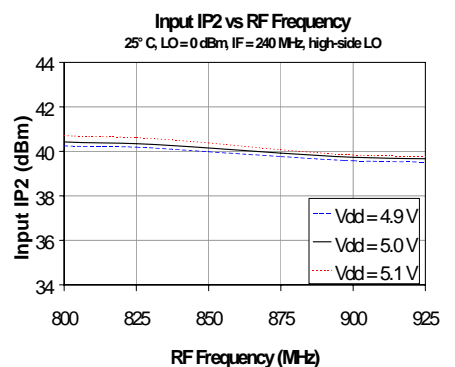
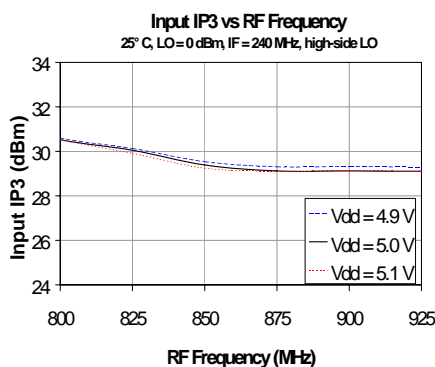
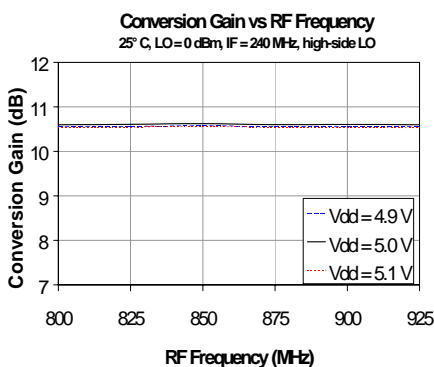
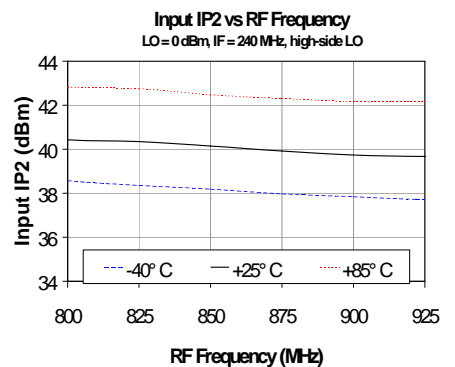
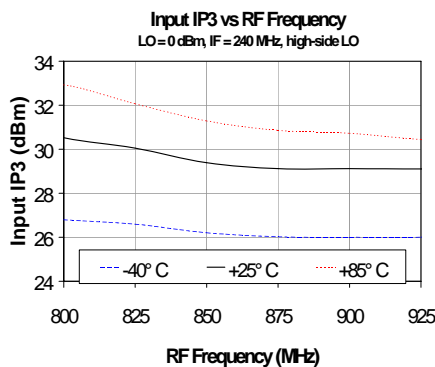
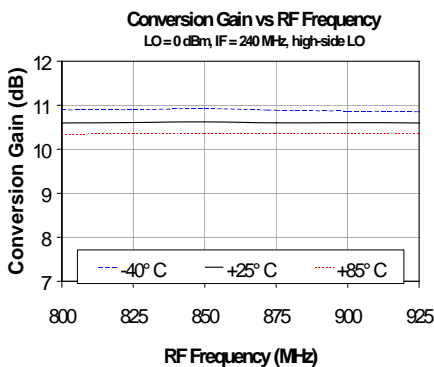
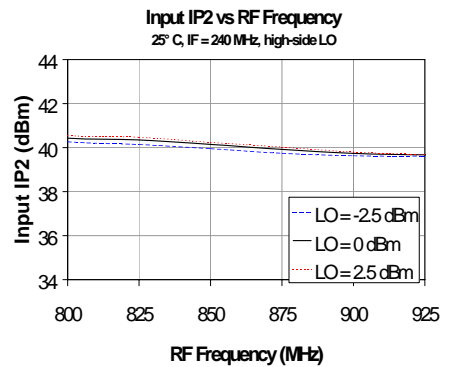
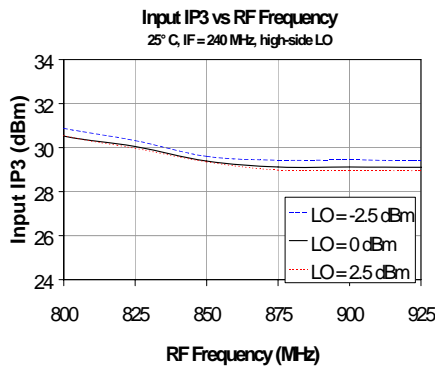
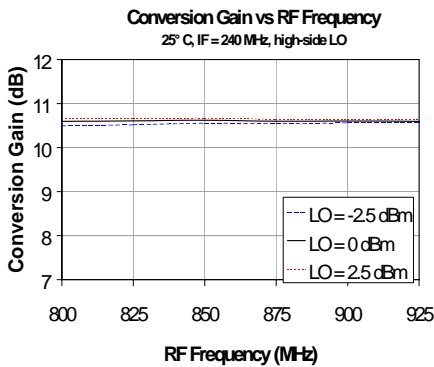
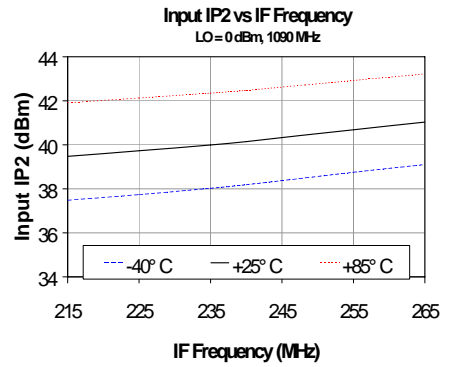
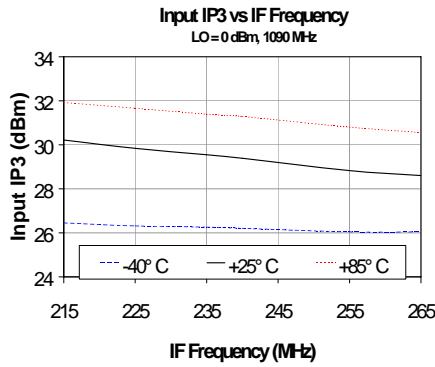
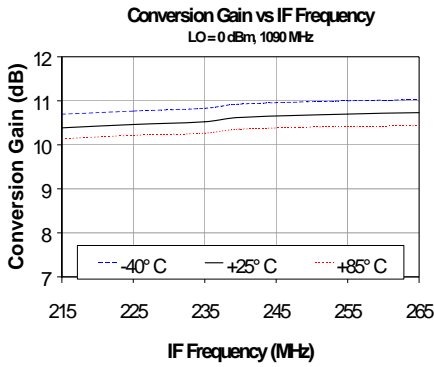
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CV210-3APCB240 Application Circuit Performance Plots





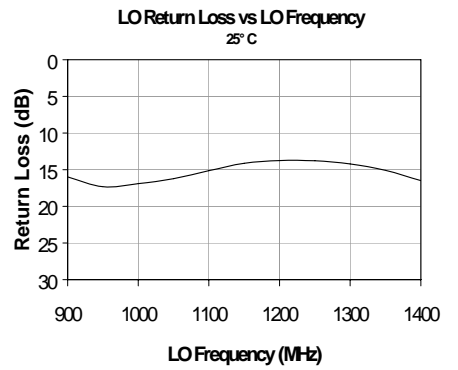
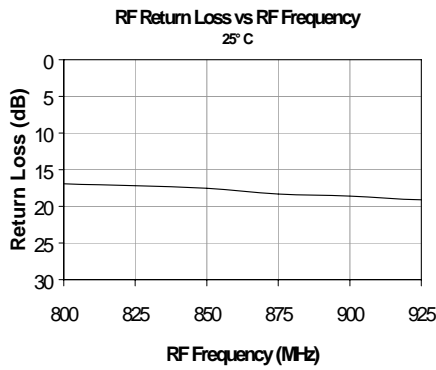
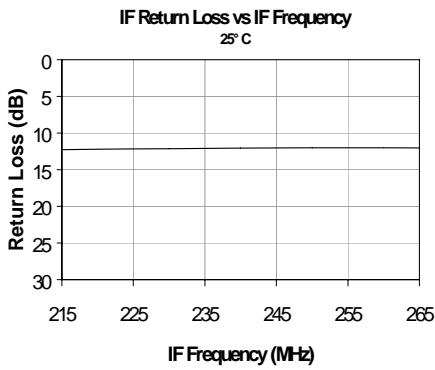
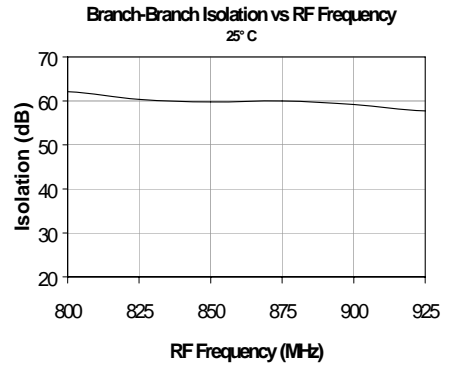
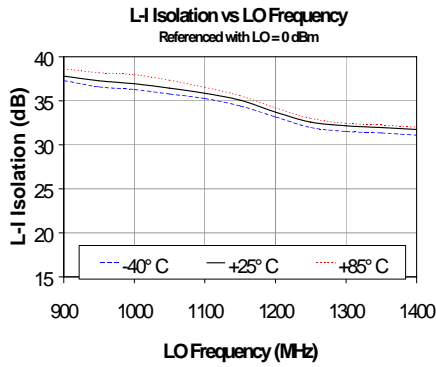
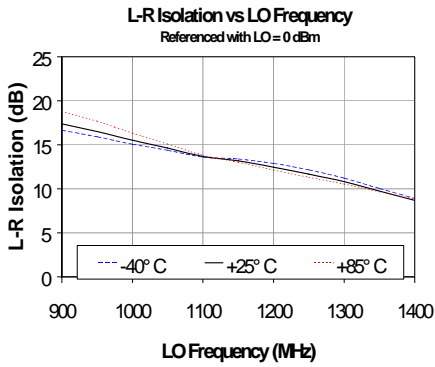
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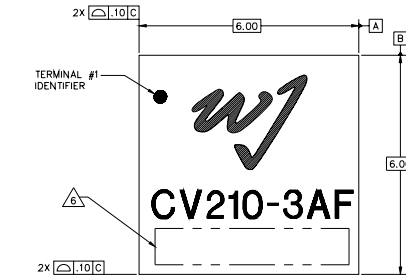
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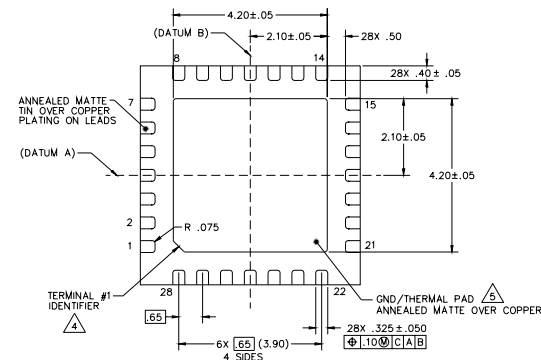
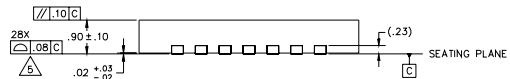
CV210-3AF Mechanical Information

This package is lead-free/RoHS-compliant. It is compatible with both lead-free (maximum 260°C reflow temperature) and leaded (maximum 245°C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

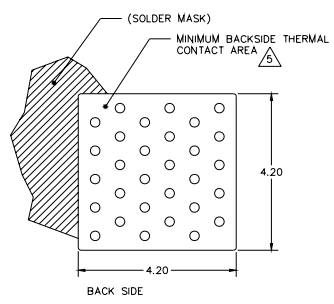
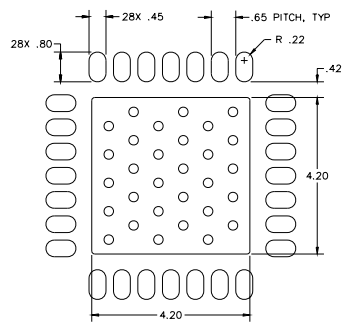
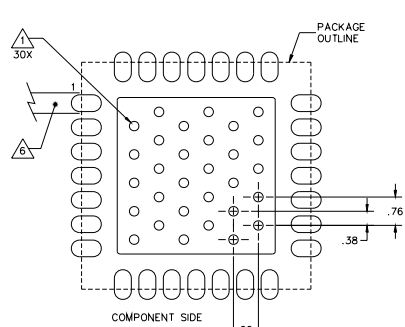
Outline Drawing



- NOTES:
- EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-220, ISSUE E (VARIATION VJJC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
 - DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
 - ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- ⚠ THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JEDEC 95-1 SPP-012.
 - ⚠ COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
 - ⚠ ALPHA-NUMERIC LOT CODE.



Mounting Configuration / Land Pattern



- NOTES:
- GROUND/THERMAL VIAS ARE CRITICAL FOR THE PROPER PERFORMANCE OF THIS DEVICE. VIAS SHOULD USE A .35mm (#80/.0135") DIAMETER DRILL AND HAVE A FINAL PLATED THRU DIAMETER OF .25mm (.010").
 - ADD AS MUCH COPPER AS POSSIBLE TO INNER AND OUTER LAYERS NEAR THE PART TO ENSURE OPTIMAL THERMAL PERFORMANCE.
 - TO ENSURE RELIABLE OPERATION, DEVICE GROUND PADDLE-TO-GROUND PAD SOLDER JOINT IS CRITICAL.
 - ADD MOUNTING SCREWS NEAR THE PART TO FASTEN THE BOARD TO A HEATSINK. ENSURE THAT THE GROUND/THERMAL VIA REGION CONTACTS THE HEATSINK.
- ⚠ DO NOT PUT SOLDER MASK ON THE BACK SIDE OF THE PC BOARD IN THE REGION WHERE THE BOARD CONTACTS THE HEATSINK.
 - ⚠ RF TRACE WIDTH DEPENDS UPON THE PC BOARD MATERIAL AND CONSTRUCTION.
 - 7. USE 1 OZ. COPPER MINIMUM.
 - 8. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

Product Marking

The component will be lasermarked with a "CV210-3AF" product label with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information



Caution! ESD sensitive device.

ESD Rating: Class 1B
 Value: Passes ≥ 500V to <1000V
 Test: Human Body Model (HBM)
 Standard: JEDEC Standard JESD22-A114

ESD Rating: Class III
 Value: Passes ≥ 500V to <1000V
 Test: Charged Device Model (CDM)
 Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 2 at +260°C convection reflow
 Standard: JEDEC Standard J-STD-020

Functional Pin Layout

| Pin | FUNCTION | Pin | FUNCTION |
|-----|---|-----|---|
| 1 | No Connect | 15 | No Connect |
| 2 | GND | 16 | GND |
| 3 | LO Amp Bias | 17 | LO input |
| 4 | GND | 18 | GND |
| 5 | No Connect | 19 | No Connect |
| 6 | GND | 20 | GND |
| 7 | No Connect | 21 | +5 V |
| 8 | GND | 22 | GND |
| 9 | Channel 2 Mixer IF/RF Port (goes to diplexer) | 23 | Channel 1 IF Amp Output / Bias |
| 10 | GND | 24 | GND |
| 11 | Channel 2 IF Amp Input | 25 | Channel 1 IF Amp Input |
| 12 | GND | 26 | GND |
| 13 | Channel 2 IF Amp Output / Bias | 27 | Channel 2 Mixer IF/RF Port (goes to diplexer) |
| 14 | GND | 28 | GND |

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