FAIRCHILD
SEMICONDUCTOR™

NC7SZ125
TinyLogic™ UHS Buffer with 3-STATE Output

General Description

The NC7SZ125 is a single buffer with 3-STATE output from Fairchild's Ultra High Speed Series of TinyLogic™. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.8V to 5.5V range.

The inputs and output are high impedance above ground when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage. The output tolerates voltages above V_{CC} when in the 3-STATE condition.

Features

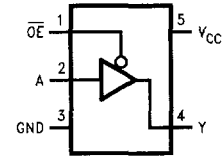
- Space saving SOT23 or SC70 5-lead package
- Ultra High Speed; t_{PD} 2.6 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive; ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.8V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Product Number	Package Drawing	Package Top Mark	Package Description	Supplied As
NC7SZ125M5	MA05B	7Z25	5-Lead SOT23, JEDEC MO-178, 1.6mm	250 Units on Tape and Reel
NC7SZ125M5X	MA05B	7Z25	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ125P5	MAA05A	Z25	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	250 Units on Tape and Reel
NC7SZ125P5X	MAA05A	Z25	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel

Logic Symbol

Connection Diagram



(Top View)

Pin Descriptions

Pin Names	Description
A, $\overline{OE}$	Inputs
Y	Output

Function Table

Inputs		Output
$\overline{OE}$	In A	Out Y
L	L	L
L	H	H
H	X	Z

H = HIGH Logic Level
L = LOW Logic Level
X = HIGH or LOW Logic Level
Z = HIGH Impedance State

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +6V
DC Input Voltage (V_{IN})	−0.5V to +6V
DC Output Voltage (V_{OUT})	−0.5V to +6V
DC Input Diode Current (I_{IK})	
@V_{IN} < −0.5V	−50 mA
@ V_{IN} > 6V	+20 mA
DC Output Diode Current (I_{OK})	
@V_{OUT} < −0.5V	−50 mA
@ V_{OUT} > 6V, V_{CC} = GND	+20 mA
DC Output Current (I_{OUT})	± 50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L);	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions

Supply Voltage Operating (V_{CC})	1.8V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	
Active State	0V to V_{CC}
3-STATE	0V to 5.5V
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 1.8V, 2.5V ±0.2V	0 ns/V to 20 ns/V
V_{CC} = 3.3V ±0.3V	0 ns/V to 10 ns/V
V_{CC} = 5.0V ± 0.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
		(V)	Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.8	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3–5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	1.8			0.25 V_{CC}		0.25 V_{CC}	V		
		2.3–5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	1.8	1.7	1.8		1.7		V	V_{IN} = V_{IH}	I_{OH} = −100 µA
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		2.3	1.9	2.15		1.9		V		I_{OH} = −8 mA
		3.0	2.4	2.80		2.4				I_{OH} = −16 mA
		3.0	2.3	2.68		2.3				I_{OH} = −24 mA
		4.5	3.8	4.20		3.8				I_{OH} = −32 mA
V_{OL}	LOW Level Output Voltage	1.8		0.0	0.1		0.1	V	V_{IN} = V_{IL}	I_{OL} = 100 µA
		2.3		0.0	0.1		0.1			
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		2.3		0.10	0.3		0.3	V		I_{OL} = 8 mA
		3.0		0.15	0.4		0.4			I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0–5.5			±1		±10	µA	0≤V_{IN} ≤5.5V	
I_{OZ}	3-STATE Output Leakage	1.8–5.5			±1		±10	µA	V_{IN} = V_{IH} or V_{IL} 0≤V_O≤ 5.5V	
I_{OFF}	Power Off Leakage Current	0.0			1		10	µA	V_{IN} or V_{OUT} = 5.5V	
I_{CC}	Quiescent Supply Current	1.8–5.5			2.0		20	µA	V_{IN} = 5.5V, GND	

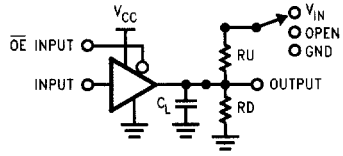
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Min	Typ	Max	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions	Fig. No.
t_{PLH}	Propagation Delay	1.8	2	5.3	11.0	2	11.5	ns	C_L = 15 pF, R_D = 1 MΩ, S_1 = OPEN	Figure 1
t_{PHL}		2.5 ± 0.2	0.8	3.4	7.5	0.8	8.0			Figure 3
		3.3 ± 0.3	0.5	2.5	5.2	0.5	5.5			
		5.0 ± 0.5	0.5	2.1	4.5	0.5	4.8			
t_{PLH}	Propagation Delay	3.3 ± 0.3	1.5	3.2	5.7	1.5	6.0	ns	C_L = 50 pF, R_D = 500Ω, S_1 = OPEN	Figure 1
t_{PHL}		5.0 ± 0.5	0.8	2.6	5.0	0.8	5.3			Figure 3
t_{PZL}	Output Enable Time	1.8	2	7.0	12.5	2	13	ns	C_L = 50 pF, RD = 500Ω RU = 500Ω S_1 = GND for t_{PZH} S_1 = V_{IN} for t_{PZL} V_{IN} = 2 x V_{CC}	Figure 1
t_{PZH}		2.5 ± 0.2	1.5	4.6	8.5	1.5	9			Figure 3
		3.3 ± 0.3	1.5	3.5	6.2	1.5	6.5			
		5.0 ± 0.5	0.8	2.8	5.5	0.8	5.8			
t_{PLZ}	Output Disable Time	1.8	2	5.4	11	2	12	ns	C_L = 50 pF, RD = 500Ω RU = 500Ω S_1 = GND for t_{PHZ} S_1 = V_{IN} for t_{PLZ} V_{IN} = 2 x V_{CC}	Figure 1
t_{PHZ}		2.5 ± 0.2	1.5	3.5	8	1.5	8.5			Figure 3
		3.3 ± 0.3	1.0	2.8	5.7	1.0	6			
		5.0 ± 0.5	0.5	2.1	4.7	0.5	5.0			
C_{IN}	Input Capacitance	0		4				pF		
C_{OUT}	Output Capacitance	0		8						
C_{PD}	Power Dissipation	3.3		17				pF	(Note 2)	Figure 2
	Capacitance	5.0		24						

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

$I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

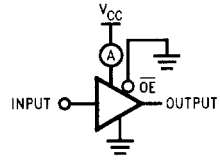
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f$ = 1.8 ns;

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

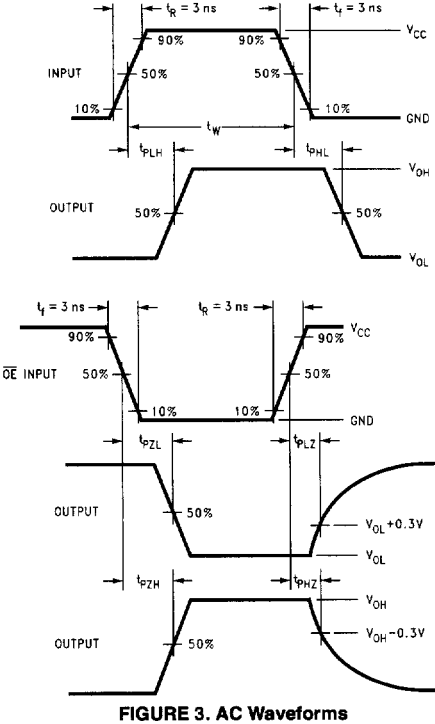


FIGURE 3. AC Waveforms