

Am29338

32-Bit Byte Queue

ADVANCE INFORMATION

Am29338

DISTINCTIVE CHARACTERISTICS

- **Intelligent FIFO Array**
 - Array of four intelligent FIFO buffers, each 9 bits wide, 32 bits deep (RAM-based)
- **Queueing/Dequeueing**
 - Allows variable width queueing/dequeueing in one cycle
- **Byte Rotation**
 - Four bytes can be rotated at the input as well as at the output of the Byte Queue. This allows interfacing between incompatible byte assignments.
- **Asynchronous and Synchronous Operation**
 - Supports communication between systems with different clocks and different bus widths
- **Retransmit**
 - Data can be read out repeatedly
- **Horizontal Cascading**
 - Up to four devices allow simultaneous input or output up to 16 bytes
- **Parity Check**
 - Protects data at the input and the output

GENERAL DESCRIPTION

The Am29338 is an intelligent FIFO that allows up to four bytes to be queued and up to four bytes to be dequeued in a single cycle. When four devices are cascaded horizontally, up to sixteen bytes can be dequeued in a single cycle.

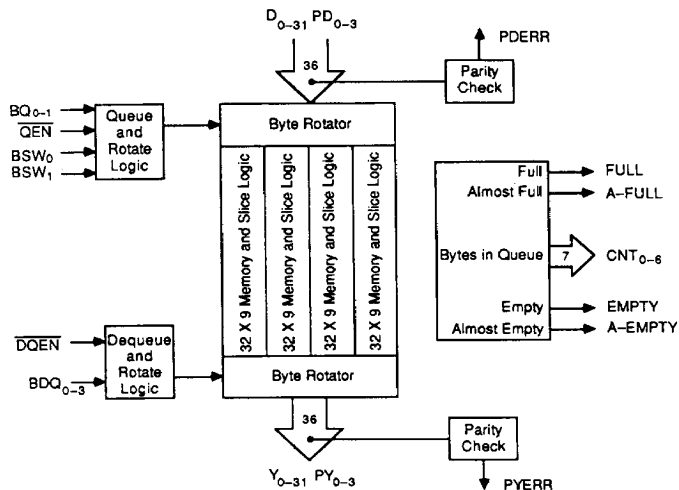
The Am29338 queues variable-length data by disassembling the input data, which is aligned on the least-significant byte of the input bus (D), into individual bytes. These bytes are packed internally in FIFO (first-in, first-out) order. The data to be dequeued is unpacked and realigned to the least-significant byte of the output bus (Y). Queueing and dequeuing can be performed simultaneously. With the

retransmit capability, the part can repeatedly send the block of data stored in the queue without having to requeue it. This is useful for retransmitting a block of data upon receipt of an error in I/O applications or for loop-locking in instruction-prefetch applications.

The queue operates in synchronous or asynchronous mode, and is useful as an instruction-prefetch queue or as a general-purpose FIFO buffer.

The device is manufactured in AMD's bipolar IMOX* technology and comes in a 120-lead pin-grid-array package.

BLOCK DIAGRAM



BD007490

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

3-115

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RELATED AMD PRODUCTS

Part No.	Description
Am2900 Family	4-Bit Microprocessor Slice Family
Am29C00 Family	CMOS 4-Bit Microprocessor Slice Family
Am29C101	CMOS 16-Bit Microprocessor Slice
Am29114	Real-Time Interrupt Controller
Am29116	16-Bit Bipolar Microprocessor
Am29116A	High-Speed 16-Bit Bipolar Microprocessor
Am29L116A	Low-Power 16-Bit Bipolar Microprocessor
Am29C116	CMOS 16-Bit Microprocessor
Am29C116-1	CMOS 16-Bit Microprocessor
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	Four-Port, Dual-Access Register File
Am29C334	CMOS Four-Port, Dual-Access Register File
Am29337	16-Bit Cascadable Bounds Checker

CONNECTION DIAGRAM Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	Y16	Y17	OE	Y21	GNDT	PY3	Y27	Y28	VCCT	CNT2	GNDT	CNT6	BDQ3
2	PY2	Y15	Y18	Y20	Y23	Y24	Y26	Y29	Y31	CNT1	CNT4	CNT5	BDQ2
3	GNDT	Y14	Y13	Y19	Y22	VCCE	Y25	GNDE	Y30	CNT0	CNT3	BDQ0	BDQ1
4	Y12	Y11	Y10								OEEN	RESET	RXMIT
5	VCCT	Y9	Y8								OEEN	BSW1	DOCLK
6	Y7	PY1	GNDT								OCLK	BO1	BSW0
7	Y6	Y5	Y4								BQ0	NC	D30
8	Y2	Y3	VCCT								D31	D28	D29
9	GNDT	Y1	Y0								D27	D25	D26
10	PY0	PYERR	PDERR								D24	PD3	D23
11	VCCT	A-FULL	PD0	D2	VCCE	D6	D7	D12	GNDE	D15	D22	D20	D21
12	FULL	POS1	POS0	D1	VCCE	D3	D8	D9	GNDE	D14	PD2	D19	D18
13	A-EMPTY	EMPTY	D5	D0	VCCE	D4	PD1	D11	GNDE	D13	D10	D16	D17

CD011040

Legend: GNDE: GND, ECL
 GNDT: GND, TTL
 VCCE: V_{CC}, ECL
 VCCT: V_{CC}, TTL

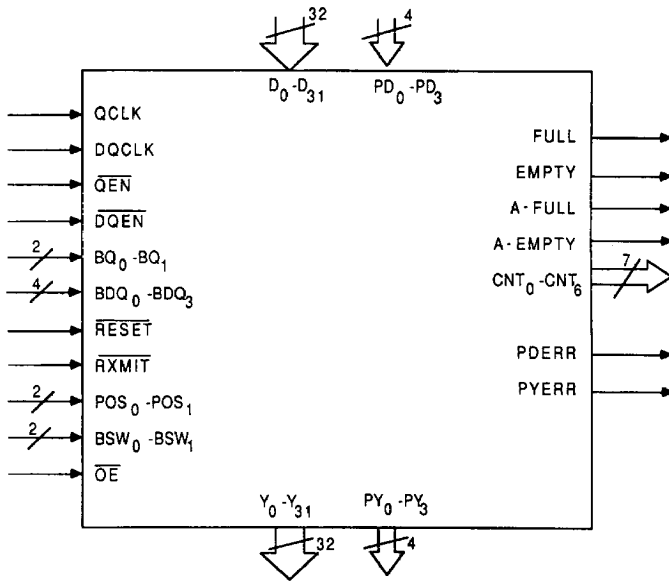
PIN DESIGNATIONS
(Sorted by Pin Number)

PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
1	A1	Y ₁₆	115	C5	Y ₈	40	G11	D ₇	27	L10	D ₂₄
120	A2	PY ₂	113	C6	GND, TTL	36	G12	D ₈	88	L11	D ₂₂
59	A3	GND, TTL	52	C7	Y ₄	96	G13	PD ₁	32	L12	PD ₂
58	A4	Y ₁₂	53	C8	V _{CC} , TTL	69	H1	Y ₂₈	35	L13	D ₁₀
56	A5	V _{CC} , TTL	109	C9	Y ₀	10	H2	Y ₂₉	75	M1	CNT ₆
114	A6	Y ₇	48	C10	PDERR	68	H3	GND, ECL	15	M2	CNT ₅
54	A7	Y ₆	44	C11	PD ₀	34	H11	D ₁₂	77	M3	BDQ ₀
51	A8	Y ₂	104	C12	POS ₀	95	H12	D ₉	78	M4	RESET
50	A9	GND, TTL	41	C13	D ₅	94	H13	D ₁₁	80	M5	BSW ₁
49	A10	PY ₀	4	D1	Y ₂₁	11	J1	V _{CC} , TTL	81	M6	BQ ₁
47	A11	V _{CC} , TTL	63	D2	Y ₂₀	71	J2	Y ₃₁	82	M7	NC
106	A12	FULL	3	D3	Y ₁₉	70	J3	Y ₃₀	25	M8	D ₂₈
46	A13	A-EMPTY	102	D11	D ₂	38	J11	GND, ECL	86	M9	D ₂₅
61	B1	Y ₁₇	43	D12	D ₁	38	J12	GND, ECL	87	M10	PD ₃
60	B2	Y ₁₅	103	D13	D ₀	38	J13	GND, ECL	89	M11	D ₂₀
119	B3	Y ₁₄	5	E1	GND, TTL	13	K1	CNT ₂	30	M12	D ₁₉
117	B4	Y ₁₁	65	E2	Y ₂₃	72	K2	CNT ₁	91	M13	D ₁₆
116	B5	Y ₉	64	E3	Y ₂₂	12	K3	CNT ₀	16	N1	BDQ ₃
55	B6	PY ₁	98	E11	V _{CC} , ECL	92	K11	D ₁₅	76	N2	BDQ ₂
112	B7	Y ₅	98	E12	V _{CC} , ECL	33	K12	D ₁₄	17	N3	BDQ ₁
111	B8	Y ₃	98	E13	V _{CC} , ECL	93	K13	D ₁₃	19	N4	FXMIT
110	B9	Y ₁	6	F1	PY ₃	14	L1	GND, TTL	20	N5	DQCLK
108	B10	PYERR	66	F2	Y ₂₄	74	L2	CNT ₄	21	N6	BSW ₀
107	B11	A-FULL	8	F3	V _{CC} , ECL	73	L3	CNT ₃	24	N7	D ₃₀
45	B12	POS ₁	100	F11	D ₆	18	L4	DQEN	84	N8	D ₂₉
105	B13	EMPTY	42	F12	D ₃	79	L5	QEN	26	N9	D ₂₆
2	C1	OE	101	F13	D ₄	23	L6	QCLK	28	N10	D ₂₃
62	C2	Y ₁₈	9	G1	Y ₂₇	22	L7	BQ ₀	29	N11	D ₂₁
118	C3	Y ₁₃	67	G2	Y ₂₆	83	L8	D ₃₁	90	N12	D ₁₈
57	C4	Y ₁₀	7	G3	Y ₂₅	85	L9	D ₂₇	31	N13	D ₁₇

PIN DESIGNATIONS
(Sorted by Pin Name)

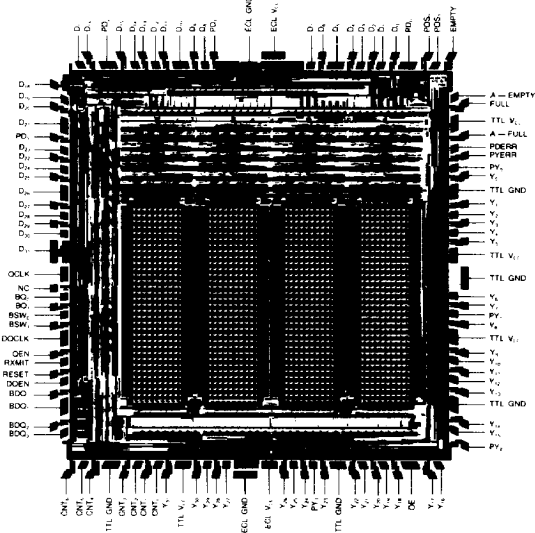
PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
82	M7	NC	34	H11	D12	59	A3	GND, TTL	51	A8	Y2
46	A13	A-EMPTY	93	K13	D13	5	E1	GND, TTL	111	B8	Y3
107	B11	A-FULL	33	K12	D14	50	A9	GND, TTL	52	C7	Y4
77	M3	BDQ ₀	92	K11	D15	2	C1	OE	112	B7	Y5
17	N3	BDQ ₁	91	M13	D16	44	C11	PD ₀	54	A7	Y6
76	N2	BDQ ₂	31	N13	D17	96	G13	PD ₁	114	A6	Y7
16	N1	BDQ ₃	90	N12	D18	32	L12	PD ₂	115	C5	Y8
22	L7	BQ ₀	30	M12	D19	87	M10	PD ₃	116	B5	Y9
81	M6	BQ ₁	89	M11	D20	48	C10	PDERR	57	C4	Y10
21	N6	BSW ₀	29	N11	D21	104	C12	POS ₀	117	B4	Y11
80	M5	BSW ₁	88	L11	D22	45	B12	POS ₁	58	A4	Y12
12	K3	CNT ₀	28	N10	D23	49	A10	PY ₀	118	C3	Y13
72	K2	CNT ₁	27	L10	D24	55	B6	PY ₁	119	B3	Y14
13	K1	CNT ₂	86	M9	D25	120	A2	PY ₂	60	B2	Y15
73	L3	CNT ₃	26	N9	D26	6	F1	PY ₃	1	A1	Y16
74	L2	CNT ₄	85	L9	D27	108	B10	PYERR	61	B1	Y17
15	M2	CNT ₅	25	M8	D28	23	L6	QCLK	62	C2	Y18
75	M1	CNT ₆	84	N8	D29	79	L5	QEN	3	D3	Y19
103	D13	D ₀	24	N7	D30	78	M4	RESET	63	D2	Y20
43	D12	D ₁	83	L8	D31	19	N4	RXMIT	4	D1	Y21
102	D11	D ₂	20	N5	DQCLK	98	E11	V _{CC} , ECL	64	E3	Y22
42	F12	D ₃	18	L4	DQEN	98	E12	V _{CC} , ECL	65	E2	Y23
101	F13	D ₄	105	B13	EMPTY	98	E13	V _{CC} , ECL	66	F2	Y24
41	C13	D ₅	106	A12	FULL	8	F3	V _{CC} , ECL	7	G3	Y25
100	F11	D ₆	38	J11	GND, ECL	56	A5	V _{CC} , TTL	67	G2	Y26
40	G11	D ₇	38	J12	GND, ECL	53	C8	V _{CC} , TTL	9	G1	Y27
36	G12	D ₈	38	J13	GND, ECL	47	A11	V _{CC} , TTL	69	H1	Y28
95	H12	D ₉	68	H3	GND, ECL	11	J1	V _{CC} , TTL	10	H2	Y29
35	L13	D ₁₀	113	C6	GND, TTL	109	C9	Y ₀	70	J3	Y30
94	H13	D ₁₁	14	L1	GND, TTL	110	B9	Y ₁	71	J2	Y31

LOGIC SYMBOL



LS002851

METALLIZATION AND PAD LAYOUT



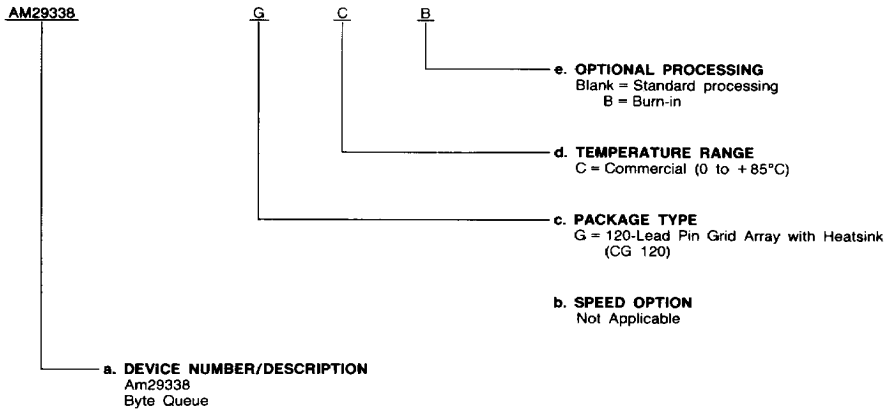
Die Size: 270 x 290 mils²
Gate Count: 9000

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM29338	GC, GCB

PIN DESCRIPTION

A-EMPTY Almost Empty (Output; Active HIGH)

Indicates that there are less than four bytes of data in the queue. It is used in either synchronous or asynchronous operation.

A-FULL Almost Full (Output; Active HIGH)

Indicates that there are less than four bytes of space remaining. It is used in either synchronous or asynchronous operation.

BDQ₀ - BDQ₃ Bytes Dequeued (Input)

Selects the number of bytes to be dequeued (see Table 2). The byte queue must operate synchronously to be able to dequeue more than four bytes in a single cycle.

BQ₀ - BQ₁ Bytes Queued (Input)

Selects the number of bytes to be queued (see Table 1).

BSW₀ - BSW₁ Byte Swap (Input)

Allows the bytes on the input to be reordered (see Table 3).

CNT₀ - CNT₆ Byte Count (Output)

Gives the current number of bytes in the queue. These are used only in synchronous operation.

D₀ - D₃₁ Data Input (Input)

Data inputs to be queued.

DQCLK Dequeue Clock (Input)

Dequeues the number of bytes set up on the Y bus. A LOW-to-HIGH transition on this input adjusts the internal dequeue pointers by the number set up on the BDQ lines.

DQEN Dequeue Enable (Input; Active LOW)

While DQEN is LOW, dequeuing is performed normally. When DQEN is HIGH, DQCLK is disabled.

EMPTY Empty (Output; Active HIGH)

Indicates that the queue is empty. It is used in either synchronous or asynchronous operation.

FULL Full (Output; Active HIGH)

Indicates that the queue is full. It is used in either synchronous or asynchronous operation.

OE Output Enable (Input; Active LOW)

When OE is LOW, the four bytes following the current dequeue pointer and the corresponding parity bits are on Y and PY outputs. When OE is HIGH, Y and PY outputs are three stated.

PD₀ - PD₃ Data Input Parity (Input)

The input parity bits for the corresponding byte on the D inputs. Only the bytes to be queued and the corresponding

PD lines are checked for possible parity error. The byte queue has the even parity.

PDERR Data Input Parity Error (Output; Active HIGH)

If any of the bytes to be queued have a parity error, PDERR is asserted.

POS₀ - POS₁ Position (Input)

These inputs are used to program the location of each byte queue in horizontally cascaded system upon RESET (see Table 4).

PY₀ - PY₃ Output Data Parity (Output; Three State)

The output parity bits for Y outputs. When OE is HIGH, the parity bits of the four bytes following the dequeue pointer appear on these outputs. The byte queue has the even parity.

PYERR Y Output Parity Error (Output; Active HIGH)

If any of the bytes on the output has a parity error, PYERR is asserted.

QCLK Queue Clock (Input)

When QCLK is LOW, the number of bytes set up on the BQ lines are written into the next free space in the queue from the data set up on the D inputs. On a LOW-to-HIGH transition of this input, the internal queue pointers are updated. If QEN is HIGH, QCLK has no effect.

QEN Queue Enable (Input; Active LOW)

When QEN is LOW, queuing is performed normally. When QEN is HIGH, QCLK is disabled.

RESET Reset (Input; Active LOW)

When RESET is LOW, both the internal queue pointer and the internal dequeue pointer are reset to the first RAM location and both EMPTY and A_EMPTY are asserted.

RXMIT Retransmit (Input; Active LOW)

When RXMIT is LOW, the internal dequeue pointers are reset to the first RAM location while the internal queue pointers remain unchanged. This allows the data contained between the current queue pointer and the first RAM location to become available for dequeuing again. The effect of asserting RXMIT is defined only if 128 bytes or less have been queued since the last assertion of RESET (see Figure 5).

Y₀ - Y₃₁ Data Output (Output; Three State)

The four bytes following the current dequeue pointer appear on these outputs when OE is LOW. When OE is HIGH, they are three stated.

FUNCTIONAL DESCRIPTION

Architecture

The Am29338 is a 32-bit high-performance general-purpose intelligent FIFO that stores up to 128 bytes in the internal RAM slices and queues or dequeues up to four bytes in a single cycle. The byte queue is divided into five functional blocks: 1) four memory-slice logics, 2) byte rotators for input and output buses, 3) rotate-enable logic, 4) byte-count logic, and 5) full/empty-generate logic. The byte-oriented parity checking is provided on both the D-input bus and the Y-output bus. Figure 1 shows a detailed block diagram of the byte queue.

Memory-Slice Logic

Figure 2 shows a detail of the memory-slice logic. It consists of a 32 x 9 RAM, queue and dequeue pointers, adders for the pointers, and a full/empty detector. The RAM has independent 9-bit read and write ports. Both ports are accessible simultaneously if different RAM locations are operated on. A parity bit is stored along with its corresponding byte into the RAM.

The queue and dequeue pointers point to the next location available for dequeuing. The next locations are produced by the internal adders with BQ_0-1 or BDQ_0-3 and the current pointer values. When RESET is asserted, both pointers are set to zero and the RAM is flushed. These pointers are also used to indicate that the RAM is either empty or full for each memory slice. The slice-empty or slice-full signal is used to

combinationally form FULL, A-FULL, EMPTY, and A-EMPTY signals.

Byte Rotator

There are two byte rotators in the byte queue. Each accepts 36-bit wide data and performs rotation of bytes according to the 2-bit rotate values fed from the rotate-enable logic. The input byte rotator realigns and stores the bytes to be queued into the next free slice location. The output byte rotator realigns the bytes to be dequeued to the least significant bit of the Y-output bus.

Rotate-Enable Logic

The queue and dequeue rotate-enable logic keeps track of which slice holds the first byte of the next queue/dequeue operation. A modulo-4 counter is used to rotate the data in operation and enables the correct slices by the number of bytes specified by either BQ_0-1 or BDQ_0-3 .

The queue rotate-enable logic also performs byte and/or word swaps on the incoming data. The input bytes are swapped in one of four ways, according to Table 3, with BSW_0-1 and the current modulo-4 byte count through the input byte rotator.

Byte-Count Logic

This logic consists of a queue count register and a dequeue count register. The registers are incremented during a queue/dequeue operation by the number of bytes in the operation. The combinational subtract logic outside of these registers determines the number of bytes stored in the byte queue.

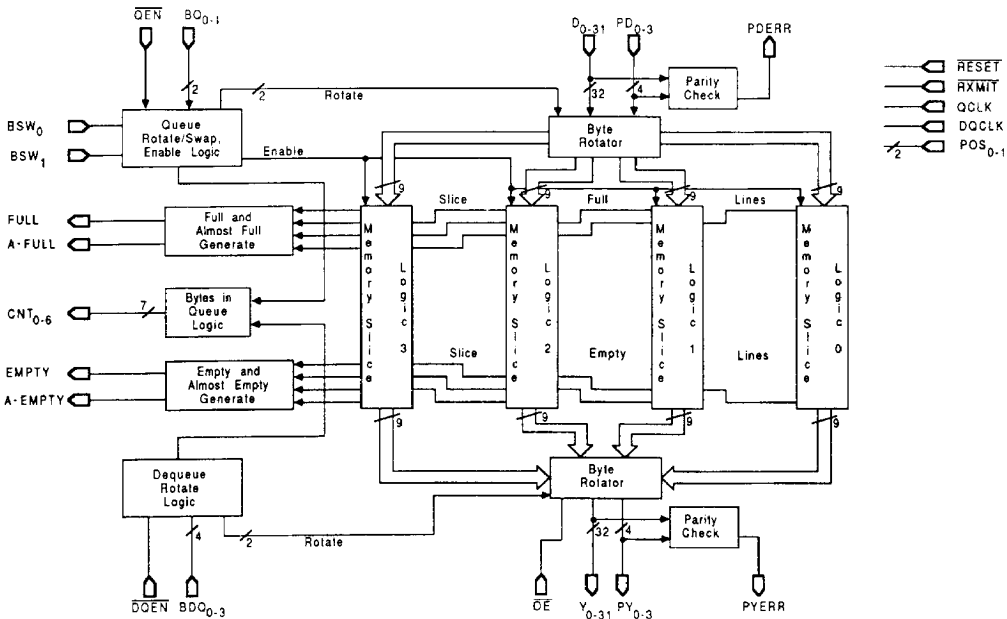
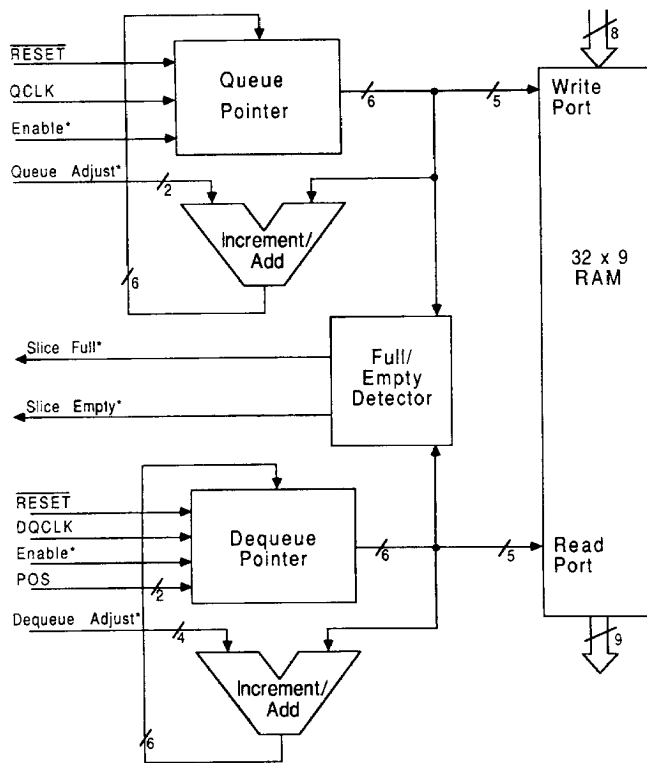


Figure 1. Am29338 Byte Queue Detailed Block Diagram

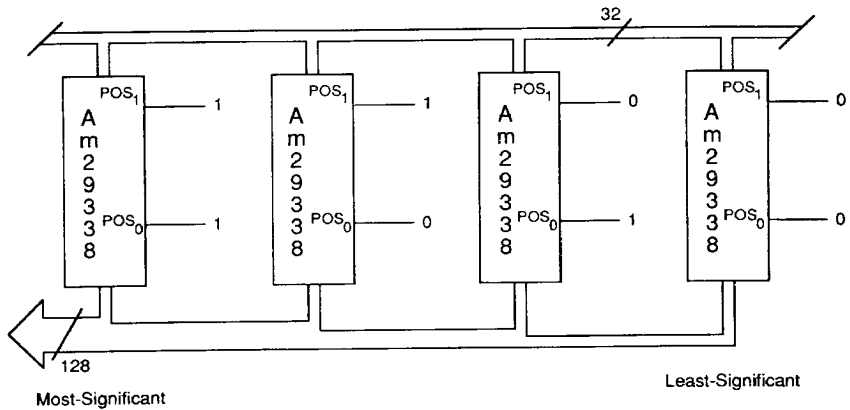
BD006902



*Internally generated inputs.

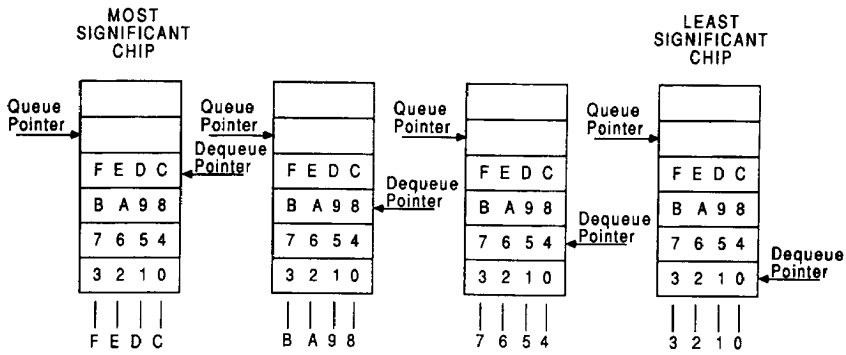
BD006911

Figure 2. Memory and Slice Logic



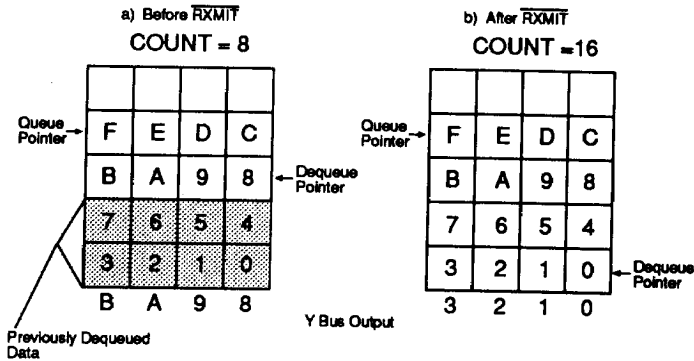
BD007010

Figure 3. Position Line Values in Horizontally Cascaded System



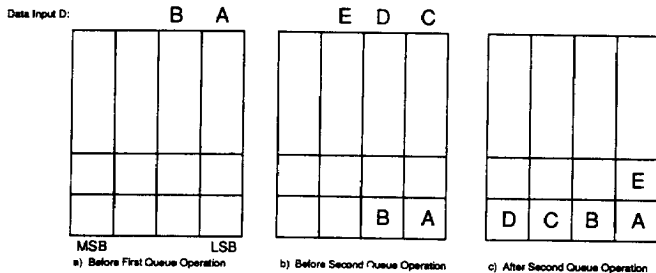
BD006930

Figure 4. An Example of Horizontal Cascading



TB001131

Figure 5. Retransmit Function with the Am29338



TB001141

Figure 6. Queuing with the Am29338

Notes: 1. Each of the four segments stands for a memory size; MSB = Most-Significant Byte, and LSB = Least-Significant Byte.

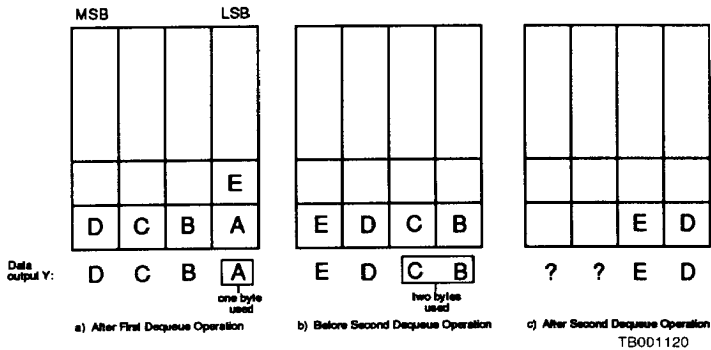


Figure 7. Dequeuing with the Am29338

- Notes: 1. Each of the four segments stands for a memory size; MSB = Most-Significant Byte, and LSB = Least-Significant Byte.
 2. First, one byte is dequeued ('A'), followed by a dequeue of two bytes ('CB').

TABLE 1. SELECTING THE NUMBER OF BYTES TO BE QUEUED

BQ ₁	BQ ₀	Bytes To Be Queued
L	H	1
H	L	2
H	H	3
L	L	4

Key: L = LOW
 H = HIGH

TABLE 2. SELECTING THE NUMBER OF BYTES TO BE DEQUEUED

BDQ ₃	BDQ ₂	BDQ ₁	BDQ ₀	Bytes To Be Dequeued
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5*
L	H	H	L	6*
L	H	H	H	7*
H	L	L	L	8*
H	L	L	H	9*
H	L	H	L	10*
H	L	H	H	11*
H	H	L	L	12*
H	H	L	H	13*
H	H	H	L	14*
H	H	H	H	15*
L	L	L	L	16*

Key: L = LOW
 H = HIGH

* This is possible when four of the byte queues are cascaded together. The byte queue must be operated synchronously to select more than four bytes for dequeuing.

TABLE 3. ENCODING OF BSW INPUTS

Inputs		Outputs			
BSW ₁	BSW ₀	A	B	C	D
L	L	A	B	C	D
L	H	B	A	D	C
H	L	C	D	A	B
H	H	D	C	B	A

Key: L = LOW
H = HIGH

Note: The assumption is made that the 32-bit data "A B C D" appears on the input bus.

TABLE 4. LOCATION IDENTIFICATION FOR HORIZONTAL CASCADING

POS ₁	POS ₀	Location
L	L	0
L	H	1
H	L	2
H	H	3

Key: L = LOW
H = HIGH

Note: "0" stands for the least significant chip and "3" the most significant chip.

Operational Modes

General Operation

To enter data into the Am29338, the number of bytes to be queued is set up on the Bytes Queued (BQ) pins; the corresponding data to be queued is set up on the Data Input (D) and Data Input Parity (PD) pins, aligned to the least-significant byte. If Queue Enable (\overline{QEN}) is asserted, the data is entered into the Am29338 while the Queue Clock (QCLK) is LOW, and the internal queue pointers are updated on the LOW-to-HIGH transition of QCLK.

Figure 6 shows an example of two bytes being queued, followed by three bytes being queued. Data is packed in the Am29338 so that no holes exist.

If Output Enable (\overline{OE}) is asserted, the first four bytes available for dequeuing and their corresponding parity appear on the Data Output (Y) and Data Parity (PY) pins. The number of these bytes to be dequeued is set up on the Bytes Dequeued (BDQ) pins. If Dequeue Enable (\overline{DEN}) is asserted, the LOW-to-HIGH transition of Dequeue Clock (DQCLK) updates the internal dequeue pointers, removing the dequeued bytes.

Figure 7 shows an example of one byte dequeued, followed by a dequeue of two bytes. The data to be dequeued next is least-significant-byte aligned on the output bus.

Synchronous Mode

Both synchronous and asynchronous operations are available for the byte queue. During synchronous operation, both QCLK and DQCLK must be asserted on the edge of a common clock within certain skew limits. The following signals can be used as valid status outputs for this mode: FULL, A-FULL, EMPTY, A-EMPTY, and CNT₀₋₆. Refer to the applications section for an example.

Asynchronous Mode

During asynchronous operation, QCLK and DQCLK clocks may be different. It is possible to execute queue and dequeue operations simultaneously if different locations are accessed. In this mode, CNT outputs are not guaranteed as valid and horizontal cascading is not possible. Refer to the applications section for an example.

Horizontal Cascading

In synchronous operation, four byte queues can be horizontally cascaded together. In this case, each of the four byte queues hold the same data and up to sixteen bytes may be dequeued in a single cycle, as shown in Table 2, and Figures 3 and 4. Each part has to be programmed with its position by the POS inputs, as shown in Table 4. In a normal operation, the internal dequeue pointer of each part is displaced according to the POS inputs. When \overline{RESET} or \overline{RXMIT} is asserted, the dequeue pointers are offset by the value programmed on the POS inputs.

Horizontal cascading is useful in instruction buffers designed for systems with large, variable instructions that can span many bytes.

APPLICATIONS

Using Am29338 as an Instruction-Prefetch Queue

Figure 8 shows the Am29338 used as an instruction-prefetch queue. Sequential 32-bit memory locations are fetched by the Instruction Fetch Unit (IFU) and are queued up in the byte queue. When the central processor needs the next instruction, it looks at the next four bytes from the byte queue. The central processor then determines the instruction length from the opcode and updates the dequeue pointer in the byte queue by setting up the instruction length on the BDQ lines and asserting DQCLK. When a jump occurs, the IFU flushes the

queue by asserting the RESET input and begins from the new address. For this application, the byte queue must be in synchronous mode.

Using the \overline{RXMIT} input, the byte queue can resend the block data through dequeuing rather than having to requeue it. This is useful for locking the loops into the byte queue and allows the processor to run faster than if it had to refetch instructions from memory or cache. Figure 9 illustrates how a loop can execute directly out of the byte queue.

Using Am29338 as a Hardware Mailbox in Multiprocessing System

A mailbox is a communication device between loosely coupled processes in a multi-programming system. Messages from one process to another are queued in the mailbox on a first-in, first-out (FIFO) basis. In a multiprocessing system, hardware mailboxes are required. This can be implemented using the Am29338 as shown in Figure 10.

When a process wishes to send a message to the mailbox, it calls a special operating-system routine. This routine first

reads the status of the mailbox; if it is not FULL, the routine first writes the message to the mailbox and returns to the calling process. If the mailbox is FULL, the operating system blocks the calling process on a special queue and enables interrupts from the mailbox. When a slot becomes available in the mailbox, the sending processor is interrupted. The interrupt routine sends the message to the mailbox, disables interrupts from the mailbox, and unblocks the blocked process. On the receiving side, the EMPTY status of the mailbox must be available to the receiving processor in order to allow the receiving process to be blocked if the mailbox is empty. When a mailbox slot becomes filled, a blocked process must be awakened by interrupting the receiving processor.

The mailbox can be extended to operate in a heterogeneous multiprocessing system. In this type of system, processors with varying data-path widths and clock frequencies are interconnected. For example, a 32-bit main processor may control 8- to 16-bit coprocessors. The ability of the Am29338 to match data-path widths and to queue and dequeue asynchronously allows processors of different widths and clock rates to communicate.

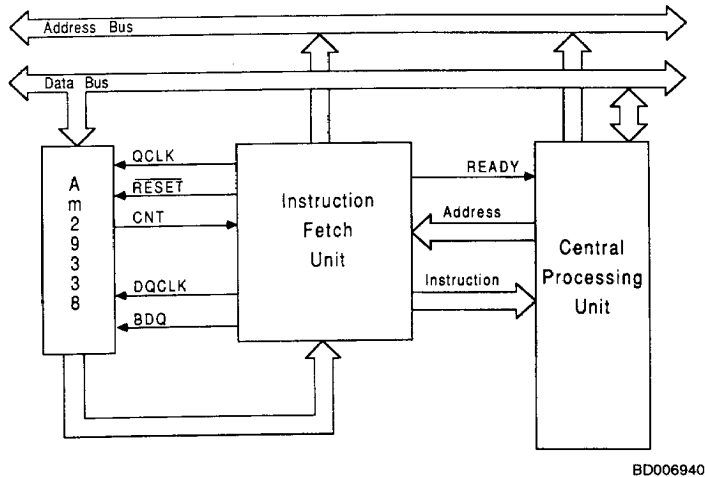
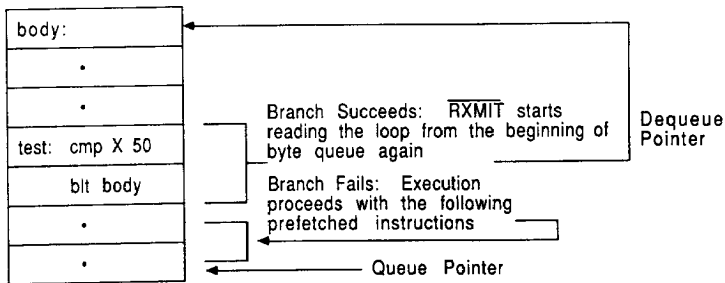
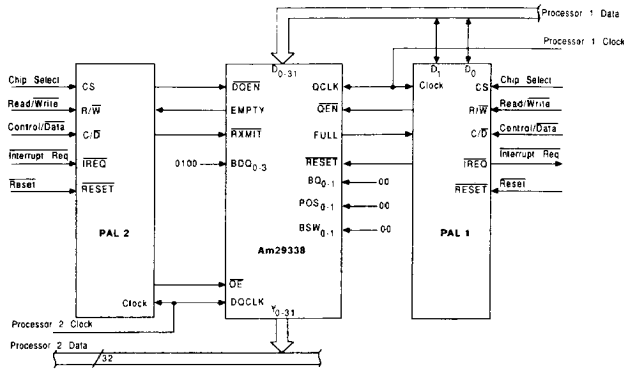


Figure 8. Instruction-Prefetch Queue



Note: This describes a block of macro instructions.

Figure 9. Loop Locking Using Am29338



BD006950

Figure 10. Implementation of a Hardware Mailbox

Suggestions for Power and Ground Pin Connections

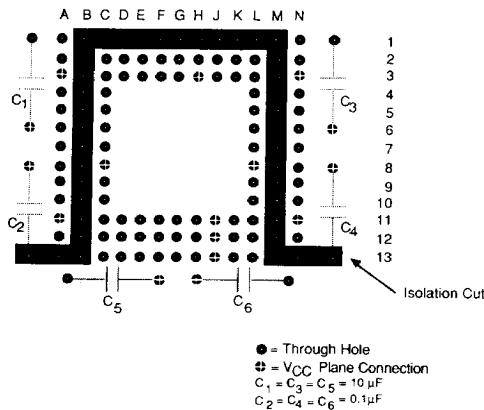
The Am29338 operates in an environment of fast signal rise times and substantial switching currents. Therefore, care must be exercised during circuit board design and layout, as with any high-performance component. The following is a suggested layout, but since systems vary widely in electrical configuration, an empirical evaluation of the intended layout is recommended.

The V_{CCT} and GN_{DT} pins, which carry output driver switching currents, tend to be electrically noisy. The V_{CCE} and GN_{DE} pins, which supply the ECL core of the device, tend to produce less noise, and the circuits they supply may be adversely affected by noise spikes on the V_{CCE} plane. For this reason, it is best to provide isolation between the V_{CCE} and V_{CCT} pins, as well as independent decoupling for each. Isolating the GN_{DE} and GN_{DT} pins is not required.

Printed Circuit-Board Layout Suggestions

1. Use of a multi-layer PC board with separate power, ground, and signal planes is highly recommended.
2. All V_{CCE} and V_{CCT} pins should be connected to the V_{CC} plane. V_{CCT} pins should be isolated from V_{CCE} pins by means of a slot cut in the V_{CC} plane; see Figure 11. By physically separating the V_{CCE} and V_{CCT} pins, coupled noise will be reduced.
3. All GN_{DE} and GN_{DT} pins should be connected directly to the ground plane.
4. The V_{CCT} pins should be decoupled to ground with a 0.1- μF ceramic capacitor and a 10- μF electrolytic capacitor, placed as closely to the Am29338 as is practical. V_{CCE} pins should be decoupled to ground in a similar manner.

A suggested layout is shown in Figure 11.



CD010890

Figure 11. Suggested Printed Circuit-Board Layout

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Case Temperature	
with Power Applied	-55 to +125°C
Supply Voltage	
with Respect to Ground	-0.5 to +7.0 V
DC Voltage Applied to Outputs	
for HIGH State	-0.5 V to +V _{CC} Max.
DC Input Voltage	-0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T _C)	0 to +85°C
Supply Voltage (V _{CC})	+4.75 to +5.25 V
θ _{JA}	(under 200 lfm)

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IL} or V _{IH} I _{OH} = -3 mA		2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IL} or V _{IH} I _{OL} = 16 mA				0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	V
V _I	Input Clamp Voltage	V _{CC} = Min. I _{IN} = -18 mA				-1.2	V
I _{IL}	Input LOW Current	V _{CC} = Max. V _{IN} = 0.5 V	QCLK, DQCLK Others			-1.0 -0.5	mA
I _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = 2.4 V				50	μA
I _I	Input HIGH Current	V _{CC} = Max. V _{IN} = 5.5 V				1.0	mA
I _{OZH} I _{OZL}	Off State (High-Impedance) Output Current	V _{CC} = Max.	V _O = 2.4 V V _O = 0.5 V			50 -50	μA
I _{SC}	Output Short-Circuit Current (Note 3)	V _{CC} = Max. to +0.5 V V _O = 0.5 V		-20		-80	mA
I _{CC}	Power Supply Current	V _{CC} = Max. All Inputs HIGH	T _C = 0 to +85°C T _C = +85°C		800	900 800	mA

- Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
 2. Typical values are for V_{CC} = +25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

SWITCHING CHARACTERISTICS over operating range (Note 1)

A. Combinational Propagation Delays

No.	From	To	Delay	Unit
1	D	PDERR	50	ns
2	PD	PDERR	50	ns
3	DQCLK ↑	A-EMPTY or A-FULL	44	ns
4	DQCLK ↑	CNT	46	ns
5	DQCLK ↑	EMPTY or FULL	44	ns
6	DQCLK ↑	PYERR	60	ns
7	DQCLK ↑	Y	52	ns
8	OE	PYERR	25	ns
9	OE	Y	25	ns
10	QCLK ↑	A-EMPTY or EMPTY	44	ns
11	QCLK ↑	CNT	46	ns
12	QCLK ↑	A-FULL or FULL	44	ns
13	RESET ↓	A-FULL or FULL	44	ns
14	RESET ↓	CNT	46	ns
15	RESET ↓	EMPTY or	44	ns
16	RESET ↓	PYERR	60	ns
17	RESET ↓	Y	52	ns
18	RXMIT ↓	A-FULL or FULL	44	ns
19	RXMIT ↓	CNT	46	ns
20	RXMIT ↓	A-EMPTY or EMPTY	44	ns
21	RXMIT ↓	PYERR	60	ns
22	RXMIT ↓	Y	52	ns

B. Setup and Hold Times

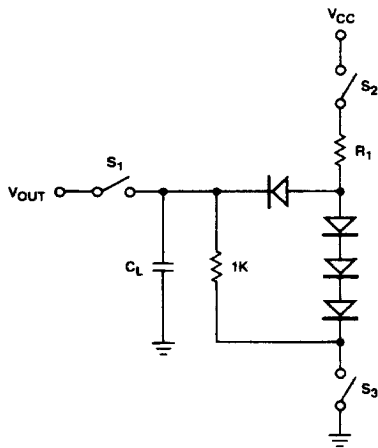
No.	Parameter	For	With Respect To	Delay	Unit
23	Bytes Dequeued Setup	BQ	DQCLK ↑	20	ns
24	Bytes Dequeued Hold	BQ	DQCLK ↑	0	ns
25	Bytes Queued Setup	BQ	QCLK ↓	12	ns
26	Bytes Queued Hold	BQ	QCLK ↑		ns
27	Byte Swap Setup	BSW	QCLK ↑	20	ns
28	Byte Swap Hold	BSW	QCLK ↓		ns
29	Data Setup	D	QCLK ↑	8	ns
30	Data Hold	D	QCLK ↑		ns
31	Data Parity Setup	PD	QCLK ↑	8	ns
32	Data Parity Hold	PD	QCLK ↑		ns
33	Dequeue Enable Setup	QEN	DQCLK ↑	8	ns
34	Dequeue Enable Hold	QEN	DQCLK ↑	0	ns
35	Queue Enable Setup	QEN	QCLK ↓		ns
36	Queue Enable Hold	QEN	QCLK ↑		ns

C. Minimum Clock Requirements

No.	Input	Description	Delay	Unit
37	DQCLK	Dequeue Min. Pulse Width LOW	10	ns
38		Dequeue Min. Pulse Width HIGH	10	
39		Dequeue Min. Cycle Time	80	
40	QCLK	Queue Min. Pulse Width LOW	10	ns
41		Queue Min. Pulse Width HIGH	10	
42		Queue Min. Cycle Time	80	

Notes: 1. Case temperature (T_C) = 0 to +85°C, supply voltage (V_{CC}) = 5 V ± 5%. It is the responsibility of the user to maintain a case temperature of +85°C or less. AMD recommends an air velocity of at least 200 linear feet per minute over the heatsink.

SWITCHING TEST CIRCUITS

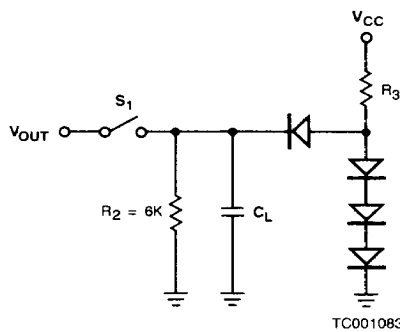


TC001102

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}}$$

A. Three-State Outputs

- Notes:
1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
 2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
 3. S_1 and S_3 are closed while S_2 is open for t_{pZH} test.
 S_1 and S_2 are closed while S_3 is open for t_{pZL} test.
 4. $C_L = 5.0$ pF for output disable tests.



TC001083

$$R_2 = \frac{2.4 \text{ V}}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}}$$

B. Normal Outputs

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown in the data sheet.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily. Current level may vary from product to product.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0$ V and $V_{IH} \geq 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench set up are used to predict the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In

these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH} , I_{OL} , for example) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.

7. Threshold Testing

The noise associated with automatic testing (due to the long, inductive cables), and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.

8. AC Testing

Occasionally parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

9. Output Short-Circuit Current Testing

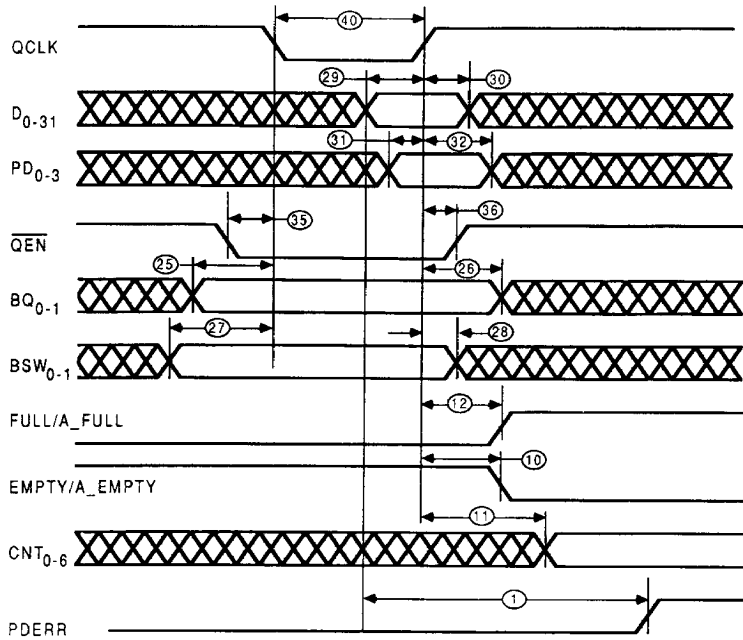
When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, $V_{CC} = \text{Max.}$ case.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

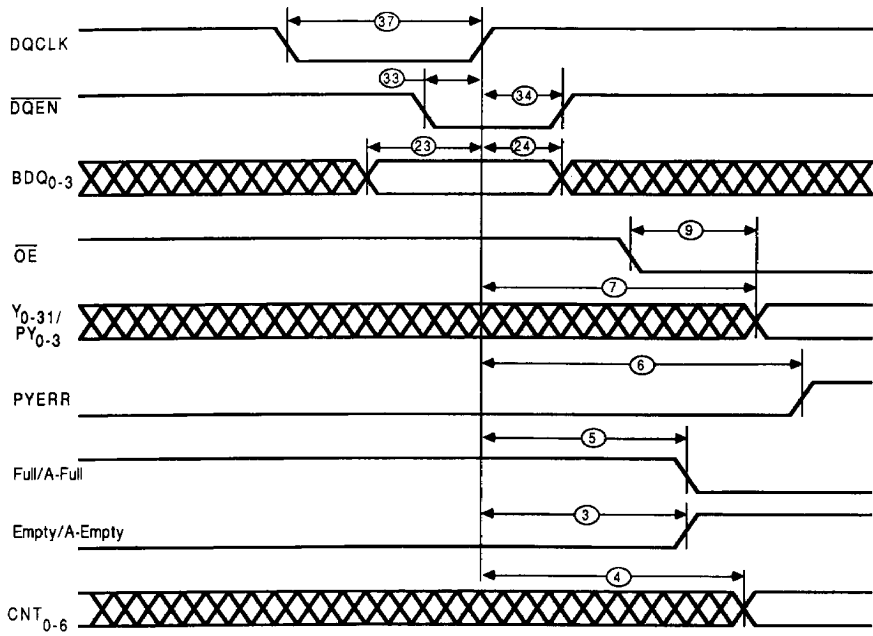
KS000010



WF023460

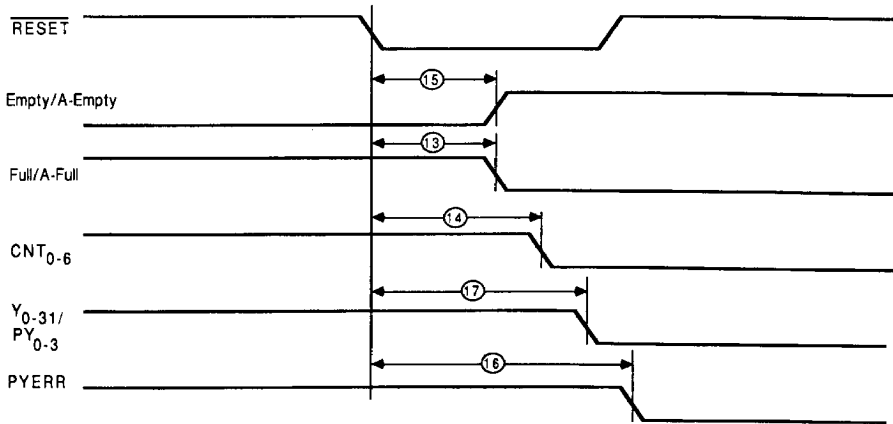
Queue Cycle

SWITCHING WAVEFORMS (Cont'd.)



WF023471

Dequeue Cycle

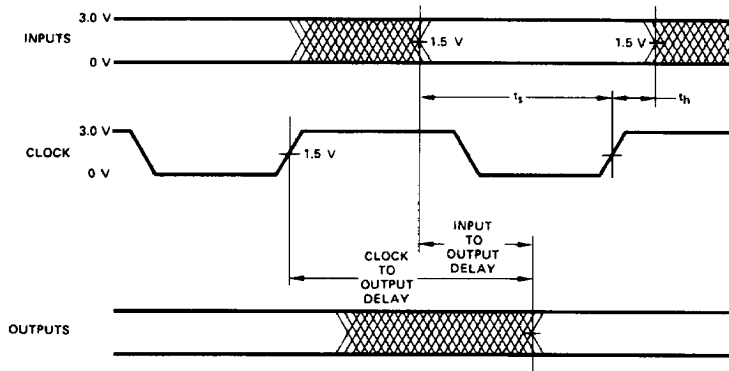


WF023481

RESET Timing Diagram

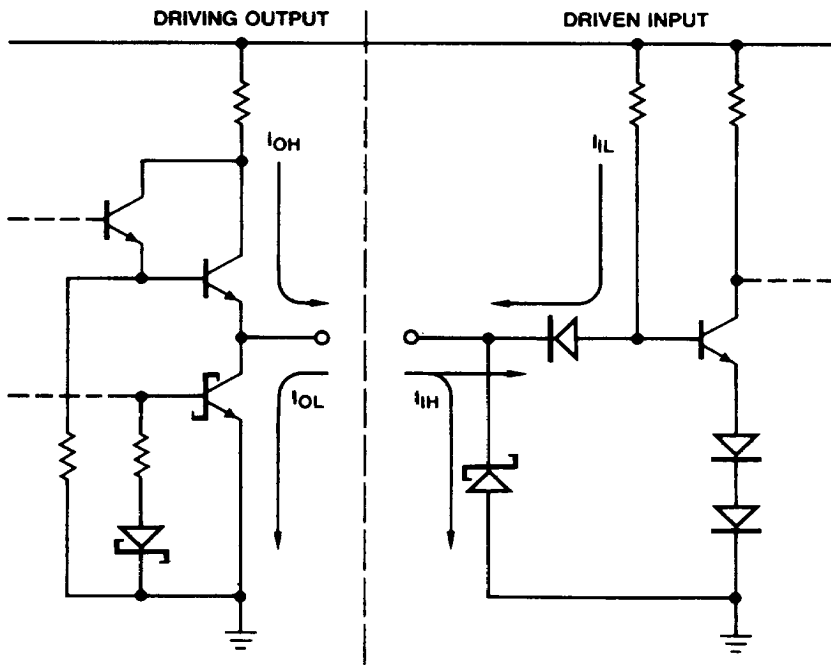
- Notes: 1. Minimum time $\overline{\text{RESET}}$ must be asserted.
 2. This timing diagram is applicable to $\overline{\text{RXMIT}}$.

SWITCHING WAVEFORMS (Cont'd.)



WFR02990

INPUT/OUTPUT CIRCUIT DIAGRAM



ICR00480