1 PRODUCT OVERVIEW

OVERVIEW

The KS57C5532/P5532 single-chip CMOS microcontroller has been designed for high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers). The KS57P5532 is a microcontroller which has 32-kbyte one-time-programmable EPROM but its functions are same to KS57C5532.

With its DTMF generator, 8-bit serial I/O interface, and versatile 8-bit timer/counters, the KS57C5532/P5532 offers an excellent design solution for a wide variety of telecommunication applications.

Up to 55 pins of the 64-pin SDIP or QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events. In addition, the KS57C5532/P5532's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

DEVELOPMENT SUPPORT

The Samsung Microcontroller Development System, SMDS, provides you with a complete PC-based development environment for KS57-series microcontrollers that is powerful, reliable, and portable. In addition to its window-based program development structure, the SMDS toolset includes versatile debugging, trace, instruction timing, and performance measurement applications.

The Samsung Generalized Assembler (SAMA) has been designed specifically for the SMDS environment and accepts assembly language sources in a variety of microprocessor formats. SAMA generates industry-standard hex files that also contain program control data for SMDS compatibility.

FEATURES SUMMARY

Memory

- 1 K × 4-bit RAM
- 32 K × 8-bit ROM

55 I/O Pins

- Input only: 4 pins
- I/O: 43 pins
- N-channel open-drain I/O (S/W): 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

DTMF Generator

- 16 dual-tone frequencies for tone dialing

8-bit Basic Timer

- Programmable internal timer
- Watchdog timer

Two 8-bit Timer/Counters

- Programmable interval timer
- External event counter function
- Timer/counters clock outputs to TCLO0 and TCLO1 pins
- External clock signal divider
- Serial I/O interface clock generator

Watch Timer

- Time interval generation: 0.5 s, 3.9 ms at 32.768 kHz
- 4 frequency outputs to the BUZ pin

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable

Bit Sequential Carrier

- Supports 8-bit serial data transfer in arbitrary format

Interrupts

- 3 external interrupt vectors
- 4 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: Main system clock stops
- Subsystem clock stop mode

Oscillation Sources

- Crystal, ceramic for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency: 3.579545 MHz (typical)
- Subsystem clock frequency: 32.768 kHz (typical)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 µs at 6.0 MHz
- 1.12, 2.23, 17.88 µs at 3.579545 MHz
- 122 µs at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (at 3 MHz)
- 2.7 V to 5.5 V (at 6 MHz)

Package Types

- 64 SDIP, 64 QFP

BLOCK DIAGRAM

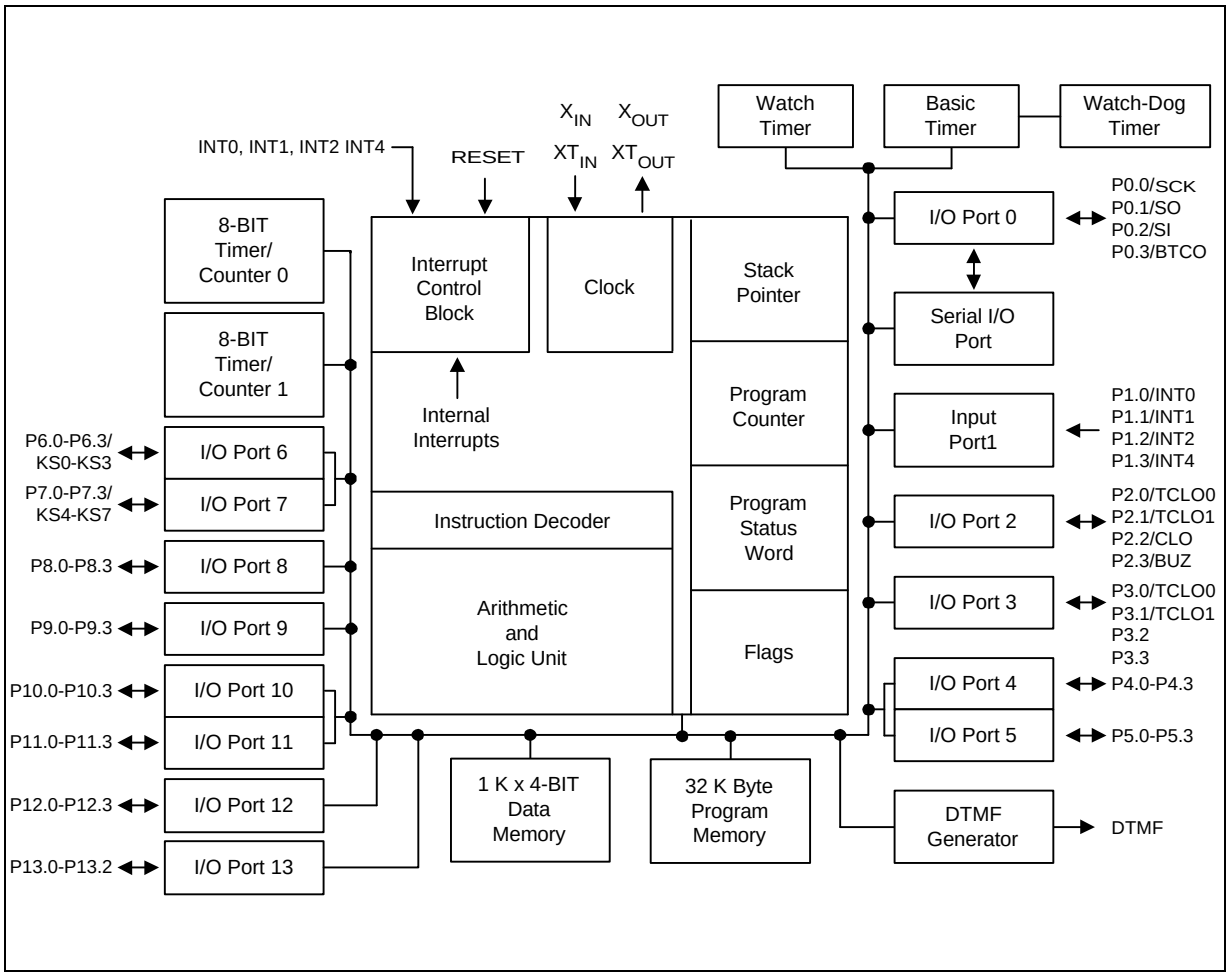


Figure 1-1. KS57C5532/P5532 Simplified Block Diagram

PIN ASSIGNMENTS

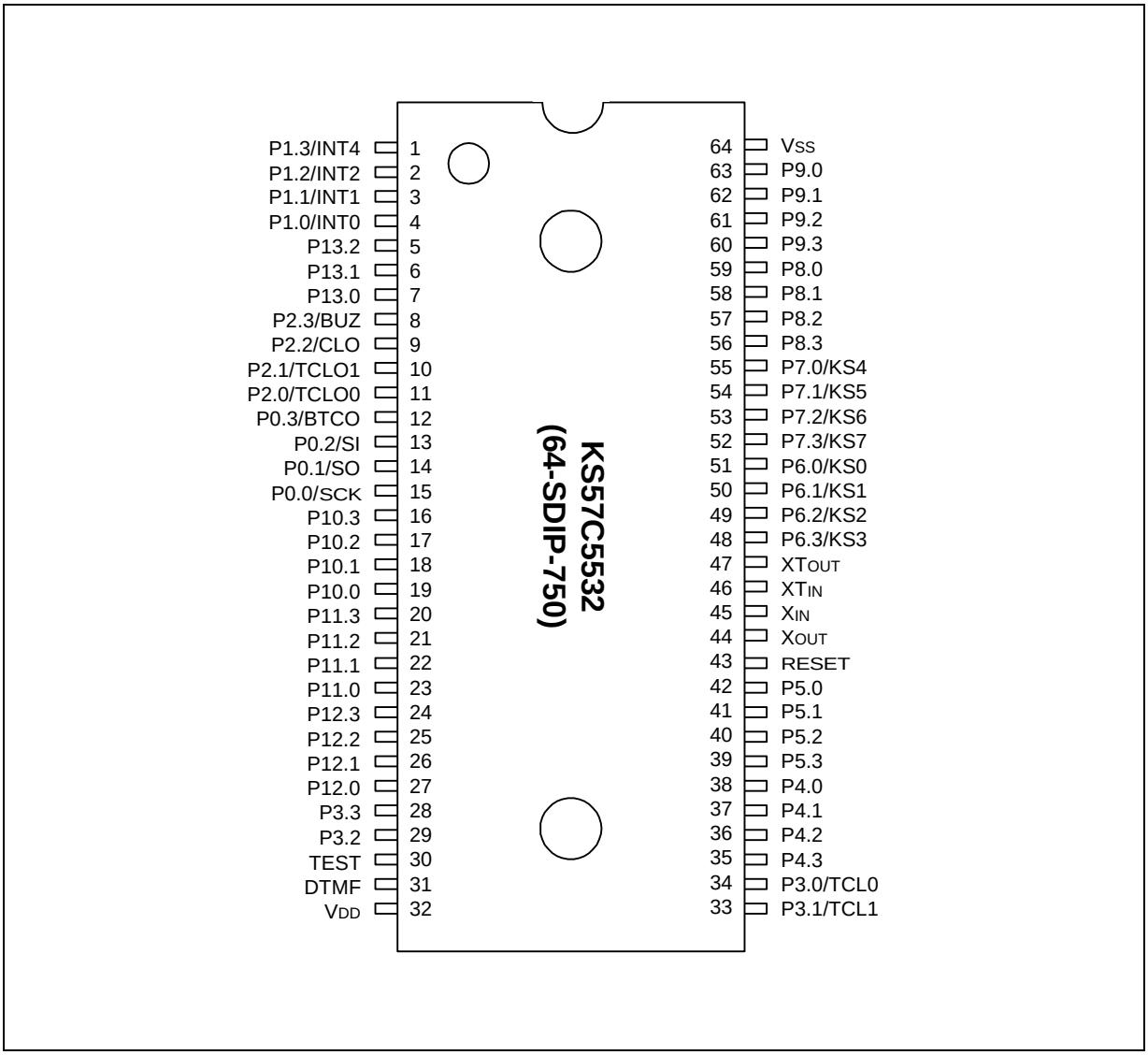


Figure 1-2. KS57C5532/P5532 Pin Assignment Diagrams

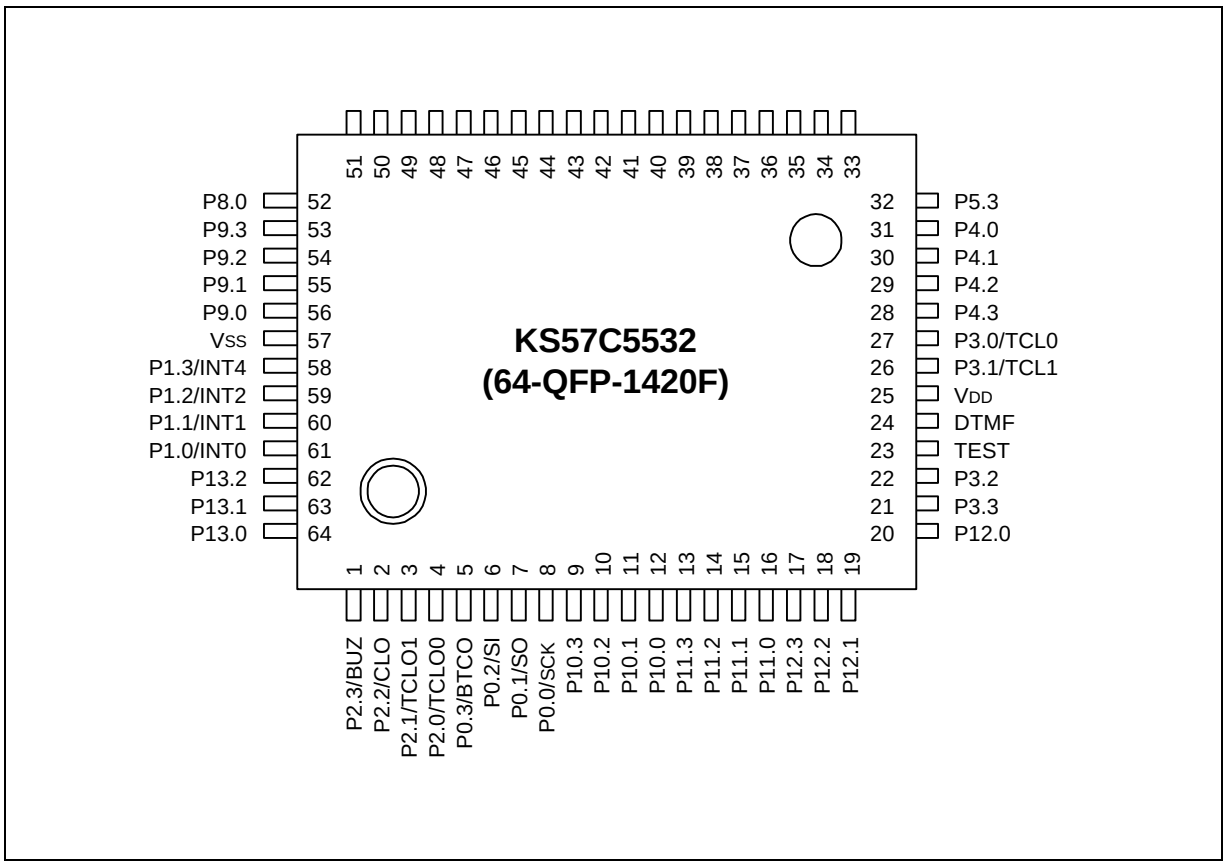


Figure 1-2. KS57C5532/P5532 Pin Assignment Diagrams (Continued)

PIN DESCRIPTIONS

Table 1-1. KS57C5532/P5532 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	15 (8) 14 (7) 13 (6) 12 (5)	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 4-bit pull-up resistors are assignable by software to port 1.	1 (61) 2 (60) 3 (59) 4 (58)	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	11 (4) 10 (3) 9 (2) 8 (1)	TCLO0 TCLO1 CLO BUZ
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	34 (27) 33 (26) 29 (22) 28 (21)	TCL0 TCL1 SCLK (1) SDAT (1)
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable to input pins and are automatically disable for output pins. N-channel open-drain or push-pull output can be selected by software. Port 4 and 5 can be paired to support 8-bit data transfer.	38–35 (31–28) 42–39 (35–32)	–
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Port 6 pins are individually software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	51–48 (44–41) 55–52 (48–45)	KS0–KS3 KS4–KS7
P8.0–P8.3	I/O	Same as port 0.	59–56 (52–49)	–
P9.0–P9.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	63–60 (56–53)	–

NOTES

1. SCLK and SDAT are used for KS57P5532 only.
2. Parentheses indicate pin number for 64 QFP package.

Table 1-1. KS57C5532/P5532 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
P10.0–P10.3 P11.0–P11.3	I/O	Same as port 9. Ports 10 and 11 can be paired to support 8-bit data transfer.	19–16 (12–9) 23–20 (16–13)	–
P12.0–P12.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit *pull-down* resistors are software assignable; pull-down resistors are automatically disabled for output pins.	27–24 (20–17)	–
P13.0–P13.2	I/O	3-bit I/O port; characteristics are same as port 9.	7–5 (64–62)	–
DTMF	O	DTMF output.	31 (24)	–
SCK	I/O	Serial I/O interface clock signal	15 (8)	P0.0
SO	I/O	Serial data output	14 (7)	P0.1
SI	I/O	Serial data input	13 (6)	P0.2
BTCO	I/O	Basic timer clock output	12 (5)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. INT0 is synchronized to system clock.	4, 3 (61, 60)	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	2 (59)	P1.2
INT4	I	External interrupt with detection of rising and falling edges.	1 (58)	P1.3
TCLO0	I/O	Timer/counter 0 clock output	11 (4)	P2.0
TCLO1	I/O	Timer/counter 1 clock output	10 (3)	P2.1
CLO	I/O	Clock output	9 (2)	P2.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at the watch timer clock frequency of 32.768 kHz for buzzer sound	8 (1)	P2.3
TCL0	I/O	External clock input for timer/counter 0	34 (27)	P3.0
TCL1	I/O	External clock input for timer/counter 1	33 (26)	P3.1
KS0–KS3 KS4–KS7	I/O	Quasi-interrupt inputs with falling edge detection	51–48 (44–41) 55–52 (48–45)	P6.0–P6.3 P7.0–P7.3

NOTE: Parentheses indicate pin number for 64 QFP package.

Table 1-1. KS57C5532/P5532Pin Descriptions (Concluded)

Pin Name	Pin Type	Description	Number	Share Pin
V_{DD}	–	Power supply	32 (25)	–
V_{SS}	–	Ground	64 (57)	–
RESET	I	Reset signal	43 (36)	–
X_{IN}, X_{OUT}	–	Crystal, ceramic, or R/C oscillator signal for main system clock. (For external clock input, use X_{IN} and input X_{IN}'s reverse phase to X_{OUT})	45, 44 (38, 37)	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator signal for subsystem clock. (For external clock input, use XT_{IN} and input XT_{IN}'s reverse phase to XT_{OUT})	46, 47 (39, 40)	–
TEST	–	Chip test input pin. Hold GND when the device is operating.	30 (23)	–

NOTE: Parentheses indicate pin number for 64 QFP package.

Table 1-2. Overview of KS57C5532/P5532 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	D-4
P1.0–P1.3	INT0, INT1, INT2, INT4	I	Input	A-1
P2.0–P2.3	TCLO0, TCLO1, CLO, BUZ	I/O	Input	D-2
P3.0–P3.1	TCL0, TCL1	I/O	Input	D-4
P3.2–P3.3	–	I/O	Input	D-2
P4.0–P4.3 P5.0–P5.3	–	I/O	Input	E-2
P6.0–P6.3 P7.0–P7.3	KS0–KS3 KS4–KS7	I/O	Input	D-4
P8.0–P8.3	–	I/O	Input	D-2
P9.0–P9.3	–	I/O	Input	D-2
P10.0–P10.3 P11.0–P11.3	–	I/O	Input	D-2
P12.0–P12.3	–	I/O	Input	D-6
P13.0–P13.2	–	I/O	Input	D-2
DTMF	–	O	High impedence	G-6
X_{IN}, X_{OUT} XT_{IN}, XT_{OUT}	–	–	–	–
RESET	–	I	–	B
NC	–	–	–	–
V_{DD}, V_{SS}	–	–	–	–

PIN CIRCUIT DIAGRAMS

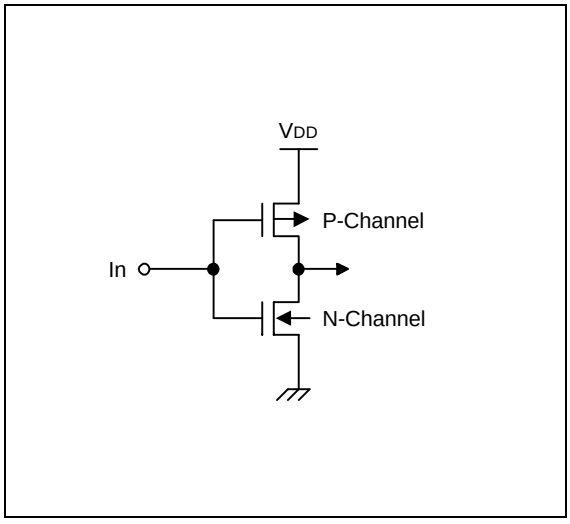


Figure 1-3. Pin Circuit Type A

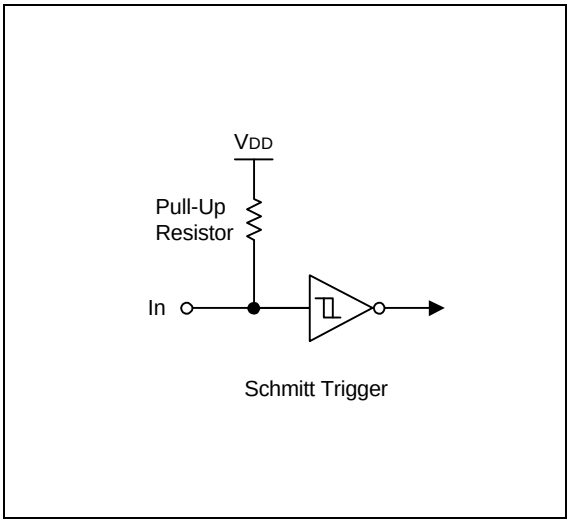


Figure 1-5. Pin Circuit Type B

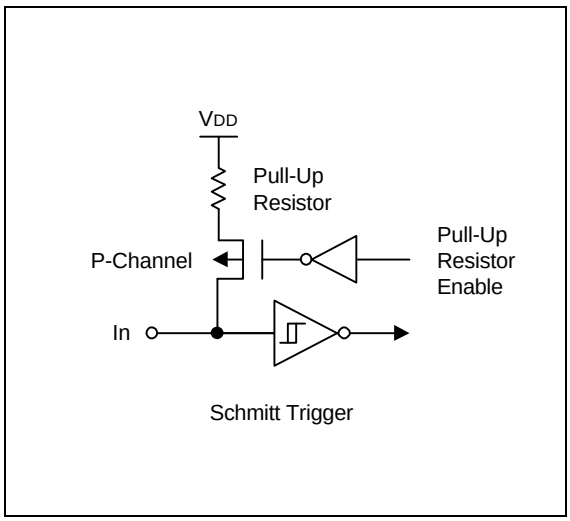


Figure 1-4. Pin Circuit Type A-1

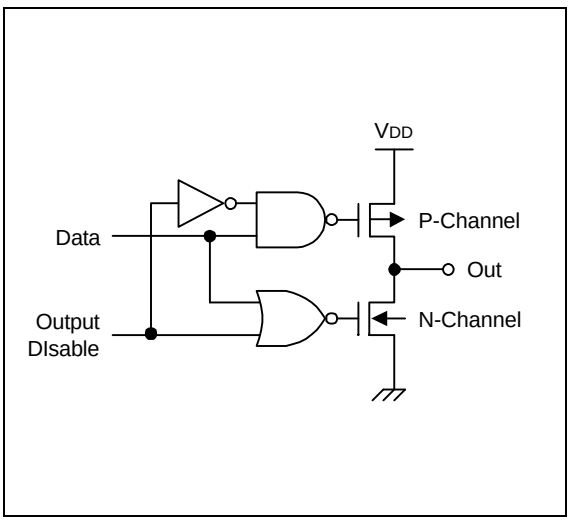


Figure 1-6. Pin Circuit Type C

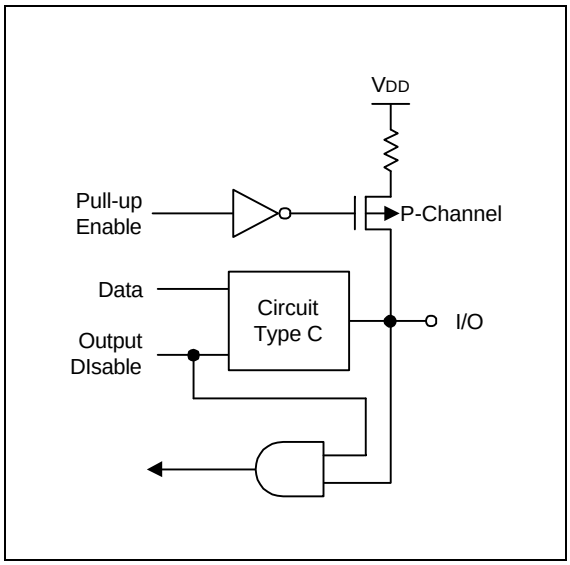


Figure 1-7. Pin Circuit Type D-2

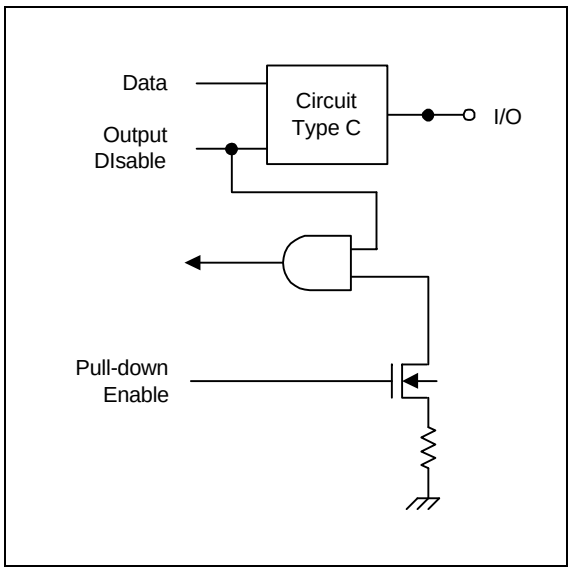


Figure 1-9. Pin Circuit Type D-6

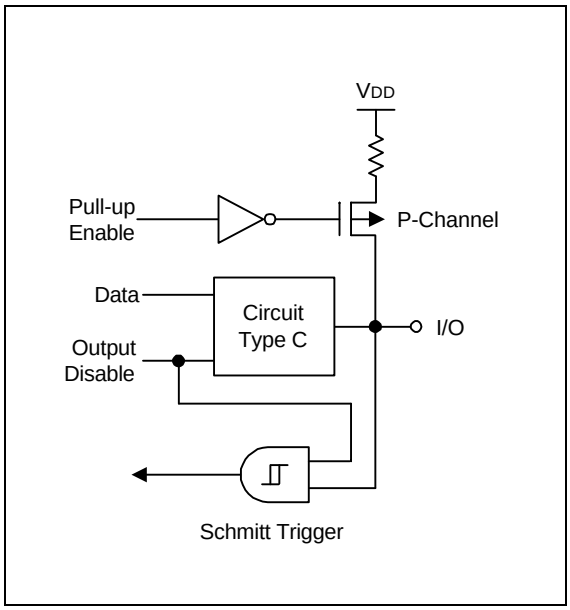


Figure 1-8. Pin Circuit Type D-4

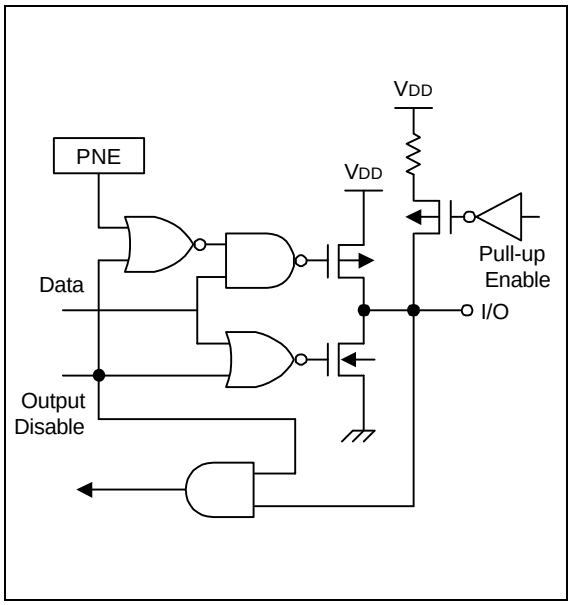
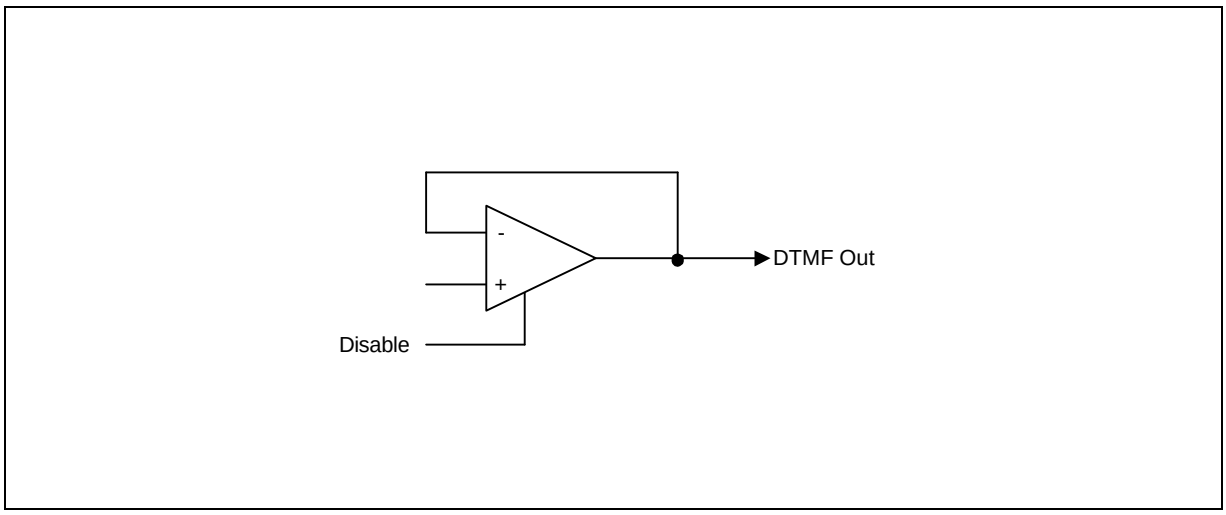


Figure 1-10. Pin Circuit Type E-2


-
+
DTMF Out
Disable

14 ELECTRICAL DATA

OVERVIEW

In this section, information on KS57C5532 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— System clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{IN} and X_{OUT}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts
— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value)	mA
			+ 15 (note)	
		All I/O ports, total	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH4}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 3, 6, 7, and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}		V_{DD}	
	V_{IH4}	X_{IN}, X_{OUT} and XT_{IN}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 3, 6, 7, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT} and XT_{IN}			0.1	

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OH}	I_{OH} = – 1 mA Ports except 1	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4,5 only	–	–	2	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6mA		–	0.4	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 4mA all out Ports except ports 4,5			2	V
		V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6mA			0.4	V
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{IN}, X_{OUT} and XT_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except below and RESET	–	–	- 3	µA
	I_{LIL2}	V_I = 0 V X_{IN}, X_{OUT} and XT_{IN}			- 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	- 3	
Pull-Up Resistor	R_{L1}	V_{DD} = 5 V; V_I = 0 V except RESET	25	45	100	kΩ
		V_{DD} = 3 V	50	89	200	
	R_{L3}	V_{DD} = 5 V; V_I = 0 V; RESET	100	212	400	
		V_{DD} = 3 V	200	441	800	
Pull-Down Resistor	R_{L4}	V_{DD} = 5 V; $V_I = V_{DD}$; Port 12	25	46	100	
		V_{DD} = 3 V	50	95	200	

Table 14-2. D.C. Electrical Characteristics (Concluded)

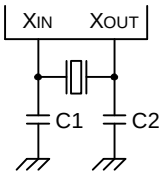
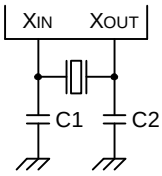
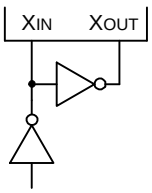
(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (DTMF ON)	Run mode; V_{DD} = 5.0 V ± 10% 3.58 MHz Crystal oscillator; C1 = C2 = 22 pF		–	3.0	5.0	mA
		V_{DD} = 3 V ± 10%			1.6	3.0	
	I_{DD2} (DTMF OFF)	Run mode; V_{DD} = 5.0 V ± 10% Crystal oscillator; C1 = C2 = 22 pF	6.0 MHz		2.7	8.0	
			3.58 MHz		2.0	4.0	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.3	4.0	
			3.58 MHz		0.9	2.3	
	I_{DD3}	Idle mode; V_{DD} = 5 V ± 10%	6.0 MHz		0.8	2.5	
			3.58 MHz		0.7	1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.3	1.5	
			3.58 MHz		0.2	1.0	
	I_{DD4}	Run mode; V_{DD} = 3.0 V ± 10% 32 kHz Crystal oscillator		–	12.5	30	µA
	I_{DD5}	Idle mode; V_{DD} = 3.0 V ± 10% 32 kHz Crystal oscillator			4.5	15	
	I_{DD6}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT = 0V	–	1.9	5	
		Stop mode; V_{DD} = 3 V ± 10%			0.6	3	
		Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2	
Row Tone Level (2)	V_{ROW}	V_{DD} = 2.0 V to 5.5 V R_L =12 KΩ; Temp = – 30 to 60 °C		– 16	– 14	– 11	dBV
Ratio of Column to Row Tone (2)	dB_{CR}	V_{DD} = 2.0 V to 5.5 V R_L = 12 KΩ; Temp = – 30 to 60 °C		1	2	3	dB
Distortion (2) (Dual tone)	THD	V_{DD} = 2.0 V to 5.5 V 1 MHz band, R_L = 12 KΩ Temp = – 30 to 60 °C		–	–	5	%

NOTES:
1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resistors.
2. DTMF electrical characteristics.
3. For D.C. electrical values, the power control register (PCON) must be set to 0011B.

Table 14-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V_{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		Stabilization time (2)	V_{DD} = 3 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3	
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES:
1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Recommended Oscillator Constants

(T_A = – 40 °C to + 85 °C)

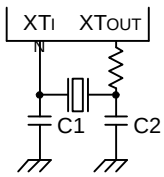
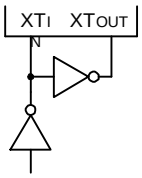
Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:

1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 14-5. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 5.5 V	–	–	10	s
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XH}, t_{XL})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs or when stop mode is terminated.

Table 14-6. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 14-7. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

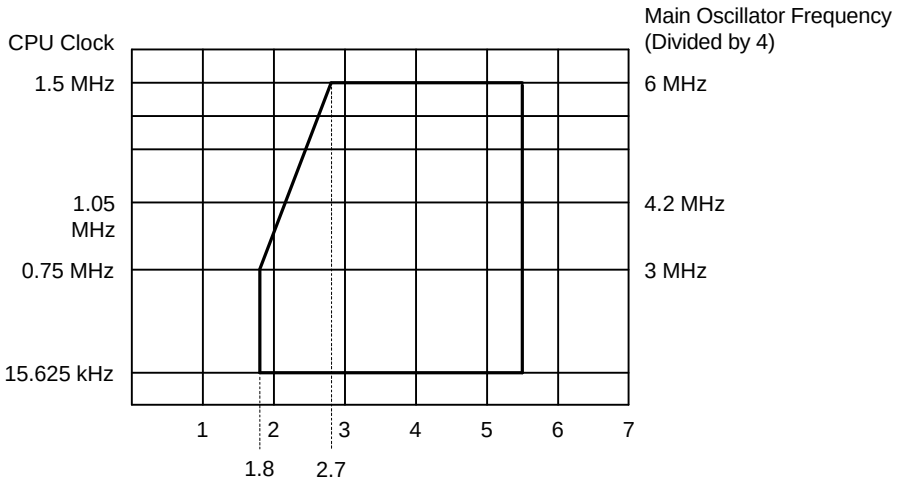
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	1.33			
TCL0, TCL1 Input Frequency	f_{TI0}, f_{TI1}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5 V			1	MHz
TCL0, TCL1 Input High, Low Width	t_{TIH0}, t_{TIL0} t_{TIH1}, t_{TIL1}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK Cycle Time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	670			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK High, Low Width	t_{KH}, t_{KL}	V_{DD} = 2.7 V to 5.5 V External SCK source	335	–	–	ns
		Internal SCK source	t_{KCY}–250			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	t_{KCY}–2150			
SI Setup Time to SCK High	t_{SIK}	V_{DD} = 2.7 V to 5.5 V External SCK source	100	–	–	ns
		Internal SCK source	150			
		V_{DD} = 1.8 V to 5.5 V External SCK source	150			
		Internal SCK source	500			
SI Hold Time to SCK High	t_{KSI}	V_{DD} = 2.7 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	400			
		V_{DD} = 1.8 V to 5.5 V External SCK source	600			
		Internal SCK source	500			

Table 14-7. A.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Delay for SCK to SO	t_{KSO} (note)	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	INT0, INT1, INT2, INT4, KS0–KS7	10	–	–	µs
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: R (1 kΩ) and C (100 pF) are the load resistance and load capacitance of the SO output line.



CPU Clock = 1/n x oscillator frequency (n = 4, 8 or 64)

Figure 14-1. Standard Operating Voltage Range

Table 14-8. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.5 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	ms

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

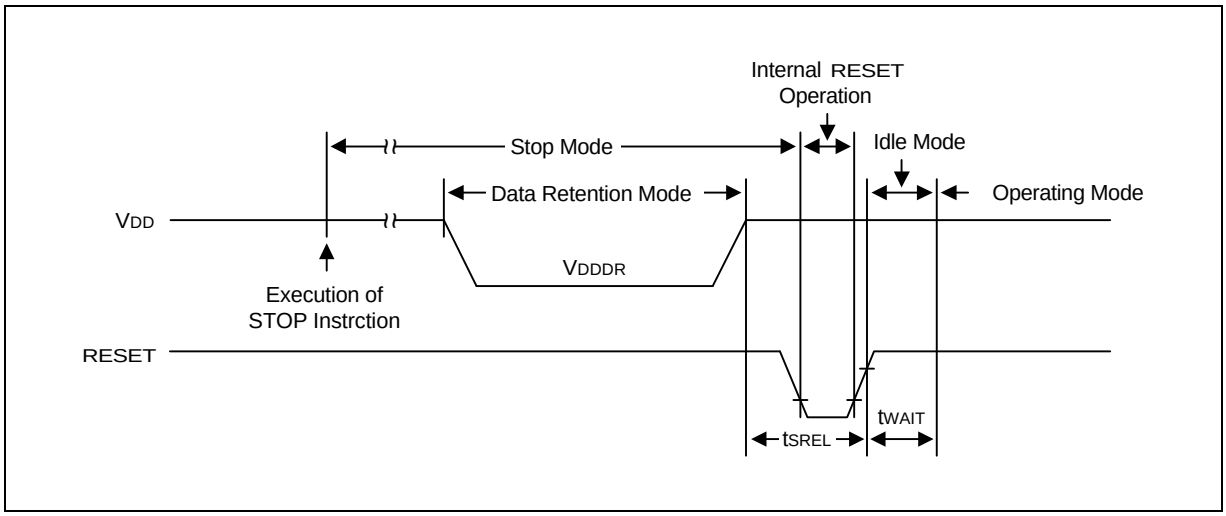


Figure 14-2. Stop Mode Release Timing When Initiated by RESET

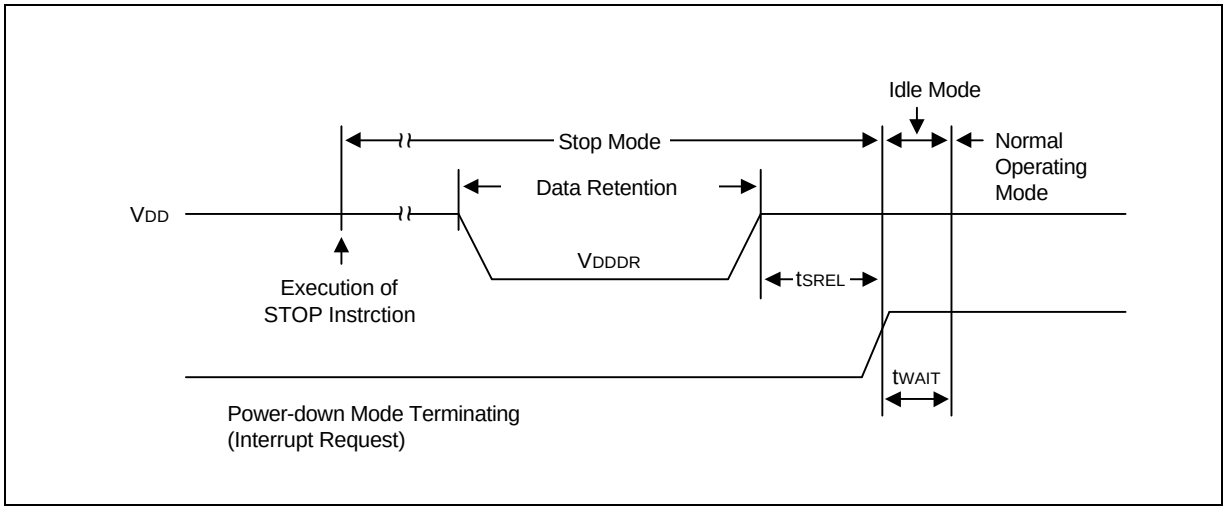


Figure 14-3. Stop Mode Release Timing When Initiated by Interrupt Request

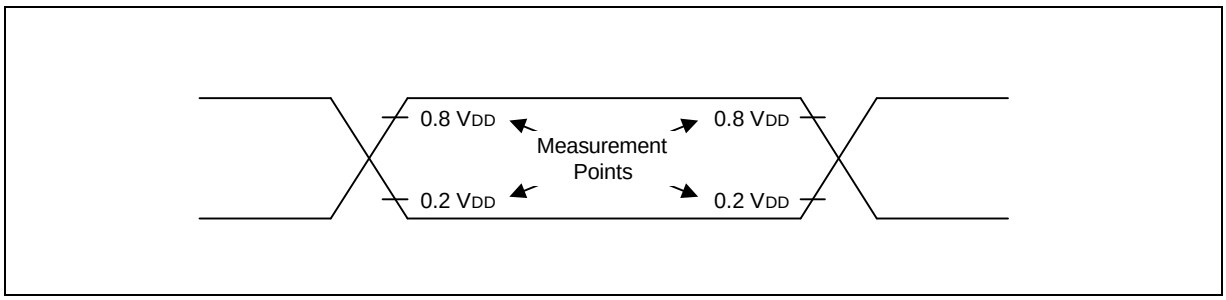


Figure 14-4. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

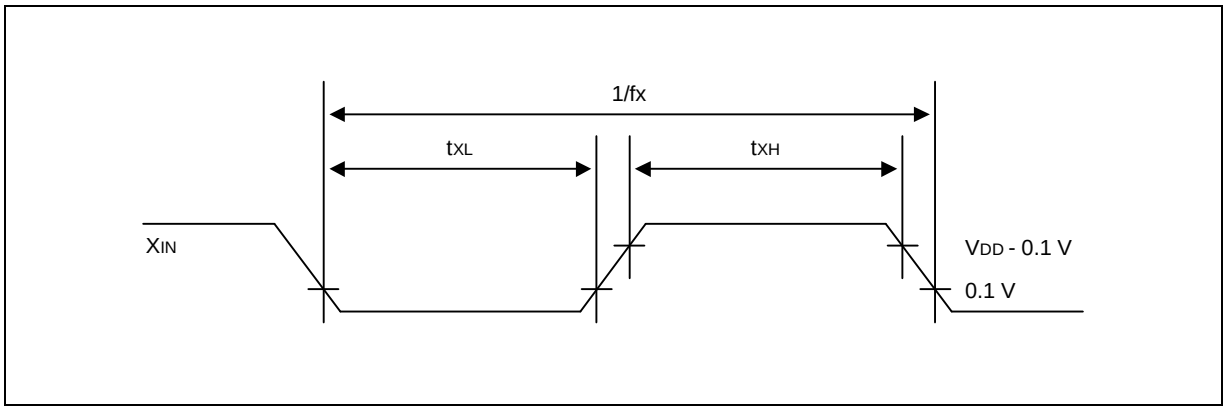


Figure 14-5. Clock Timing Measurement at X_{IN} (XT_{IN})

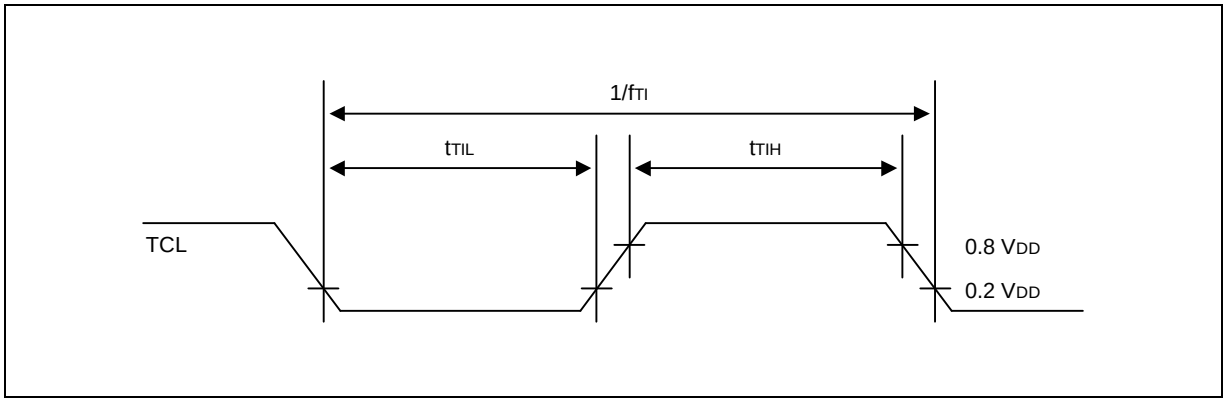


Figure 14-6. TCL0/1 Timing

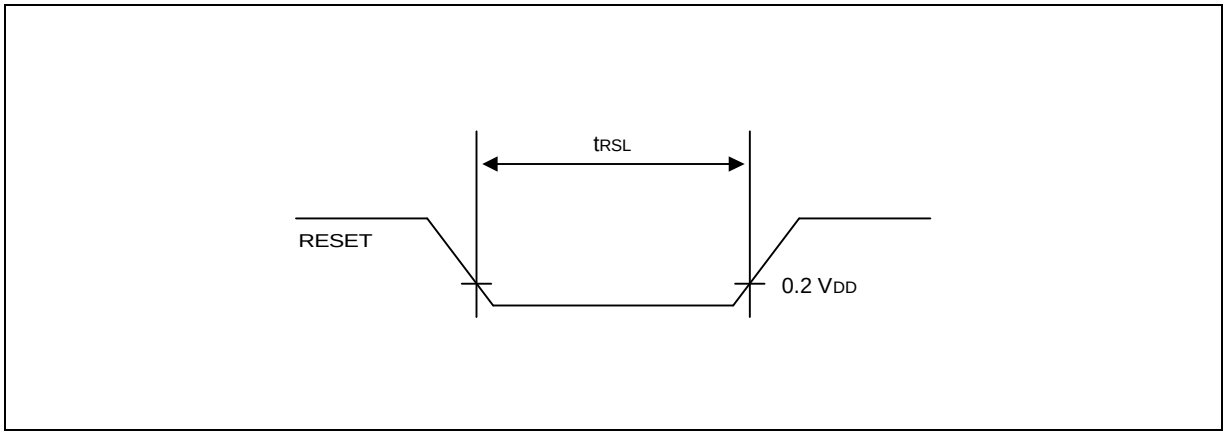


Figure 14-7. Input Timing for RESET Signal

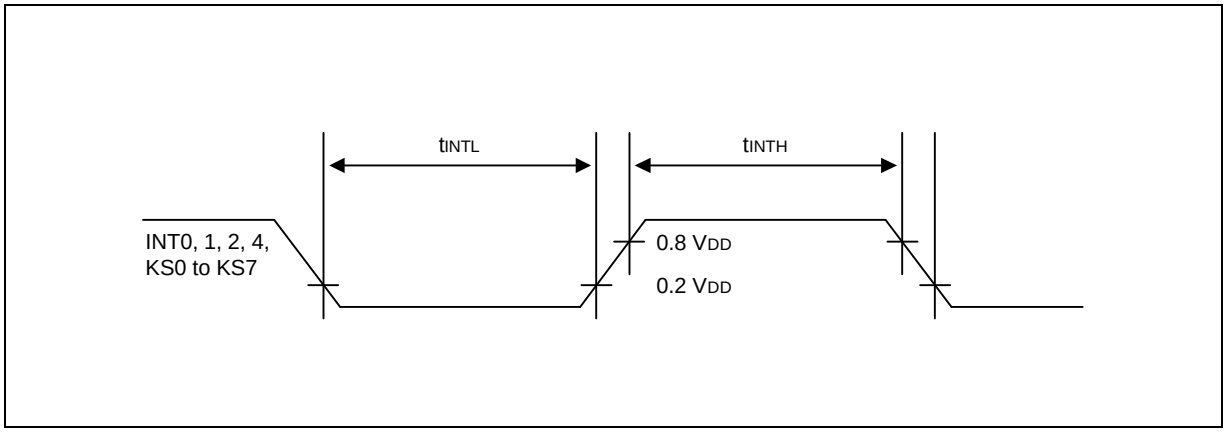


Figure 14-8. Input Timing for External Interrupts and Quasi-Interrupts

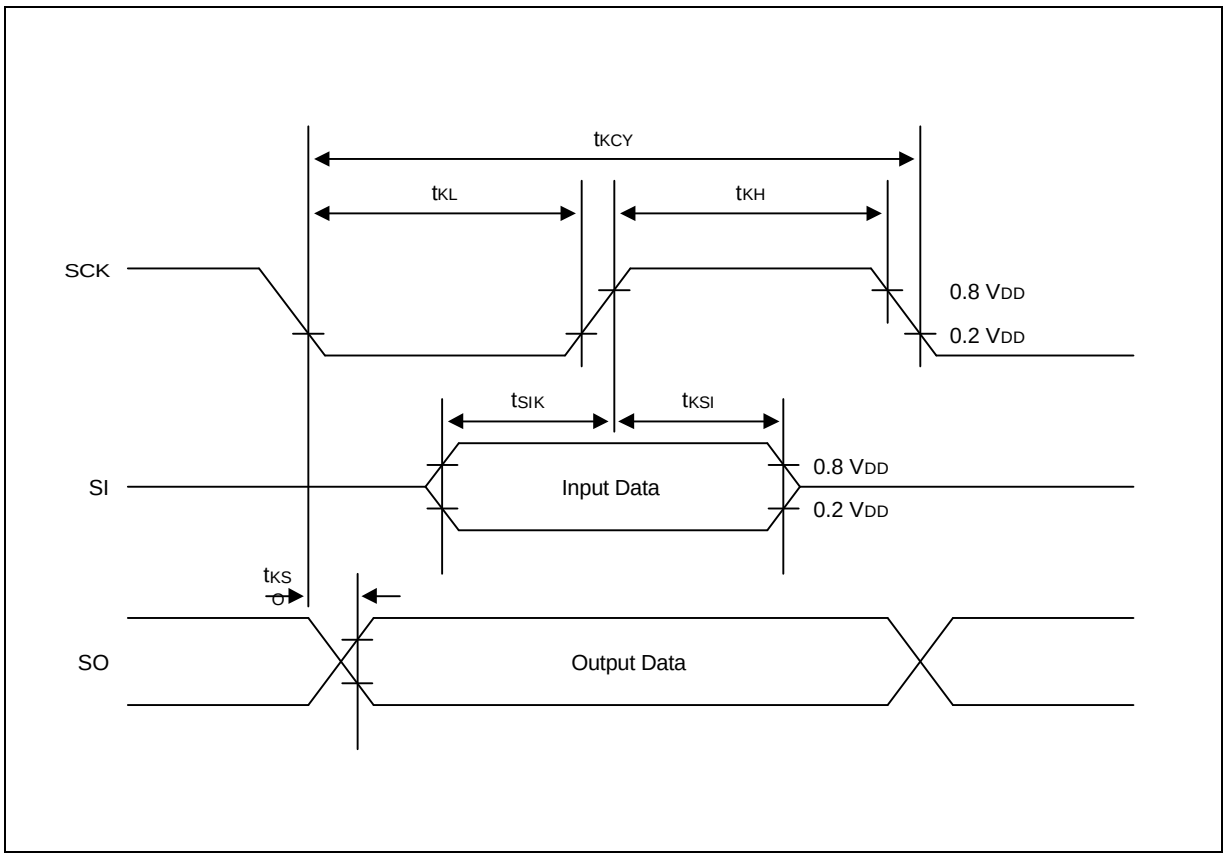


Figure 14-9. Serial Data Transfer Timing

15 MECHANICAL DATA

This section contains the following information about the device package:

— Package dimensions in millimeters

— Pad diagram

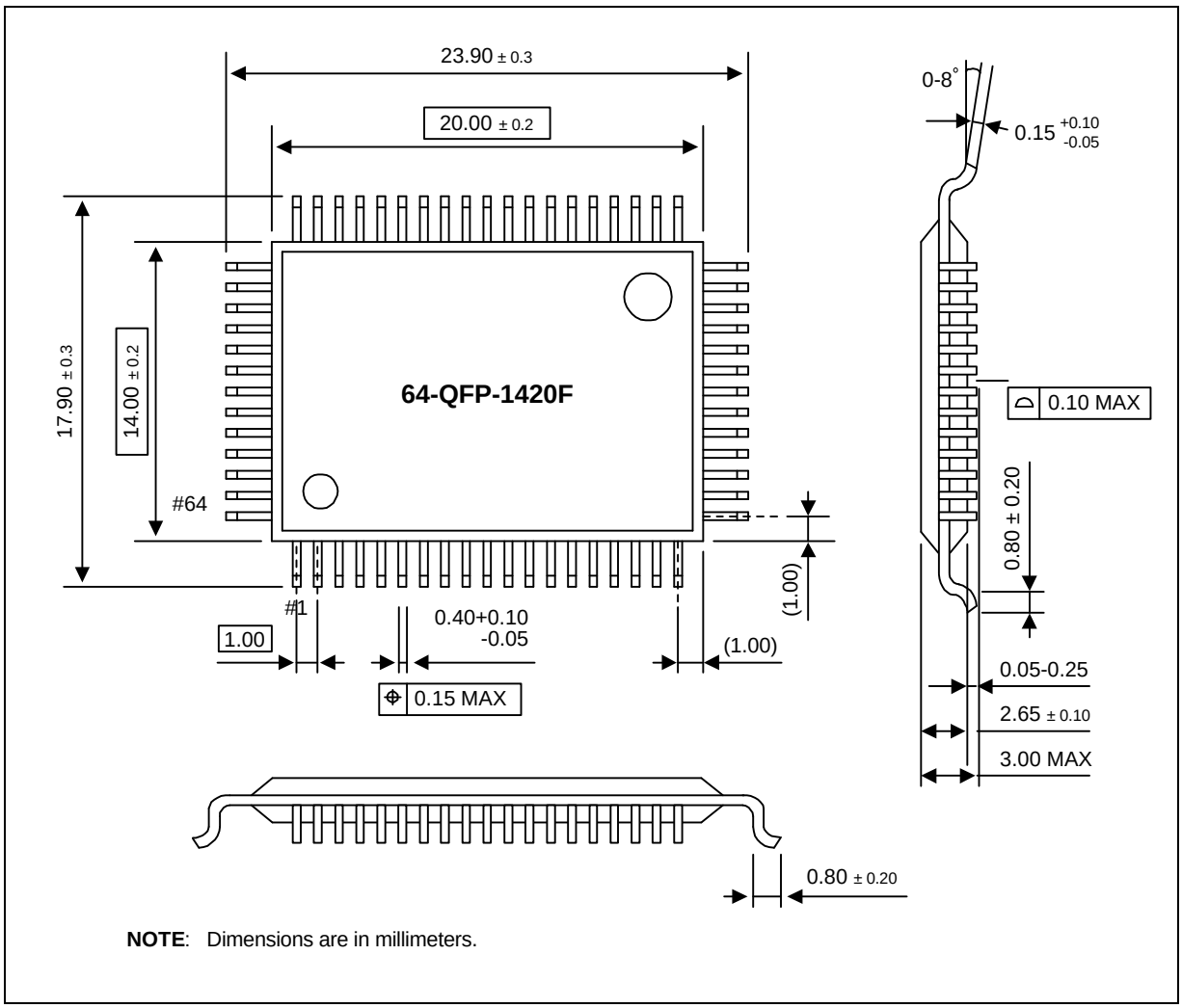
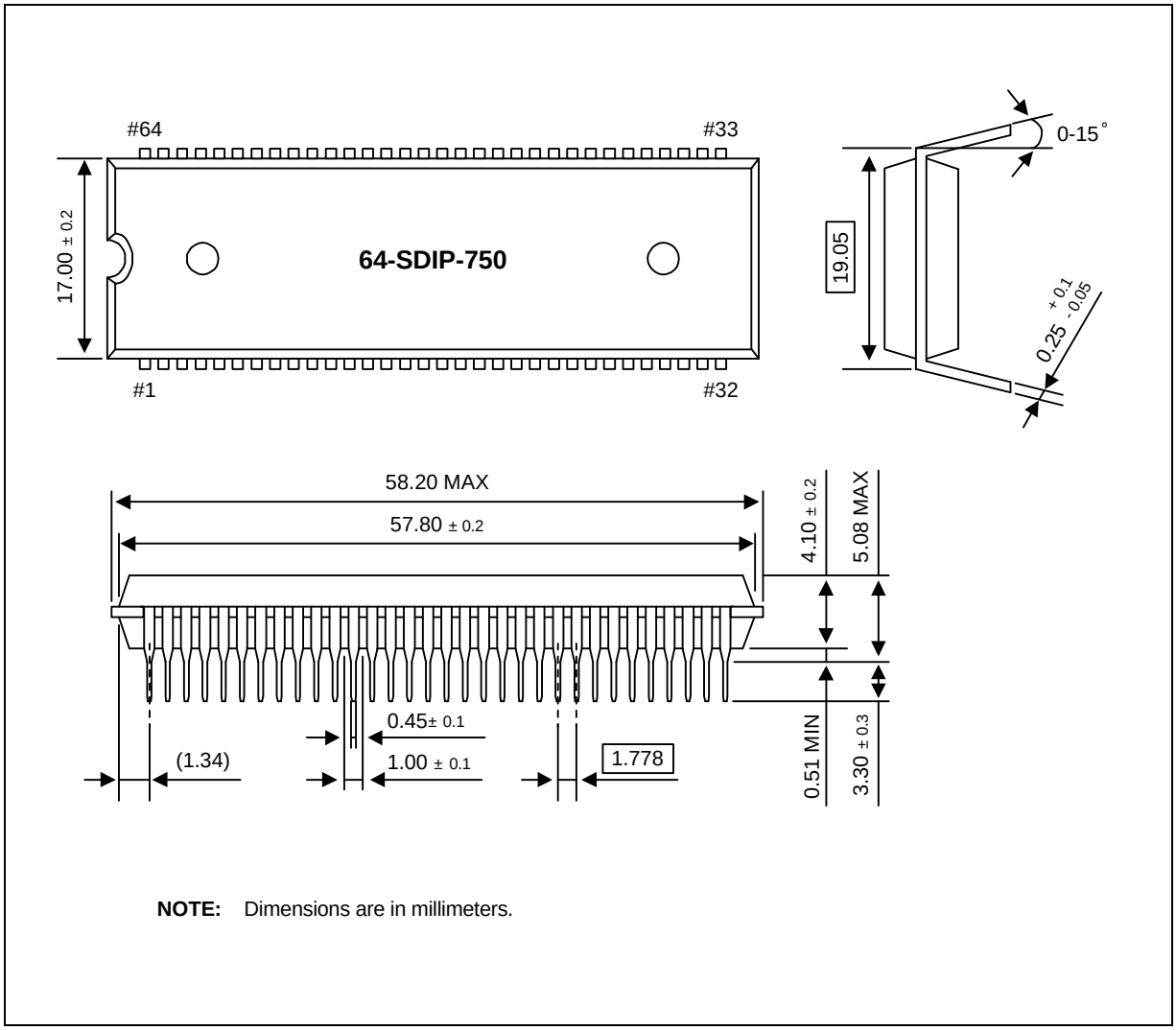


Figure 15-1. 64-QFP-1420F Package Dimensions



NOTE: Dimensions are in millimeters.

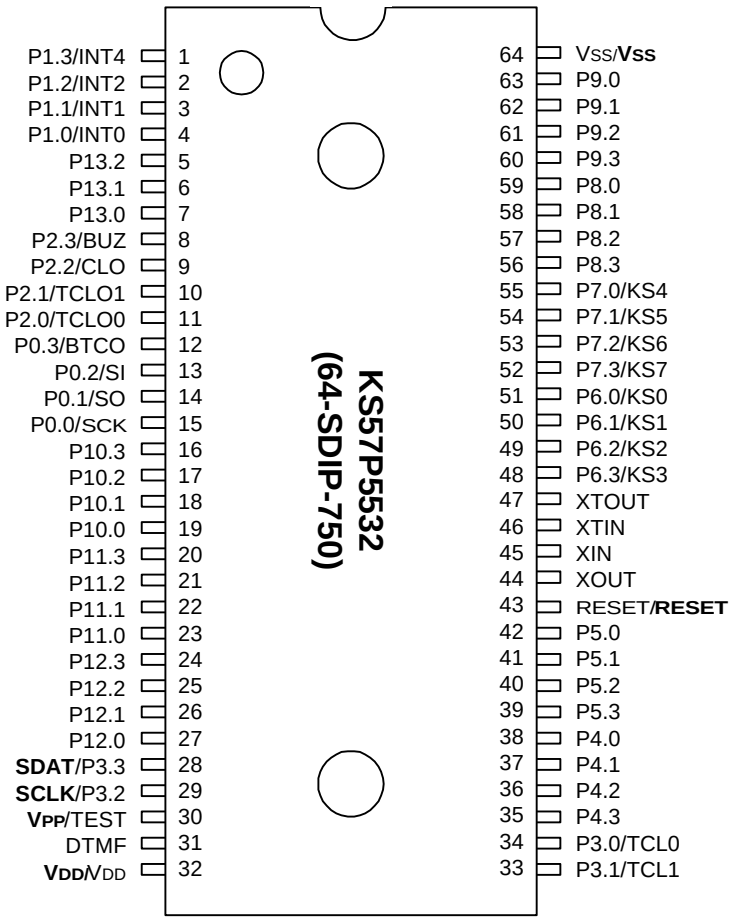
Figure 15-2. 64-SDIP-750C Package Dimensions

16 KS57P5532OTP

OVERVIEW

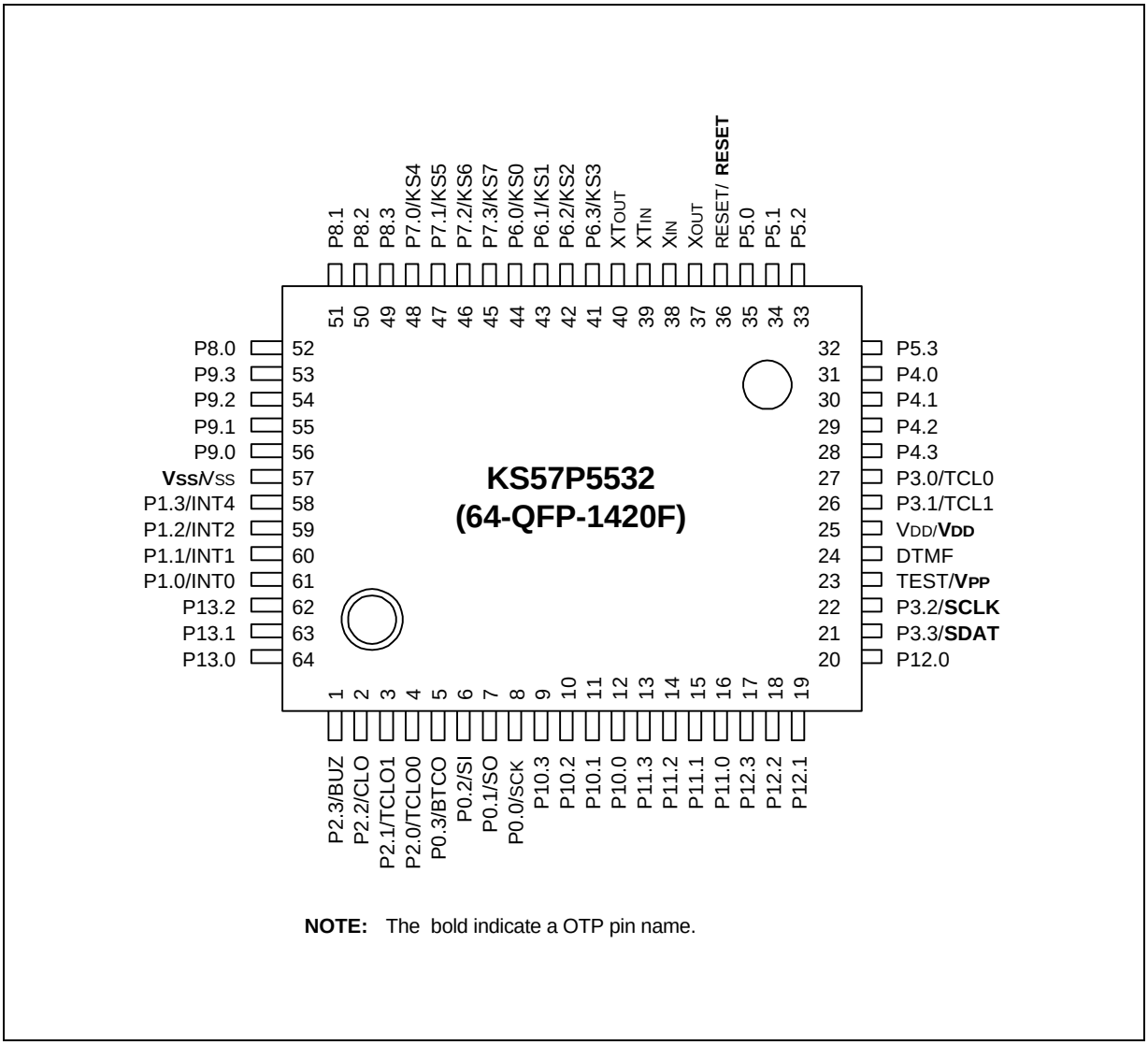
The KS57P5532 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS57C5532 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS57P5532 is fully compatible with the KS57C5532, both in function and in pin configuration. Because of its simple programming requirements, the KS57P5532 is ideal for use as an evaluation chip for the KS57C5532.



NOTE: The bold indicate a OTP pin name.

Figure 16-1. KS57P5532 Pin Assignments (64-SDIP)



NOTE: The bold indicate a OTP pin name.

Figure 16-2. KS57P5532 Pin Assignments (64-QFP)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Pin Name	During Programming		
	Pin No.	I/O	Function
SDAT	28 (21)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
SCLK	29 (22)	I	Serial clock pin. Input only pin.
V_{PP} (TEST)	30 (23)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option) Hold GND when OTP is operating.
RESET	43 (36)	I	Chip initialization
V_{DD}/V_{SS}	32 (25) / 64 (57)	I	Logic power supply pin. V_{DD} should be tied to + 5 V during programming.

NOTE: Parentheses indicate pin number for 64 QFP package.

Table 16-2. Comparison of KS57P5532 and KS57C5532 Features

Characteristic	KS57P5532	KS57C5532
Program Memory	32 K byte EPROM	32 K byte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5V	
Pin Configuration	64 SDIP/QFP	64 SDIP/QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the KS57P5532, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/MEM	Address (A15–A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5V	0	0000H	0	EPROM program
	12.5V	0	0000H	1	EPROM verify
	12.5V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 16-4. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O port active	– 15	mA
		All I/O ports active	– 30	
Output Current Low	I_{OL}	One I/O port active	+ 30 (Peak value)	mA
			+ 15 (note)	
		All I/O ports, total	+ 100 (Peak value)	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 16-5. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except those specified below for V_{IH2}–V_{IH4}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 3, 6, 7, and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}		V_{DD}	
	V_{IH4}	X_{IN}, X_{OUT} and XT_{IN}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except those specified below for V_{IL2}–V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 3, 6, 7, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT} and XT_{IN}			0.1	

Table 16-5. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output High Voltage	V_{OH}	I_{OH} = – 1 mA Ports except 1	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 4,5 only	–	–	2	V
		V_{DD} = 2.0 to 5.5 V, I_{OL} = 1.6mA		–	0.4	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 4mA all out Ports except ports 4,5			2	V
		V_{DD} = 2.0 to 5.5 V, I_{OL} = 1.6mA			0.4	V
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ X_{IN}, X_{OUT} and XT_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except below and RESET	–	–	- 3	µA
	I_{LIL2}	V_I = 0 V X_{IN}, X_{OUT} and XT_{IN}			– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	
Pull-up Resistor	R_{L1}	V_{DD} = 5 V; V_I = 0 V except RESET	25	45	100	kΩ
		V_{DD} = 3 V	50	89	200	
	R_{L3}	V_{DD} = 5 V; V_I = 0 V; RESET	100	212	400	
		V_{DD} = 3 V	200	441	800	
Pull-Down Resistor	R_{L4}	V_{DD} = 5 V ; $V_I = V_{DD}$; Port 12	25	46	100	
		V_{DD} = 3 V	50	95	200	

Table 16-5. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

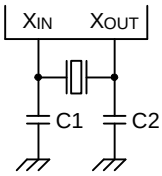
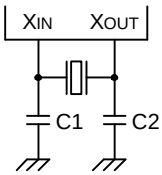
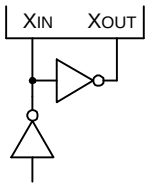
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1)	I_{DD1} (DTMF ON)	Run mode; V_{DD} = 5.0 V ± 10% 3.58 MHz Crystal oscillator; C1 = C2 = 22 pF		–	3.0	5.0	mA
		V_{DD} = 3 V ± 10%			1.6	3.0	
	I_{DD2} (DTMF OFF)	Run mode; V_{DD} = 5.0 V ± 10% Crystal oscillator; C1 = C2 = 22 pF	6.0 MHz		2.7	8.0	
			3.58 MHz		2.0	4.0	
		V_{DD} = 3 V ± 10%	6.0 MHz		1.3	4.0	
			3.58 MHz		0.9	2.3	
	I_{DD3}	Idle mode; V_{DD} = 5 V ± 10%	6.0 MHz		0.8	2.5	
			3.58 MHz		0.7	1.8	
		V_{DD} = 3 V ± 10%	6.0 MHz		0.3	1.5	
			3.58 MHz		0.2	1.0	
	I_{DD4}	Run mode; V_{DD} = 3.0 V ± 10% 32 kHz Crystal oscillator		–	12.5	30	µA
	I_{DD5}	Idle mode; V_{DD} = 3.0 V ± 10% 32 kHz Crystal oscillator			4.5	15	
	I_{DD6}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B	–	1.9	5	
		Stop mode; V_{DD} = 3 V ± 10%	XT = 0 V		0.6	3	
		Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0100B		0.2	3	
		Stop mode; V_{DD} = 3 V ± 10%			0.1	2	
Row Tone Level (2)	V_{ROW}	V_{DD} = 2.0 V to 5.5 V R_L =12 KΩ; Temp = – 30 to 60 °C		– 16	– 14	– 11	dBV
Ratio of Column to Row Tone (2)	dB_{CR}	V_{DD} = 2.0 V to 5.5 V R_L =12 KΩ; Temp = – 30 to 60 °C		1	2	3	dB
Distortion (2) (Dual tone)	THD	V_{DD} = 2.0 V to 5.5 V 1 MHz band, R_L = 12 KΩ Temp = – 30 to 60 °C		–	–	5	%

NOTES:

1. D.C. electrical values for Supply Current (I_{DD1} to I_{DD3}) do not include current drawn through internal pull-up resistors.
2. DTMF electrical characteristics.
3. For D.C. electrical values, the power control register (PCON) must be set to 0011B.

Table 16-6. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		Stabilization time (2)	V_{DD} = 3 V	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		Stabilization time (2)	V_{DD} = 3 V	–	–	10	ms
External Clock		X_{IN} input frequency (1)	V_{DD} = 2.7 V to 5.5 V	0.4	–	6.0	MHz
			V_{DD} = 1.8 V to 5.5 V	0.4	–	3.0	
		X_{in} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	1250	ns

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs, or when stop mode is terminated.

Table 16-7. Recommended Oscillator Constants

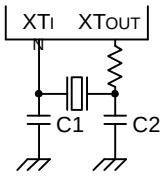
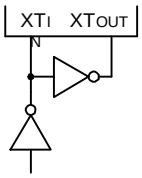
(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Manufacturer	Series Number (1)	Frequency Range	Load Cap (pF)		Oscillator Voltage Range (V)		Remarks
			C1	C2	MIN	MAX	
TDK	FCR ðÿM5	3.58 MHz–6.0 MHz	33	33	2.0	5.5	Leaded Type
	FCR ðÿMC5	3.58 MHz–6.0 MHz	(2)	(2)	2.0	5.5	On-chip C Leaded Type
	CCR ðÿMC3	3.58 MHz–6.0 MHz	(3)	(3)	2.0	5.5	On-chip C SMD Type

NOTES:
1. Please specify normal oscillator frequency.
2. On-chip C: 30pF built in.
3. On-chip C: 38pF built in.

Table 16-8. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

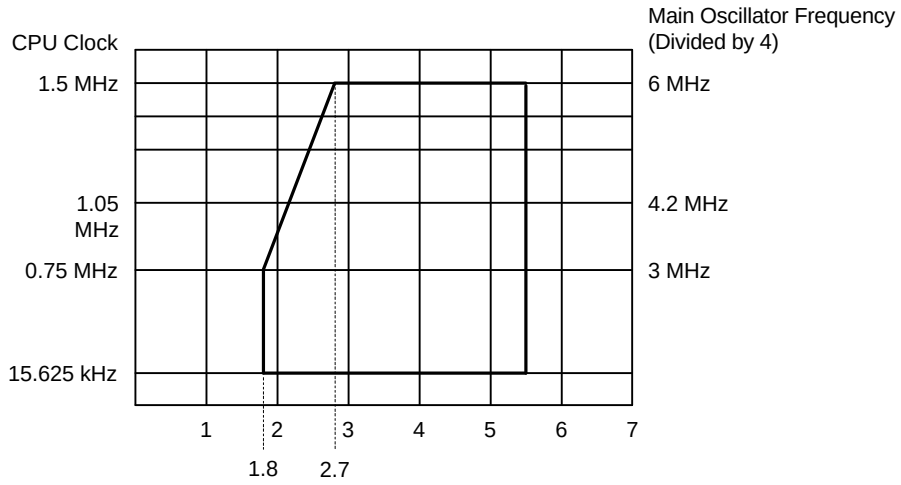
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 5.5 V	–	–	10	s
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XH}, t_{XL})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs or when stop mode is terminated.

Table 16-9. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF



CPU Clock = 1/n x oscillator frequency (n = 4, 8 or 64)

Figure 16-3. Standard Operating Voltage Range