



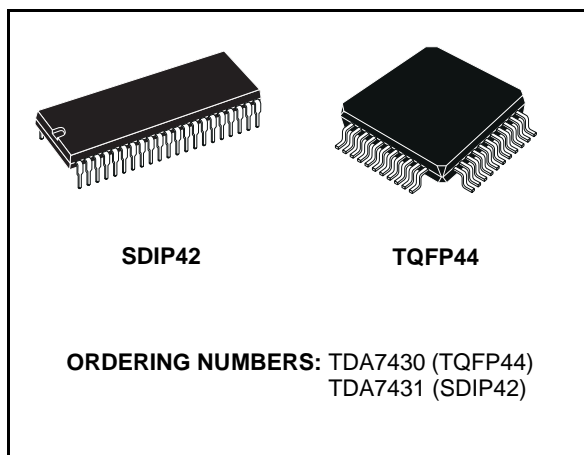
# TDA7430 TDA7431

## DIGITALLY CONTROLLED AUDIO PROCESSOR WITH SURROUND SOUND MATRIX AND VOICE CANCELLER

- 1 STEREO (4 STEREO) INPUT + 1 MIXER INPUT
- INPUT ATTENUATION CONTROL IN 0.5dB STEP
- VOICE CANCELLER IS AVAILABLE
- TREBLE MIDDLE AND BASS CONTROL
- THREE SURROUND MODES ARE AVAILABLE:
  - MUSIC: 4 SELECTABLE RESPONSES
  - MOVIE AND SIMULATED: 256 SELECTABLE RESPONSES
- 2 SPEAKER AND 2 RECORD ATTENUATORS:
  - 2 INDEPENDENT SPEAKERS AND 2 INDEPENDENT RECORD CONTROL IN 1dB STEP FOR BALANCE FACILITY
  - AVAILABILITY OF LOUDSPEAKER EQUALIZATION FIXED BY EXTERNAL COMPONENTS
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS

### DESCRIPTION

The TDA7430/7431 are volume tone (bass middle and treble) balance (Left/Right) processors with



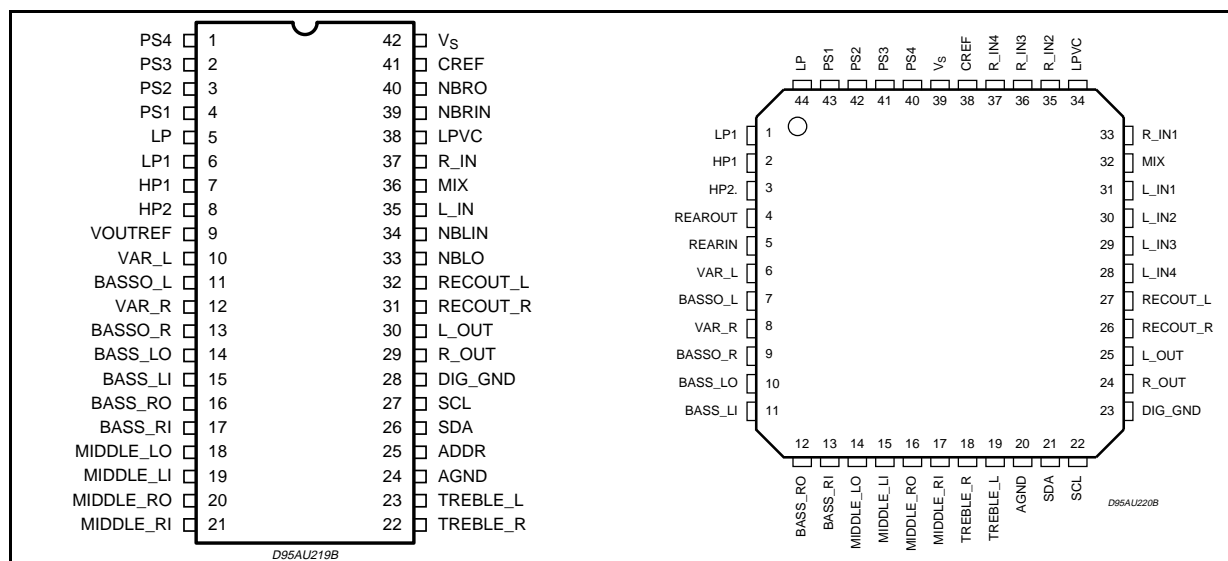
voice canceller for quality audio applications in car radio and Hi-Fi systems.

They reproduce surround sound by using programmable phase shifters and a signal matrix. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

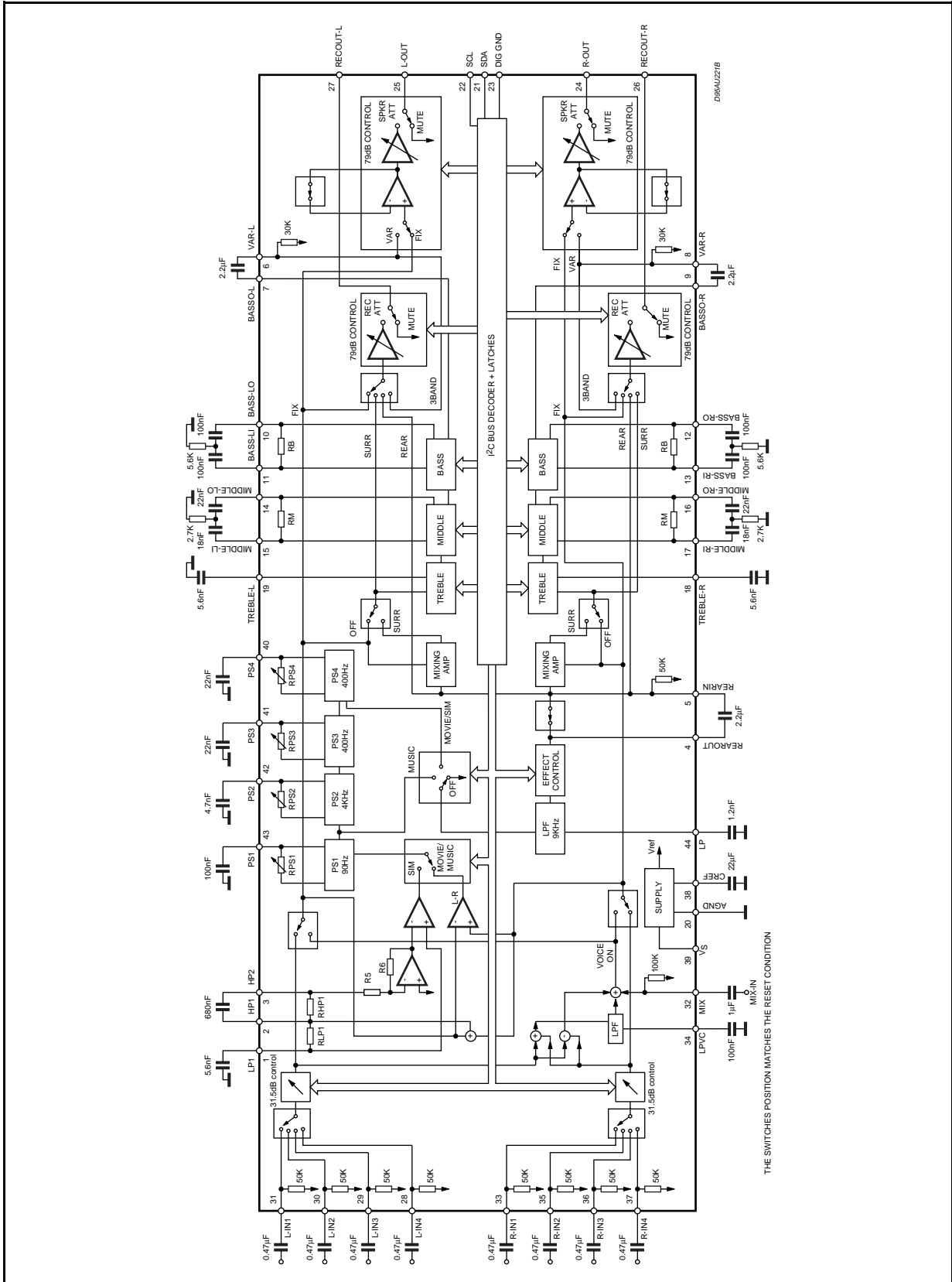
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

### PIN CONNECTIONS

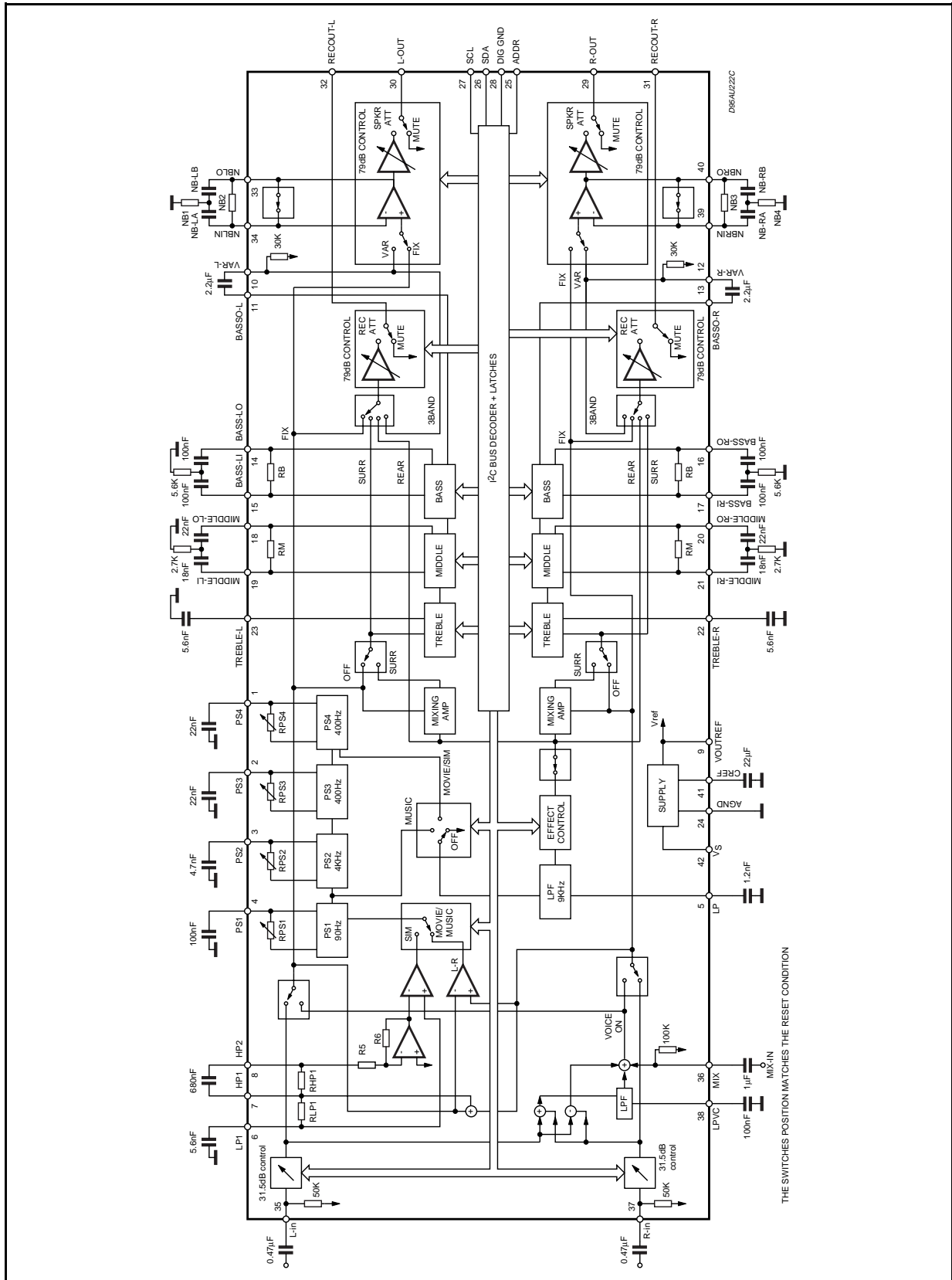


# TDA7430 - TDA7431

## BLOCK DIAGRAM (TDA7430)



BLOCK DIAGRAM (TDA7431)



THE SWITCHES POSITION MATCHES THE RESET CONDITION



**THERMAL DATA**

Symbol	Description	Value	Unit
$R_{th\ j-pins}$	Thermal Resistance Junction-pins	Max. 85	°C/W

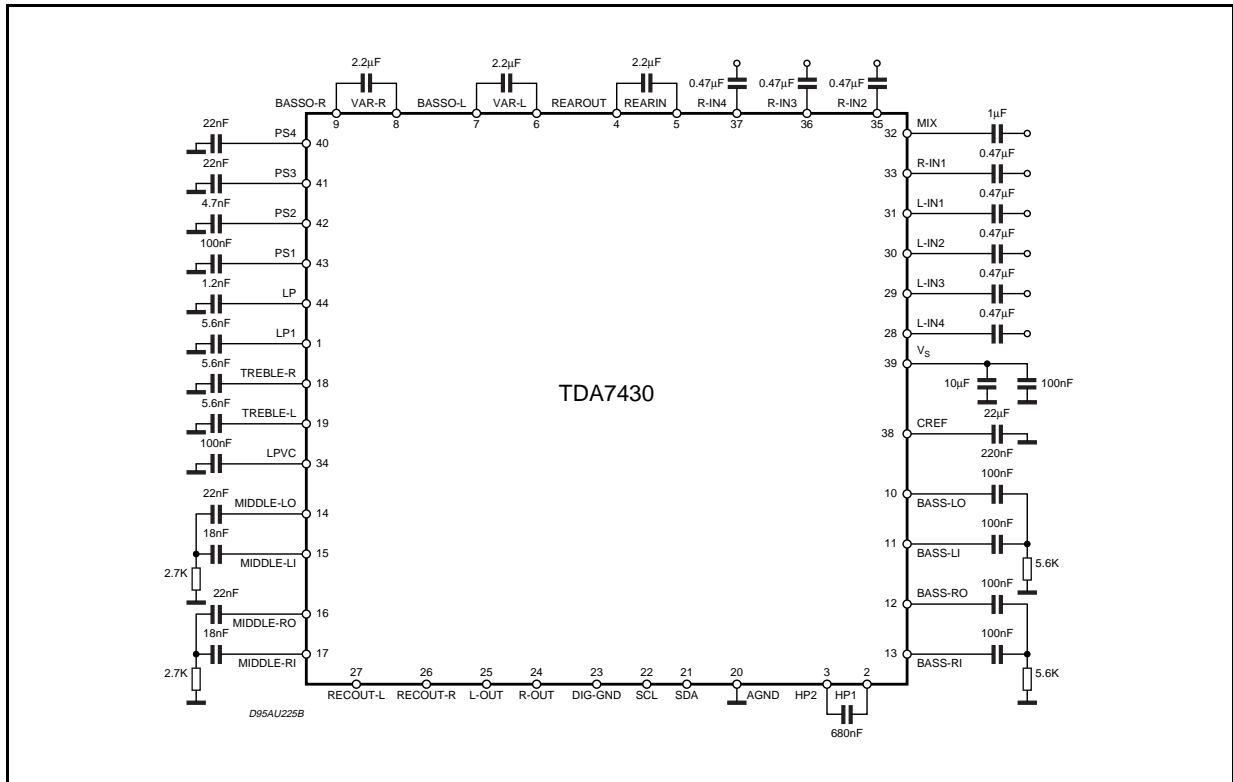
**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_S$	Operating Supply Voltage	11	V
$T_{amb}$	Operating Ambient Temperature	-10 to 85	°C
$T_{stg}$	Storage Temperature Range	-55 to +150	°C

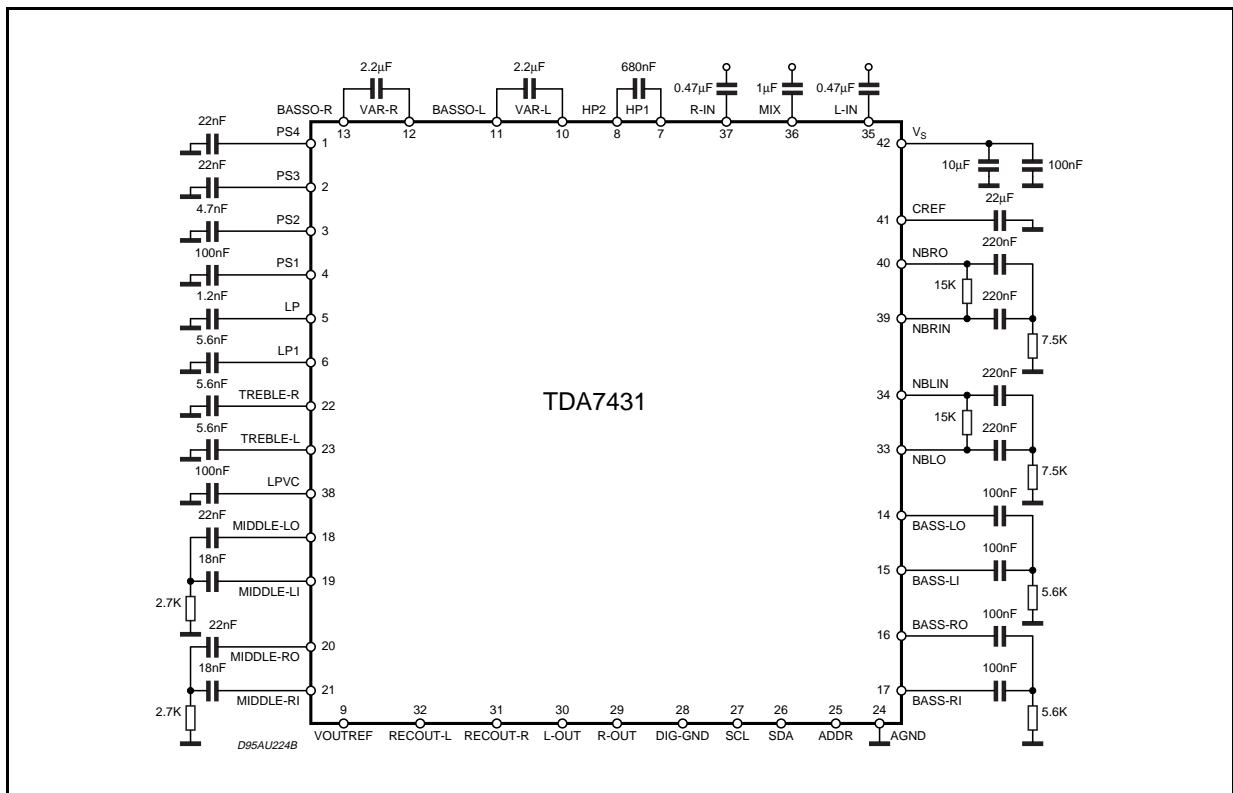
**QUICK REFERENCE DATA**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage	7	9	10.2	V
$V_{CL}$	Max. input signal handling	2			V <sub>rms</sub>
THD	Total Harmonic Distortion $V = 1V_{rms}$ $f = 1KHz$		0.01	0.1	%
S/N	Signal to Noise Ratio $V_{out} = 1V_{rms}$ (mode = OFF)		106		dB
$S_C$	Channel Separation $f = 1KHz$		90		dB
	Treble Control (2db step)	-14		+14	dB
	Middle Control (2db step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control 1dB step (L <sub>CH</sub> , R <sub>CH</sub> )	-79		0	dB
	Mute Attenuation		100		dB

TEST CIRCUIT (TDA7430)



TEST CIRCUIT (TDA7431)



## TDA7430 - TDA7431

**ELECTRICAL CHARACTERISTICS** (refer to the test circuit  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 9\text{V}$ ,  $R_L = 10\text{K}\Omega$ ,  $V_{in} = 1\text{V}_{rms}$ ;  $R_G = 600\Omega$ , all controls flat ( $G = 0\text{dB}$ ), Effect Ctrl =  $-6\text{dB}$ , MODE = OFF;  $f = 1\text{KHz}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>SUPPLY</b>						
$V_S$	Supply Voltage		7	9	10.2	V
$I_S$	Supply Current		10	18	26	mA
SVR	Ripple Rejection	LCH / RCH out, Mode = OFF	60	80		dB
<b>INPUT STAGE</b>						
$R_{IN}$	Input Resistance		35	50	65	$\text{K}\Omega$
$V_{CL}$	Clipping Level	THD = 0.3%	2	2.5		$\text{V}_{rms}$
$C_{RANGE}$	Control Range			31.5		dB
$A_{VMIN}$	Min. Attenuation		-1	0	1	dB
$A_{VMAX}$	Max. Attenuation		31	31.5	32	dB
$A_{STEP}$	Step Resolution			0.5	1	dB
$V_{DC}$	DC Steps	adjacent att. step	-3	0	3	mV
$A_{VO1}$	Voice Canceler Output 1	$L_{IN} = R_{IN}$ , $R_{IN} = \text{ON}$ , $V_{mix} = 0\text{V FIX}$ , 0dB attenuation	5	6	7	dB
$A_{VO2}$	Voice Canceler Output 2	$L_{IN} = R_{IN} = 0\text{V}$ $V_{mix} = 1\text{V}_{rms}$ FIX, 0dB attenuation	-1	0	1	dB
$A_{VO3}$	Voice Canceler Output 3	$L_{IN} = -R_{IN}$ , $V_{mix} = 0\text{V FIX}$ , 0dB attenuation	5	6	7	dB
$R_{LPV}$	Low Pass Filter Resistance		22.4	32	41.6	$\text{K}\Omega$
$R_{MIX}$	Input Impedance		70	100	130	$\text{K}\Omega$
<b>BASS CONTROL</b>						
$G_b$	Control Range	Max. Boost/cut	$\pm 11.5$	$\pm 14.0$	$\pm 16.0$	dB
$B_{STEP}$	Step Resolution		1	2	3	dB
$R_B$	Internal Feedback Resistance		32	44	56	$\text{K}\Omega$
<b>MIDDLE CONTROL</b>						
$G_m$	Control Range	Max. Boost/cut	$\pm 11.5$	$\pm 14.0$	$\pm 16.0$	dB
$M_{STEP}$	Step Resolution		1	2	3	dB
$R_M$	Internal Feedback Resistance		17.5	25	32.5	$\text{K}\Omega$
<b>TREBLE CONTROL</b>						
$G_t$	Control Range	Max. Boost/cut	$\pm 13.0$	$\pm 14.0$	$\pm 15.0$	dB
$T_{STEP}$	Step Resolution		1	2	3	dB
<b>EFFECT CONTROL</b>						
$C_{RANGE}$	Control Range		-21		-6	dB
$S_{STEP}$	Step Resolution		0.5	1	1.5	dB

**ELECTRICAL CHARACTERISTICS** (continued)

## SURROUND SOUND MATRIX

TEST CONDITION (Phase Resistor Selection D0=0, D1=1, D2=0, D3=1, D4=0, D5=1, D6=0, D7=1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G <sub>OFF</sub>	In-phase Gain (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> → R <sub>out</sub> L <sub>in</sub> → L <sub>out</sub>	-1	0	1	dB
D <sub>G<sub>OFF</sub></sub>	LR In-phase Gain Difference (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V <sub>p-p</sub> R <sub>in</sub> → R <sub>out</sub> , L <sub>in</sub> → L <sub>out</sub>	-1	0	1	dB
G <sub>MOV</sub>	In-phase Gain (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V <sub>p-p</sub> R <sub>in</sub> → R <sub>out</sub> , L <sub>in</sub> → L <sub>out</sub>		8		dB
D <sub>G<sub>MOV</sub></sub>	LR In-phase Gain Difference (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V <sub>p-p</sub> (R <sub>in</sub> → R <sub>out</sub> ) - (L <sub>in</sub> → L <sub>out</sub> )		0		dB
G <sub>MUS</sub>	In-phase Gain (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V <sub>p-p</sub> (R <sub>in</sub> → R <sub>out</sub> ), (L <sub>in</sub> → L <sub>out</sub> )		7		dB
D <sub>G<sub>MUS</sub></sub>	LR In-phase Gain Difference (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V <sub>p-p</sub> (R <sub>in</sub> → R <sub>out</sub> ) - (L <sub>in</sub> → L <sub>out</sub> )		0		dB
L <sub>MON1</sub>	Simulated L Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> and L <sub>in</sub> → L <sub>out</sub>		4.5		dB
L <sub>MON2</sub>	Simulated L Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> and L <sub>in</sub> → L <sub>out</sub>		-4.0		dB
L <sub>MON3</sub>	Simulated L Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> and L <sub>in</sub> → L <sub>out</sub>		7.0		dB
R <sub>MON1</sub>	Simulated R Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> and L <sub>in</sub> → R <sub>out</sub>		-4.5		dB
R <sub>MON2</sub>	Simulated R Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> and L <sub>in</sub> → R <sub>out</sub>		3.8		dB
R <sub>MON3</sub>	Simulated R Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V <sub>p-p</sub> , R <sub>in</sub> and L <sub>in</sub> → R <sub>out</sub>		-20		dB
R <sub>LP1</sub>	Low Pass Filter Resistance		7	10	13	KΩ
R <sub>HPI</sub>	High Pass Filter Resistance		42	60	78	KΩ
R <sub>LPF</sub>	LP Pin Impedance		7	10	13	KΩ

## TDA7430 - TDA7431

### ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>SURROUND SOUND MATRIX PHASE</b>						
R <sub>PS10</sub>	Phase Shifter 1: D1 = 0, D0 = 0		8.3	11.8	15.2	K $\Omega$
R <sub>PS11</sub>	Phase Shifter 1: D1 = 0, D0 = 1		10	14.1	18.3	K $\Omega$
R <sub>PS12</sub>	Phase Shifter 1: D1 = 1, D0 = 0		12.6	17.9	23.3	K $\Omega$
R <sub>PS13</sub>	Phase Shifter 1: D1 = 1, D0 = 1		26.4	37.3	48.85	K $\Omega$
R <sub>PS20</sub>	Phase Shifter 2: D3 = 0, D2 = 0		4	5.6	7.2	K $\Omega$
R <sub>PS21</sub>	Phase Shifter 2: D3 = 0, D2 = 1		4.8	6.8	8.7	K $\Omega$
R <sub>PS22</sub>	Phase Shifter 2: D3 = 1, D2 = 0		6	8.4	10.9	K $\Omega$
R <sub>PS23</sub>	Phase Shifter 2: D3 = 1, D2 = 1		12.9	18.3	23.7	K $\Omega$
R <sub>PS30</sub>	Phase Shifter 3: D5 = 0, D4 = 0		8.5	12.1	15.6	K $\Omega$
R <sub>PS31</sub>	Phase Shifter 3: D5 = 0, D4 = 1		10.2	14.5	18.7	K $\Omega$
R <sub>PS32</sub>	Phase Shifter 3: D5 = 1, D4 = 0		12.7	18.1	23.3	K $\Omega$
R <sub>PS33</sub>	Phase Shifter 3: D5 = 1, D4 = 1		27.4	39.1	50.75	K $\Omega$
R <sub>PS40</sub>	Phase Shifter 4: D7 = 0, D6 = 0		8.5	12.1	15.6	K $\Omega$
R <sub>PS41</sub>	Phase Shifter 4: D7 = 0, D6 = 1		10.2	14.5	18.7	K $\Omega$
R <sub>PS42</sub>	Phase Shifter 4: D7 = 1, D6 = 0		12.7	18.1	23.3	K $\Omega$
R <sub>PS43</sub>	Phase Shifter 4: D7 = 1, D6 = 1		27.4	39.1	50.75	K $\Omega$
<b>SPEAKER &amp; RECORD ATTENUATORS</b>						
C <sub>range</sub>	Control Range			79		dB
S <sub>STEP</sub>	Step Resolution		-0.5	1	1.5	dB
E <sub>A</sub>	Attenuation set error	Av = 0 to -20dB	-1.5	0	1.5	dB
		Av = -20 to -79dB	-3	0	2	dB
V <sub>DC</sub>	DC Steps	adjacent att. steps	-3	0	3	mV
A <sub>MUTE</sub>	Output Mute Condition		+70	100		dB
R <sub>VEA</sub>	Input Impedance		21	30	39	K $\Omega$
<b>AUDIO OUTPUTS</b>						
N <sub>O(OFF)</sub>	Output Noise (OFF)	Output Mute, Flat B <sub>W</sub> = 20Hz to 20KHz		4 5		$\mu$ Vrms $\mu$ Vrms
N <sub>O(MOV)</sub>	Output Noise (Movie)	Mode = Movie, B <sub>W</sub> = 20Hz to 20KHz		30		$\mu$ Vrms
N <sub>O(MUS)</sub>	Output Noise (Music)	Mode = Music, B <sub>W</sub> = 20Hz to 20KHz,		30		mVrms
N <sub>O(MON)</sub>	Output Noise (Simulated)	Mode = Simulated, B <sub>W</sub> = 20Hz to 20KHz		30		$\mu$ Vrms
d	Distorsion	Av = 0 ; V <sub>in</sub> = 1Vrms		0.01	0.1	%
S <sub>C</sub>	Channel Separation		70	90		dB
V <sub>OCL</sub>	Clipping Level	d = 0.3%	2	2.5		Vrms
R <sub>OUT</sub>	Output Resistance		10	40	70	$\Omega$
V <sub>OUT</sub>	DC Voltage Level			3.8		V
<b>BUS INPUTS</b>						
V <sub>IL</sub>	Input Low Voltage				1	V
V <sub>IH</sub>	Input High Voltage		3			V
I <sub>IN</sub>	Input Current		-5		+5	$\mu$ A
V <sub>O</sub>	Output Voltage SDA Acknowledge	I <sub>o</sub> = 1.6mA			0.4	V



**I<sup>2</sup>C BUS INTERFACE**

Data transmission from microprocessor to the TDA7430/TDA7431 and viceversa takes place through the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

**Data Validity**

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

**Start and Stop Conditions**

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

**Byte Format**

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-

knowledge bit. The MSB is transferred first.

**Acknowledge**

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

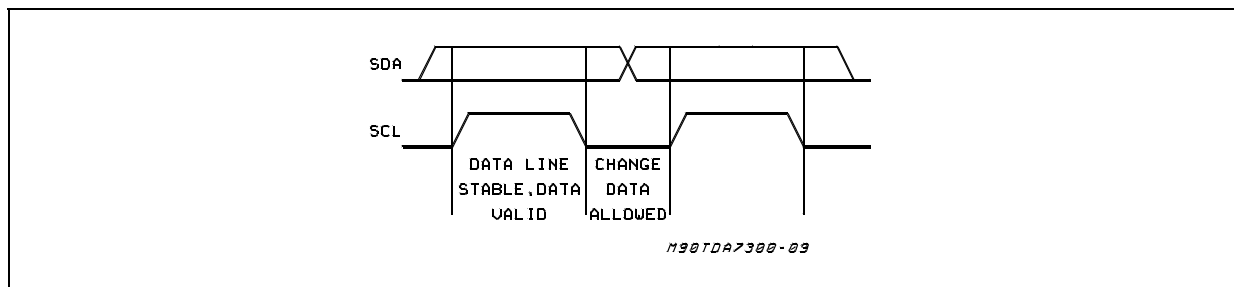
The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

**Transmission without Acknowledge**

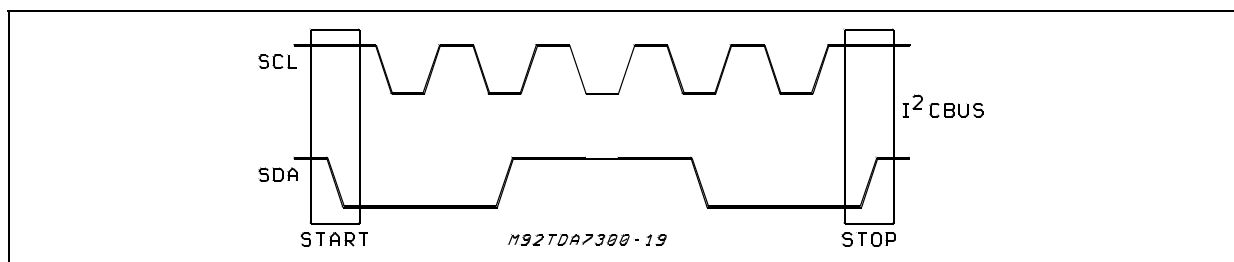
Avoiding to detect the acknowledge of the audioprocessor, the  $\mu$ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

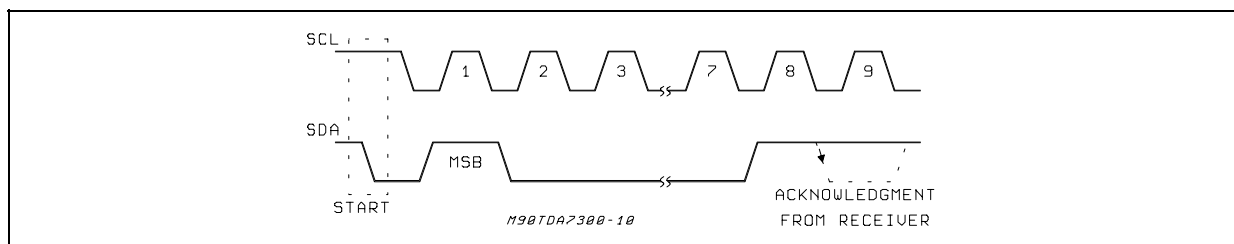
**Figure 3:** Data Validity on the I<sup>2</sup>C BUS



**Figure 4:** Timing Diagram of I<sup>2</sup>C BUS



**Figure 5:** Acknowledge on the I<sup>2</sup>C BUS



# TDA7430 - TDA7431

## SOFTWARE SPECIFICATION

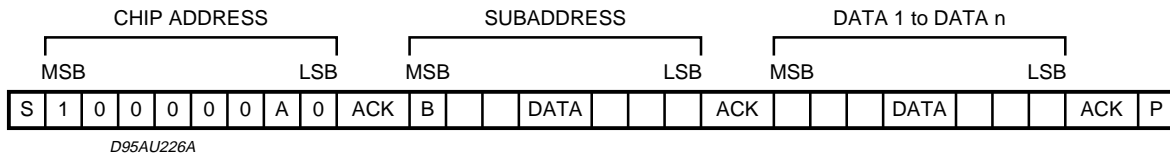
Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7430

/TDA7431 address

- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)



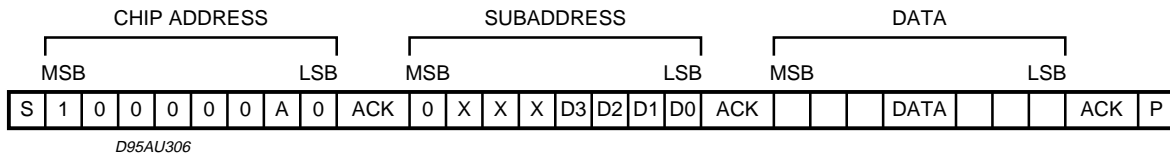
ACK = Acknowledge  
 S = Start  
 P = Stop  
 A = Address  
 B = Auto Increment

## EXAMPLES

### No Incremental Bus

The TDA7430 /TDA7431 receives a start condi-

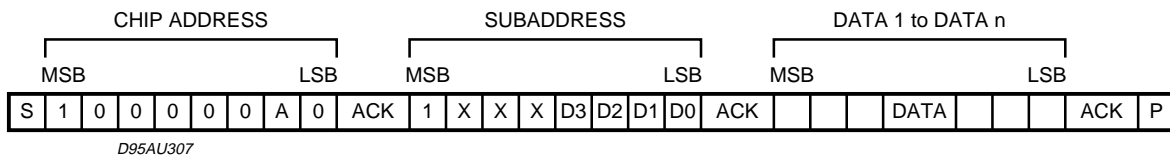
tion, the correct chip address, a subaddress with the MSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a stop condition.



### Incremental Bus

The TDA7430 /TDA7431 receive s a start condition, the correct chip address, a subaddress with the MSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress

whereas SUBADDRESS from "1XXX1010" to "1XXX1111" of DATA are ignored. The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.



**DATA BYTES**

Address = 80(HEX): ADDR open; 82 (HEX): need to connect supply

**FUNCTION SELECTION:**

The first byte (subaddress)

MSB							LSB		SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0		
B	X	X	X	0	0	0	0	INPUT ATTENUATION	
B	X	X	X	0	0	0	1	SURROUND & OUT & EFFECT CONTROL	
B	X	X	X	0	0	1	0	PHASE RESISTOR	
B	X	X	X	0	0	1	1	BASS & NATURAL BASE	
B	X	X	X	0	1	0	0	MIDDLE & TREBLE	
B	X	X	X	0	1	0	1	SPEAKER ATTENUATION "L"	
B	X	X	X	0	1	1	0	SPEAKER ATTENUATION "R"	
B	X	X	X	0	1	1	1	RECORD ATTENUATION "L"	
B	X	X	X	1	0	0	0	RECORD ATTENUATION"R"	
B	X	X	X	1	0	0	1	INPUT MULTIPLEXER, VOICE CANCELLER & REC OUT	

B = 1 incremental bus; active

B = 0 no incremental bus;

X = indifferent 0,1

**INPUT ATTENUATION SELECTION**

MSB							LSB		INPUT ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	0.5 dB STEPS	
					0	0	0	0	
					0	0	1	-0.5	
					0	1	0	-1	
					0	1	1	-1.5	
					1	0	0	-2	
					1	0	1	-2.5	
					1	1	0	-3	
					1	1	1	-3.5	
								<b>4 dB STEPS</b>	
		0	0	0				0	
		0	0	1				-4	
		0	1	0				-8	
		0	1	1				-12	
		1	0	0				-16	
		1	0	1				-20	
		1	1	0				-24	
		1	1	1				-28	

INPUT ATTENUATION = 0 ~ -31.5dB

D7	D6	D5	D4	D3	D2	D1	D0	REAR SWITCH
	0							REARIN, REAROUT PIN ACTIVE
	1							NO REARIN, REAROUT PIN



**SURROUND SELECTION**

MSB							LSB		
D7	D6	D5	D4	D3	D2	D1	D0	SURROUND MODE	
						0	0	SIMULATED	
						0	1	MUSIC	
						1	0	OFF	
						1	1	MOVIE	
								<b>OUT</b>	
								VAR	
								FIX	
								<b>EFFECT CONTROL</b>	
	0	0	0	0				-6	
	0	0	0	1				-7	
	0	0	1	0				-8	
	0	0	1	1				-9	
	0	1	0	0				-10	
	0	1	0	1				-11	
	0	1	1	0				-12	
	0	1	1	1				-13	
	1	0	0	0				-14	
	1	0	0	1				-15	
	1	0	1	0				-16	
	1	0	1	1				-17	
	1	1	0	0				-18	
	1	1	0	1				-19	
	1	1	1	0				-20	
	1	1	1	1				-21	

**PHASE RESISTOR SELECTION**

MSB							LSB		SURROUND PHASE RESISTOR
D7	D6	D5	D4	D3	D2	D1	D0	PHASE SHIFT 1 (KΩ)	
						0	0	12	
						0	1	14	
						1	0	18	
						1	1	37	
								<b>PHASE SHIFT 2 (KΩ)</b>	
								6	
								7	
								8	
								18	
								<b>PHASE SHIFT 3 (KΩ)</b>	
								12	
								14	
								18	
								39	
								<b>PHASE SHIFT 4 (KΩ)</b>	
0	0							12	
0	1							14	
1	0							18	
1	1							39	

<b>BASS SELECTION</b>								
<b>MSB</b>							<b>LSB</b>	<b>BASS</b>
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>2 dB STEPS</b>
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14
								<b>NATURAL BASE</b>
								NBRIN, NBRO, NBLIN, NBLO PIN ACTIVE
								NO NBRIN, NBRO, NBLIN, NBLO PIN
<b>SPEAKER/RECORD ATT. R &amp; L SELECTION</b>								
<b>MSB</b>							<b>LSB</b>	<b>SPEAKER/RECORD ATT</b>
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>1 dB STEPS</b>
					0	0	0	0
					0	0	1	-1
					0	1	0	-2
					0	1	1	-3
					1	0	0	-4
					1	0	1	-5
					1	1	0	-6
					1	1	1	-7
								<b>8 dB STEPS</b>
	0	0	0	0				0
	0	0	0	1				-8
	0	0	1	0				-16
	0	0	1	1				-24
	0	1	0	0				-32
	0	1	0	1				-40
	0	1	1	0				-48
	0	1	1	1				-56
	1	0	0	0				-64
	1	0	0	1				-72
								<b>MUTE</b>
	1	0	1	X				
	1	1	X	X				

X = INDIFFERENT 0,1

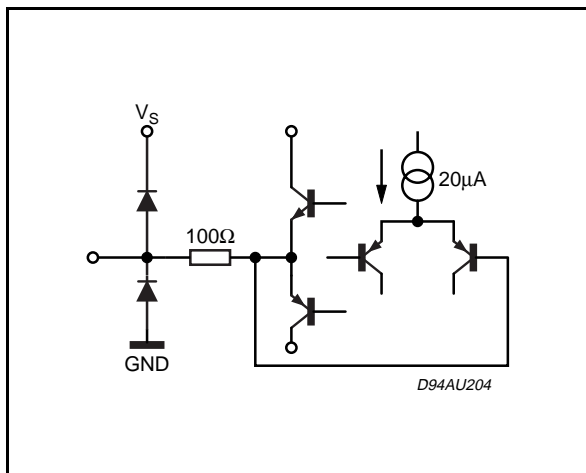
SPEAKER/RECORD ATTENUATION = 0dB ~ -79dB

MIDDLE & TREBLE SELECTION									
MSB								LSB	MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2 dB STEPS	
				0	0	0	0	-14	
				0	0	0	1	-12	
				0	0	1	0	-10	
				0	0	1	1	-8	
				0	1	0	0	-6	
				0	1	0	1	-4	
				0	1	1	0	-2	
				0	1	1	1	0	
				1	1	1	1	0	
				1	1	1	0	2	
				1	1	0	1	4	
				1	1	0	0	6	
				1	0	1	1	8	
				1	0	1	0	10	
				1	0	0	1	12	
				1	0	0	0	14	
								<b>TREBLE</b>	
								<b>2 dB STEPS</b>	
0	0	0	0					-14	
0	0	0	1					-12	
0	0	1	0					-10	
0	0	1	1					-8	
0	1	0	0					-6	
0	1	0	1					-4	
0	1	1	0					-2	
0	1	1	1					0	
1	1	1	1					0	
1	1	1	0					2	
1	1	0	1					4	
1	1	0	0					6	
1	0	1	1					8	
1	0	1	0					10	
1	0	0	1					12	
1	0	0	0					14	

VOICE CANCELLER/INPUT/RECOUT L & R SELECTION									
MSB							LSB		
D7	D6	D5	D4	D3	D2	D1	D0	VOICE CANCELLER	
							0	OFF	
							1	ON	
								INPUT MULTIPLEXER	
					0	0		IN2	
					0	1		IN3	
					1	0		IN4	
					1	1		IN1	
								REC OUT "L"	
			0	0				VER 1 (3BAND)	
			0	1				VER 2 (SURR)	
			1	0				VER 3 (REAR)	
			1	1				FIX	
								REC OUT "R"	
	0	0						VER 1 (3BAND)	
	0	1						VER 2 (SURR)	
	1	0						VER 3 (REAR)	
	1	1						FIX	

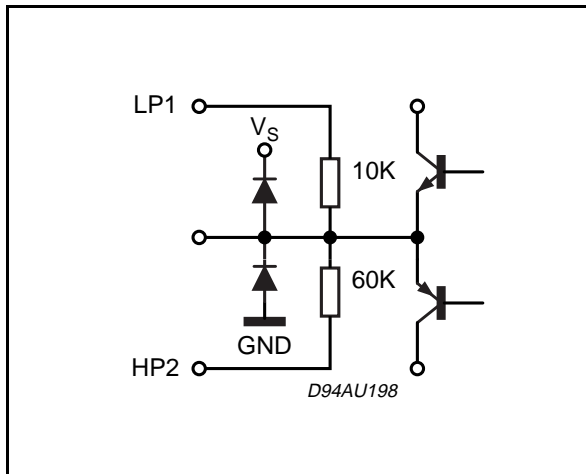
POWER ON RESET	
BASS & MIDDLE	2dB
TREBLE	0dB
SURROUND & OUT CONTROL+ EFFECT CONTROL	OFF + FIX + MAX ATTENUATION
SPEAKER/RECORD ATTENUATION L & R	MUTE
INPUT ATTENUATION + REARN SWITCH	MAX ATTENUATION + ON
NATURAL BASE	OFF
VOICE CANCELER	OFF
INPUT	IN1

**PIN:** L-OUT, R-OUT, RECOUT-L, RECOUT-R

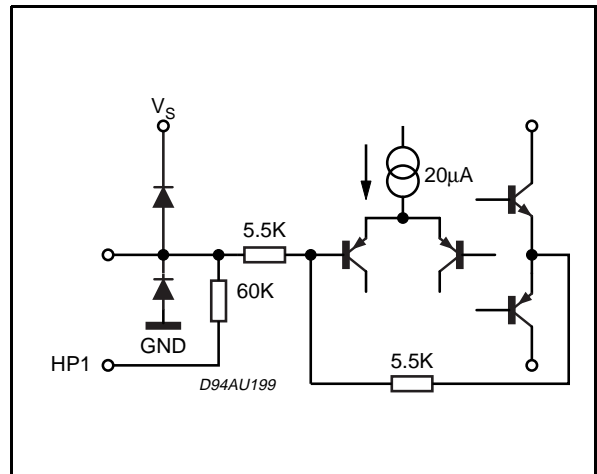


**TDA7430 - TDA7431**

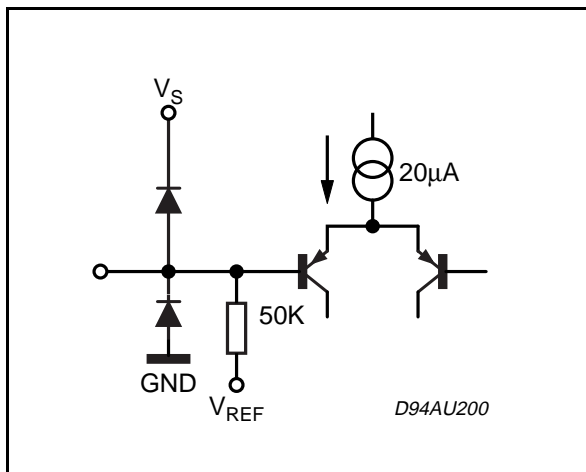
**PIN: HP1**



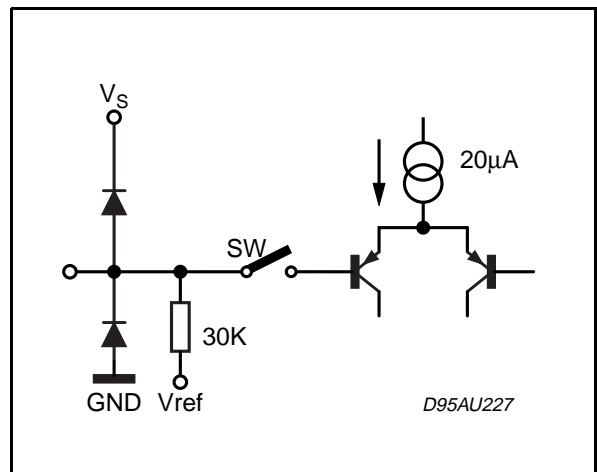
**PIN: HP2**



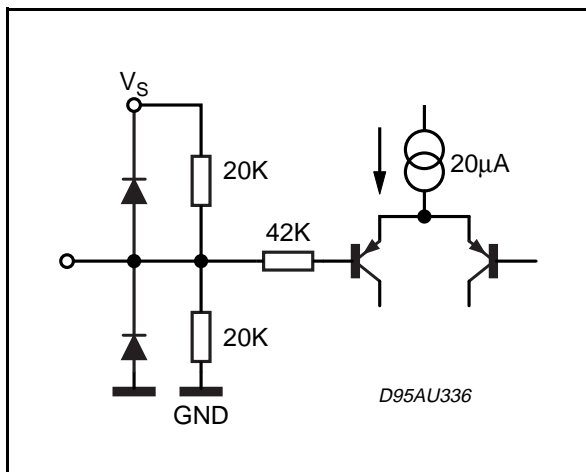
**PIN: L-IN, R-IN, L-IN2, R-IN2, L-IN3, R-IN3, L-IN4, R-IN4,**



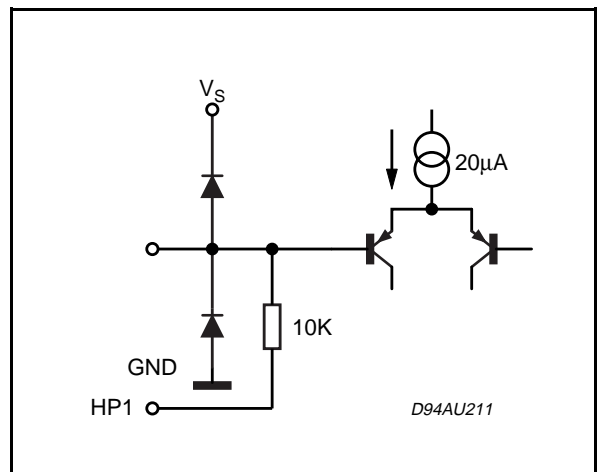
**PIN: VER-L, VER-R,**



**PIN: CREF**

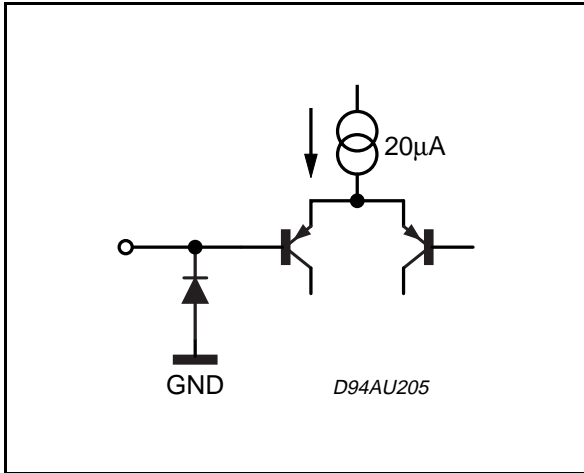


**PIN: LP1**

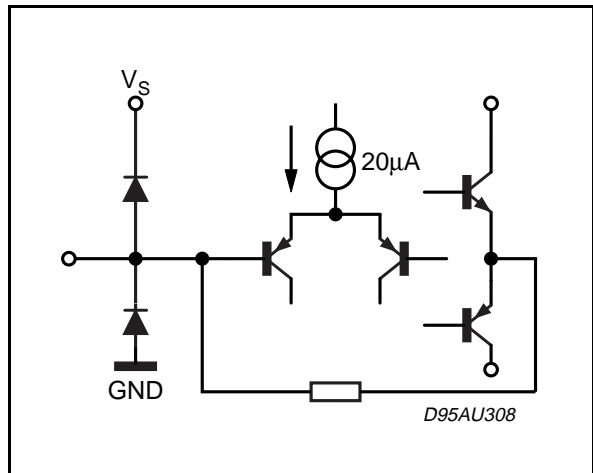




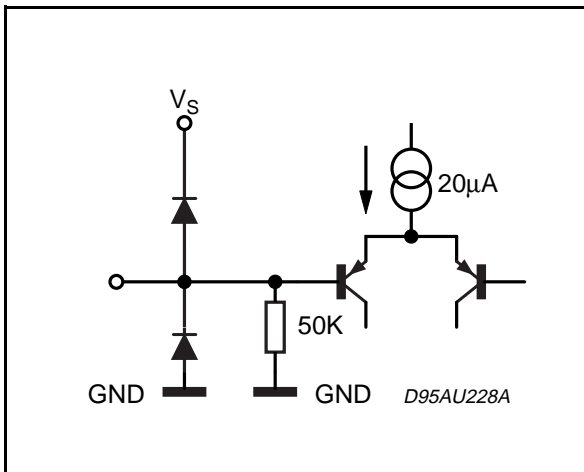
**PIN: SCL, SDA**



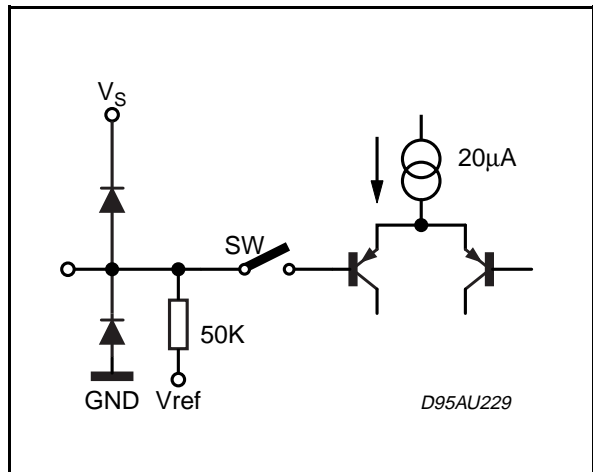
**PIN: PS1, PS2, PS3, PS4 LP**



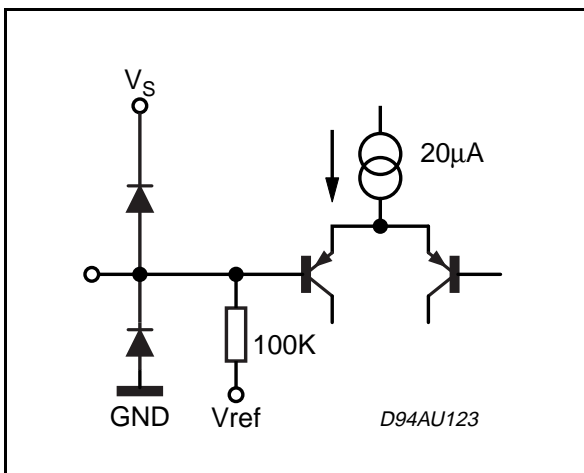
**PIN: ADDR**



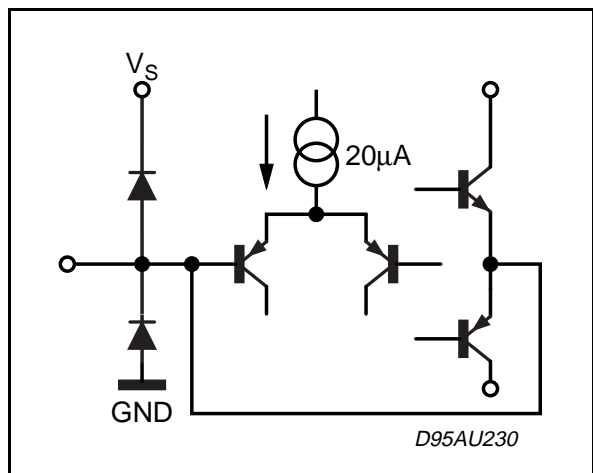
**PIN: REARIN**



**PIN: MIX**

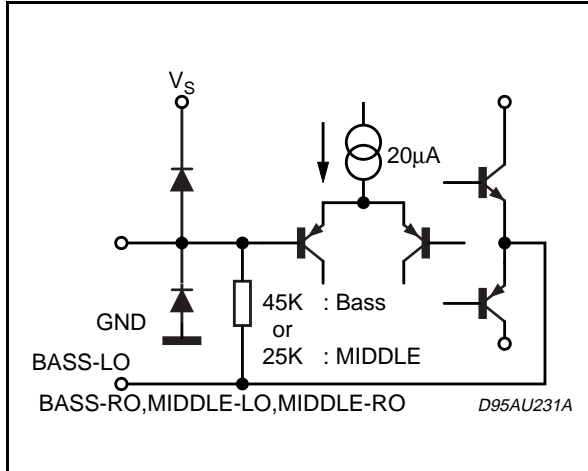


**PIN: REAROUT, BASSO-L, BASSO-R**

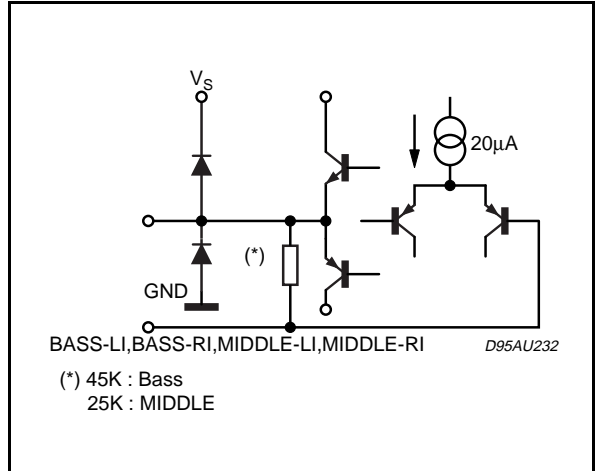


**TDA7430 - TDA7431**

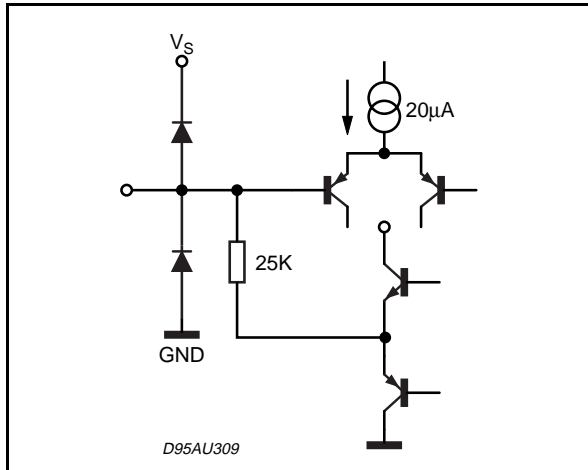
**PIN:** BASS-LI, BASS-RI, MIDDLE-LI, MIDDLE-RI,



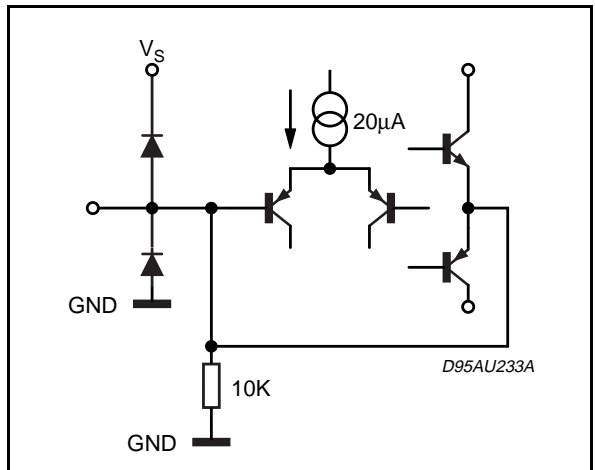
**PIN:** BASS-LO, BASS-RO, MIDDLE-LO, MIDDLE-RO,



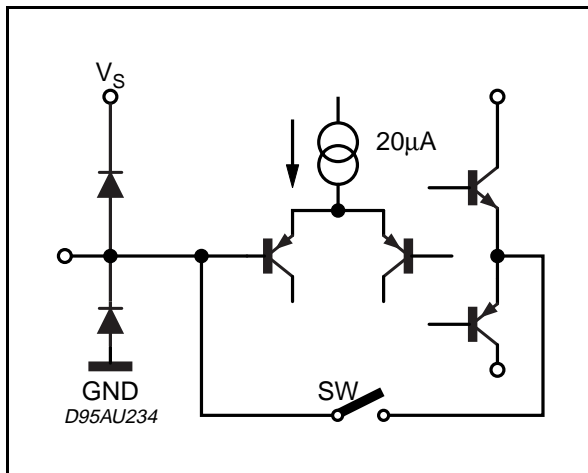
**PIN:** TREBLE-L, TREBLE-R



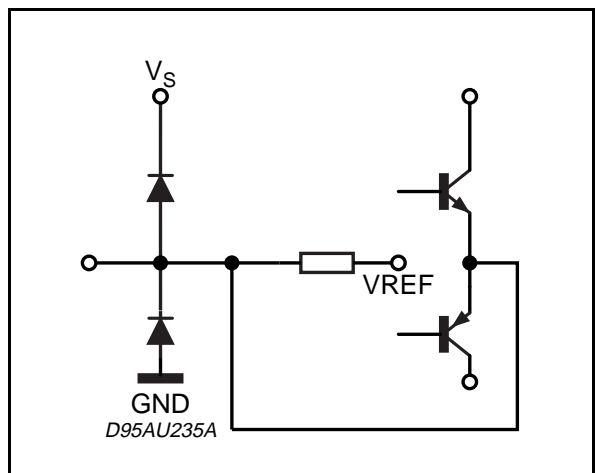
**PIN:** VOUT REF



**PIN:** NBLIN, NBRIN



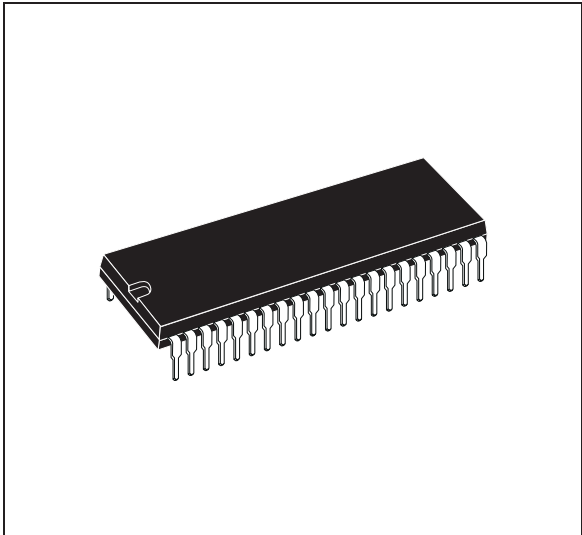
**PIN:** NBLO, NBRO



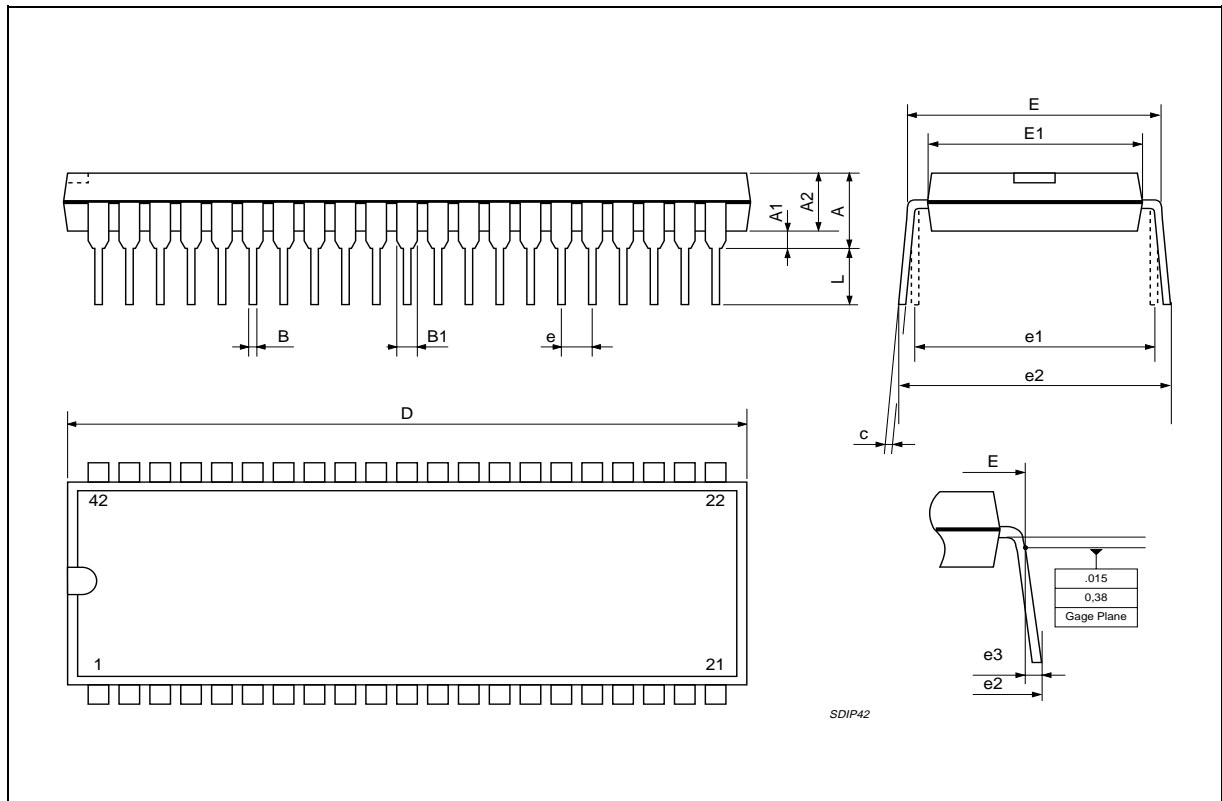
**SDIP42 PACKAGE MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.38	0.46	0.56	0.0149	0.0181	0.0220
B1	0.89	1.02	1.14	0.035	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	36.58	36.83	37.08	1.440	1.450	1.460
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

**OUTLINE AND MECHANICAL DATA**



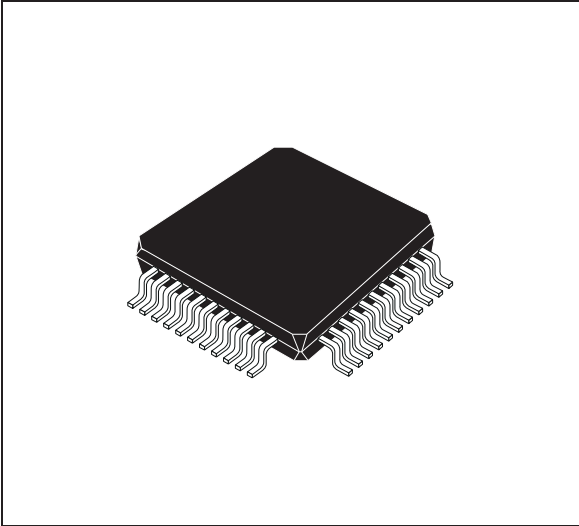
**SDIP42 (0.600")**



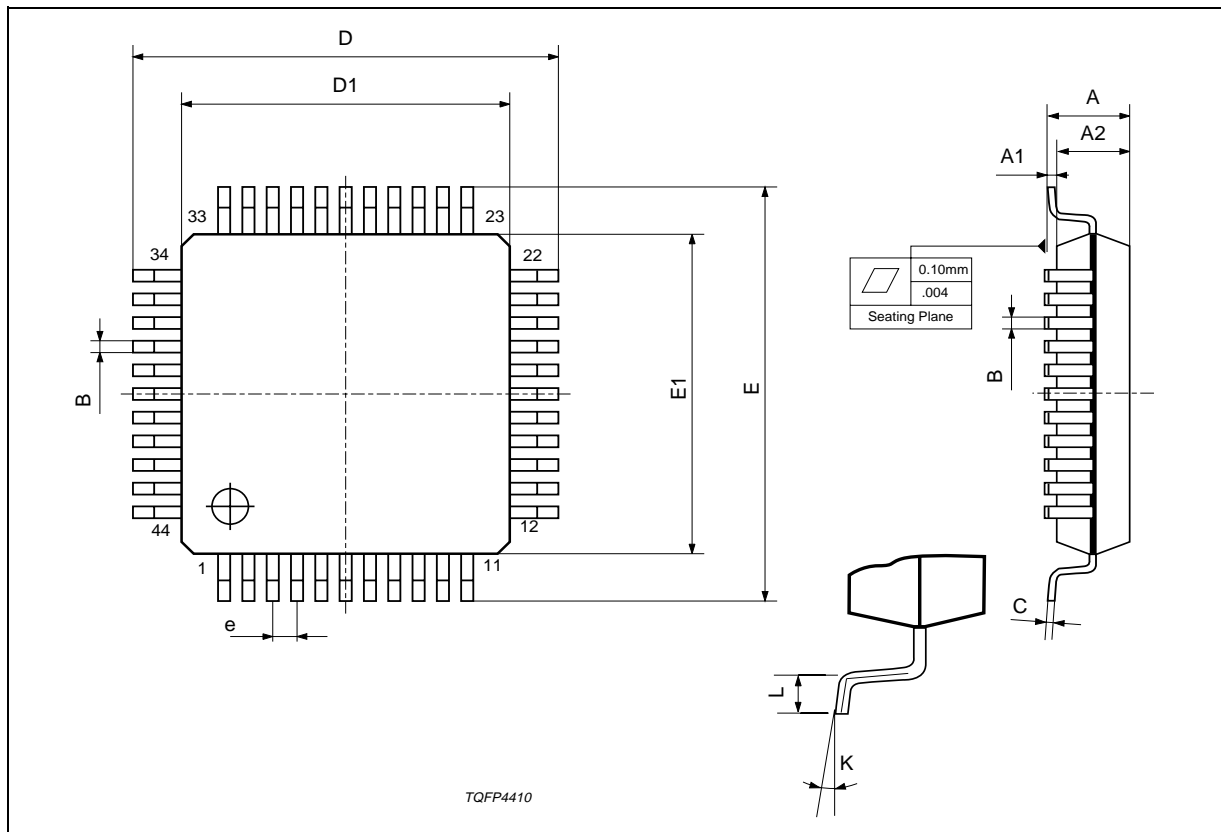
# TDA7430 - TDA7431

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

## OUTLINE AND MECHANICAL DATA



## TQFP44 (10 x 10)



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