N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
N-Channel	20	0.036 at V_{GS} = 4.5 V	4[g]	6.5 nC
		0.041 at V_{GS} = 2.5 V	4[g]	
		0.050 at V_{GS} = 1.8 V	4[g]	
P-Channel	- 20	0.100 at V_{GS} = - 4.5 V	- 4[g]	6.2 nC
		0.120 at V_{GS} = - 2.5 V	- 4[g]	
		0.156 at V_{GS} = - 1.8 V	- 3.8	

FEATURES

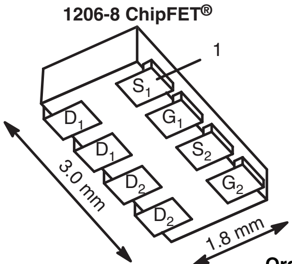
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFETs
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

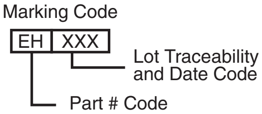
- Load Switch for Portable Devices

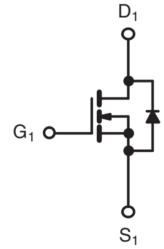
1206-8 ChipFET®



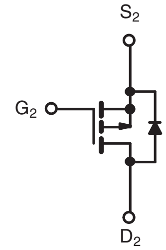
Bottom View

Marking Code





N-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si5515CDC-T1-E3 (Lead (Pb)-free)
Si5515CDC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Unit**
Drain-Source Voltage		V_{DS}	20	- 20	V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	4[g]	- 4[g]	A
	T_C = 70 °C		4[g]	- 3.8	
	T_A = 25 °C		4[b, c, g]	- 3.1[b, c]	
	T_A = 70 °C		4[b, c, g]	- 2.5[b, c]	
Pulsed Drain Current		I_{DM}	20	- 10	
Source Drain Current Diode Current	T_C = 25 °C	I_S	2.6	- 2.6	
	T_A = 25 °C		1.7[b, c]	- 1.7[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	3.1	3.1	W
	T_C = 70 °C		2.0	2.0	
	T_A = 25 °C		2.1[b, c]	1.3[b, c]	
	T_A = 70 °C		1.3[b, c]	0.8[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d, e]			260		

THERMAL RESISTANCE RATINGS							
			N-Channel		**P-Channel**		
Parameter		**Symbol**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	50	60	77	95	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	30	40	33	40	

Notes:
a. Based on T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequade bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 110 °C/W for N-Channel and 130 °C/W for P-Channel.
g. Package limited.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

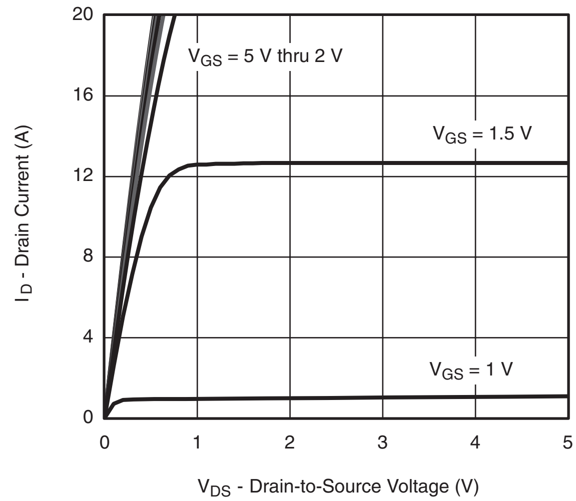
Parameter	Symbol	Test Conditions		Min.	Typ.[a]	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = - 250 µA	P-Ch	- 20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch		18		mV/°C
		I_D = - 250 µA	P-Ch		- 19		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch		- 2.7		
		I_D = - 250 µA	P-Ch		2.5		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.4		0.8	V
		V_{DS} = V_{GS}, I_D = - 250 µA	P-Ch	- 0.4		- 0.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	N-Ch			100	nA
			P-Ch			- 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V	P-Ch			- 1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	N-Ch			10	
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C	P-Ch			- 10	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	N-Ch	20			A
		$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	P-Ch	- 10			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 6.0 A	N-Ch		0.030	0.036	Ω
		V_{GS} = - 4.5 V, I_D = - 3.1 A	P-Ch		0.083	0.100	
		V_{GS} = 2.5 V, I_D = 5.6 A	N-Ch		0.034	0.041	
		V_{GS} = - 2.5 V, I_D = - 2.8 A	P-Ch		0.100	0.120	
		V_{GS} = 1.8 V, I_D = 5.1 A	N-Ch		0.040	0.050	
		V_{GS} = - 1.8 V, I_D = - 2.5 A	P-Ch		0.130	0.156	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 6.0 A	N-Ch		22.4		S
		V_{DS} = - 10 V, I_D = - 3.1 A	P-Ch		9.5		
Dynamic[a]							
Input Capacitance	C_{iss}	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		632		pF
			P-Ch		455		
Output Capacitance	C_{oss}		N-Ch		80		
			P-Ch		70		
Reverse Transfer Capacitance	C_{rss}		N-Ch		40		
			P-Ch		54		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 5 V, I_D = 6.0 A	N-Ch		7.5	11.3	nC
		V_{DS} = - 10 V, V_{GS} = - 5 V, I_D = - 3.1 A	P-Ch		7	11	
		N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 6.0 A P-Channel V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 3.1 A	N-Ch		6.5	9.8	
			P-Ch		6.2	9.3	
Gate-Source Charge	Q_{gs}		N-Ch		1.1		
			P-Ch		0.85		
Gate-Drain Charge	Q_{gd}		N-Ch		0.9		
			P-Ch		1.75		
Gate Resistance	R_g	f = 1 MHz	N-Ch	0.66	3.3	6.6	Ω
			P-Ch	1.22	6.1	12.2	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**[a]	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 2.1 Ω $I_D \cong$ 4.8 A, V_{GEN} = 8 V, R_g = 1 Ω P-Channel V_{DD} = - 10 V, R_L = 4.2 Ω $I_D \cong$ - 2.4 A, V_{GEN} = - 8 V, R_g = 1 Ω	N-Ch		3.5	7	ns
			P-Ch		3	6	
Rise Time	t_r		N-Ch		8	18	
			P-Ch		11	17	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		18	27	
			P-Ch		21	32	
Fall Time	t_f		N-Ch		8	16	
			P-Ch		6	12	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 2.1 Ω $I_D \cong$ 4.8 A, V_{GEN} = 4.5 V, R_g = 1 Ω P-Channel V_{DD} = - 10 V, R_L = 4.2 Ω $I_D \cong$ - 2.4 A, V_{GEN} = - 4.5 V, R_g = 1 Ω	N-Ch		7	14	
			P-Ch		10	20	
Rise Time	t_r		N-Ch		9	18	
			P-Ch		32	48	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		30	45	
			P-Ch		25	38	
Fall Time	t_f		N-Ch		10	20	
			P-Ch		6	12	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	N-Ch			2.6	A
			P-Ch			- 2.6	
Pulse Diode Forward Current[a]	I_{SM}		N-Ch			20	
			P-Ch			- 10	
Body Diode Voltage	V_{SD}	I_S = 4.8 A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = - 2.4 A, V_{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 4.8 A, dI/dt = 100 A/µs, T_J = 25 °C P-Channel I_F = - 2.4 A, dI/dt = - 100 A/µs, T_J = 25 °C	N-Ch		11	17	ns
			P-Ch		21	32	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		3	5	nC
			P-Ch		13	20	
Reverse Recovery Fall Time	t_a		N-Ch		6		ns
			P-Ch		17		
Reverse Recovery Rise Time	t_b		N-Ch		5		
			P-Ch		4		

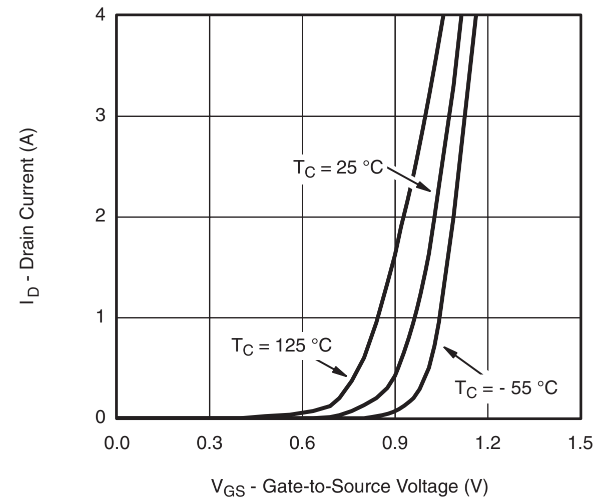
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

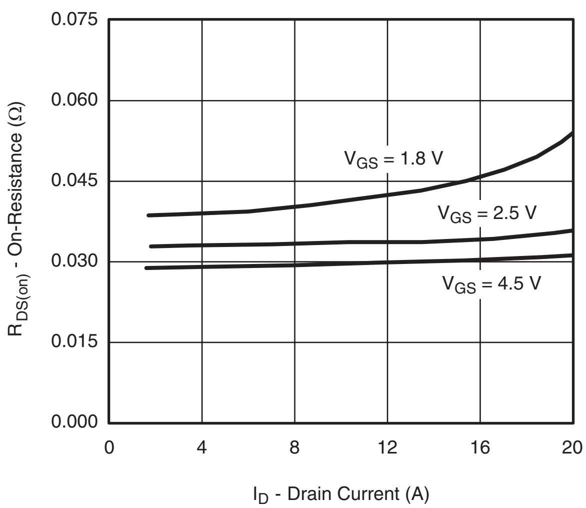
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



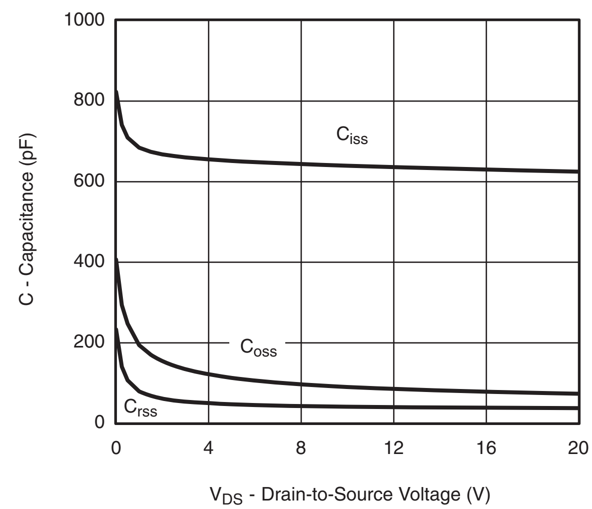
Output Characteristics



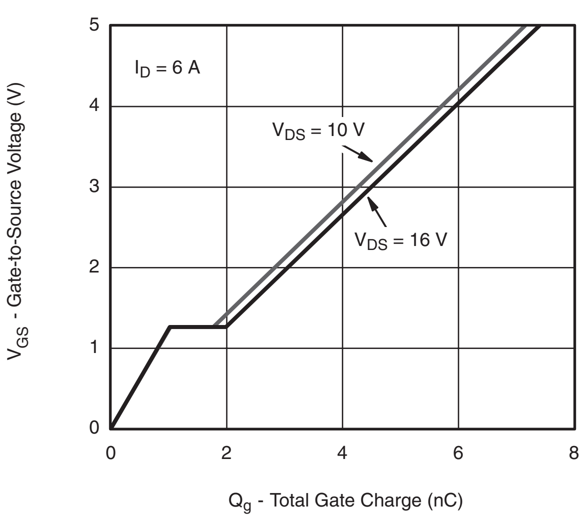
Transfer Characteristics



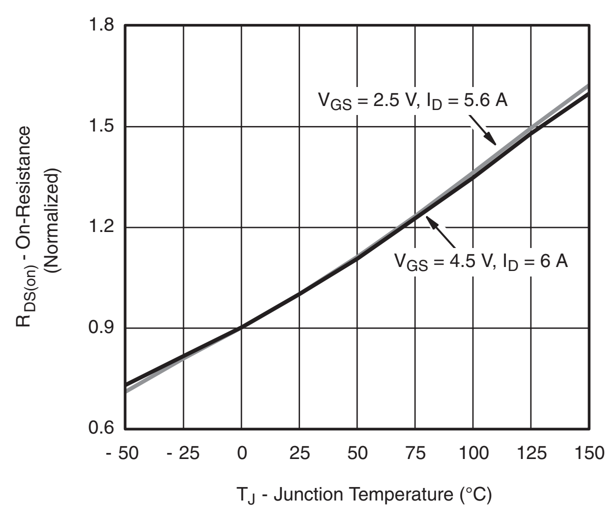
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

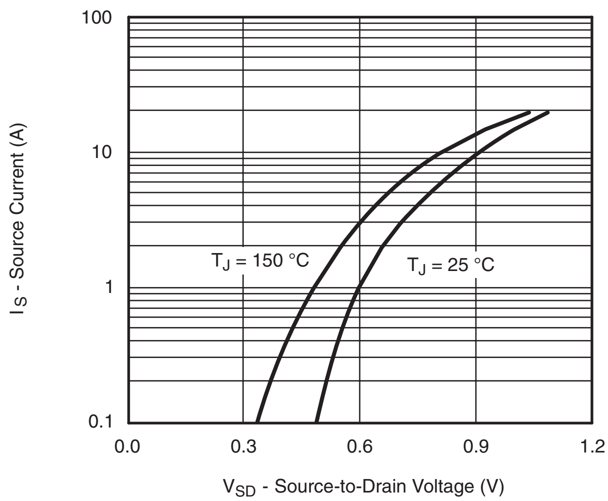


Gate Charge

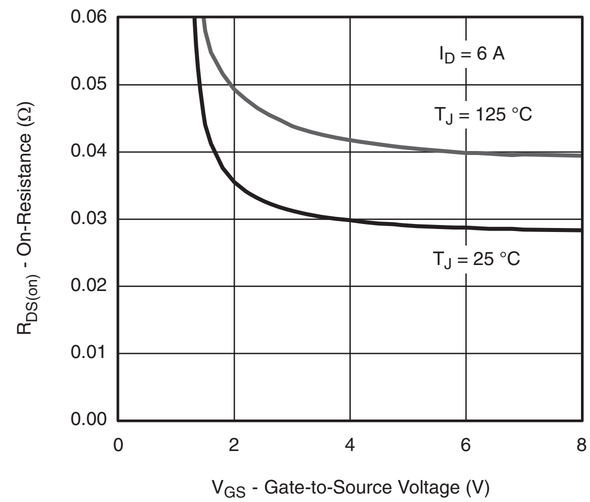


On-Resistance vs. Junction Temperature

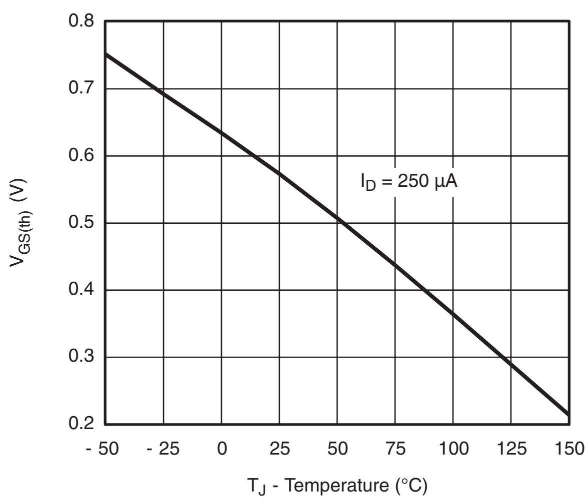
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



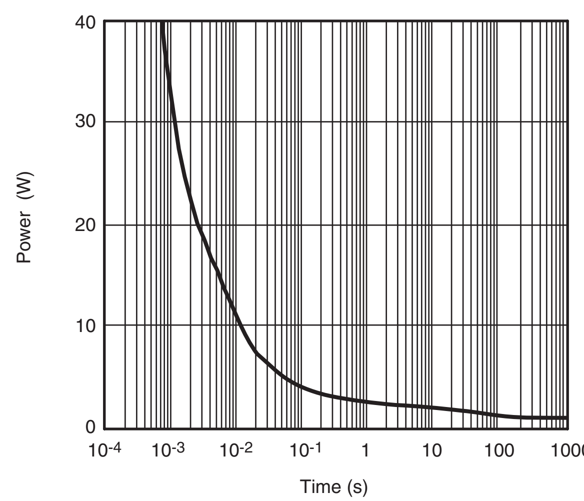
Source-Drain Diode Forward Voltage



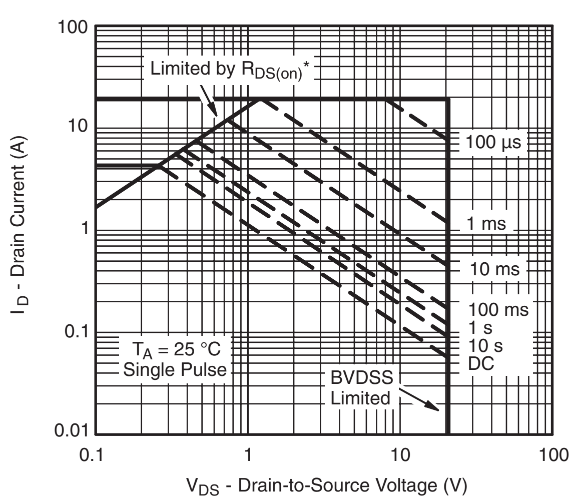
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



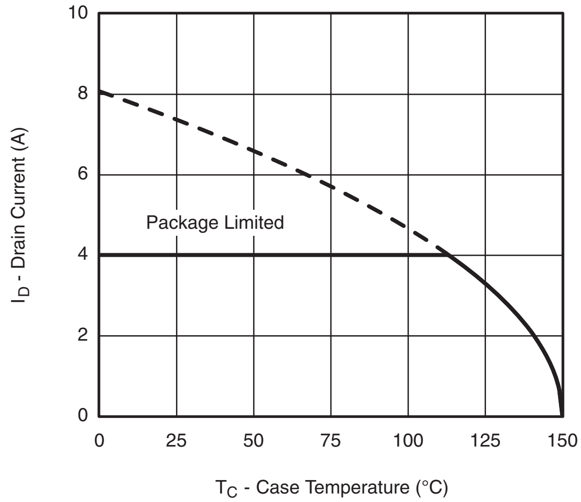
Single Pulse Power



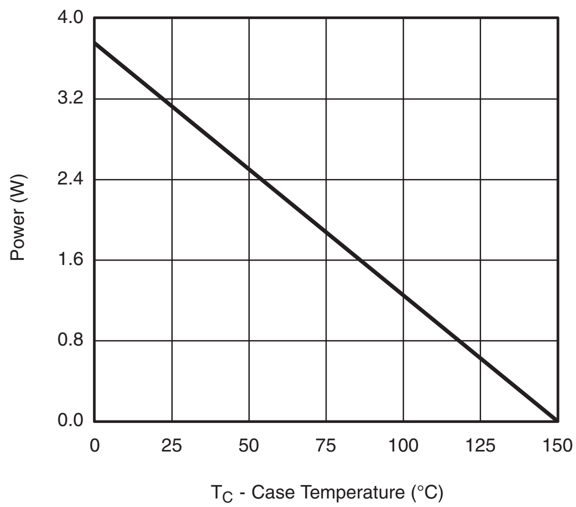
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

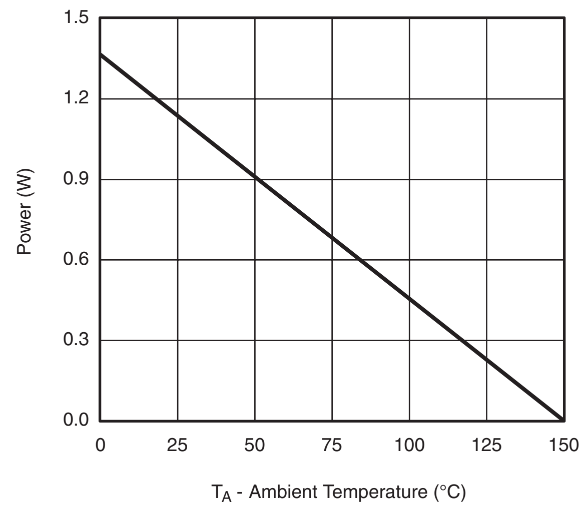
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



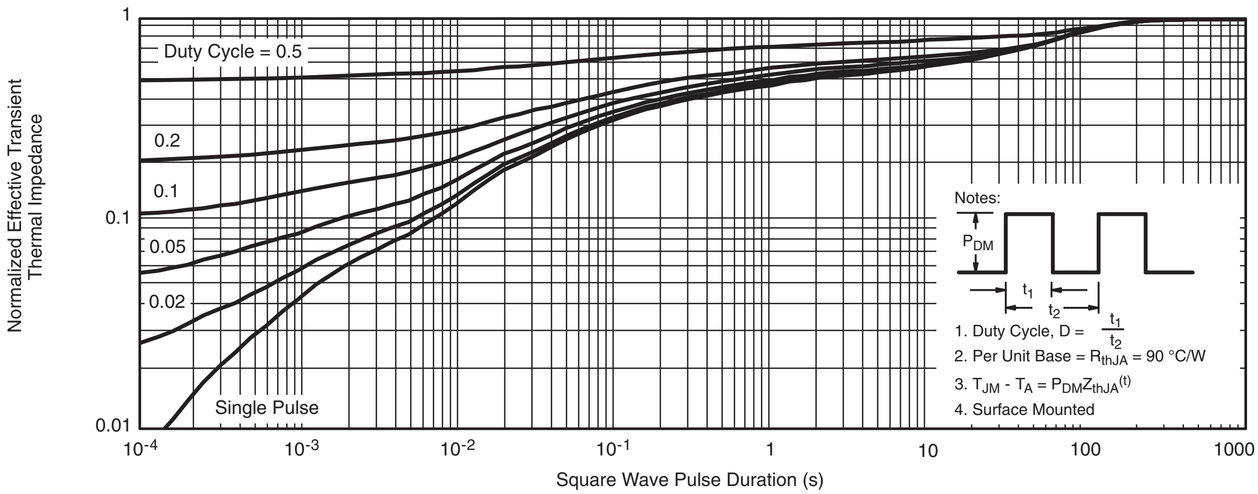
Power Derating, Junction-to-Foot



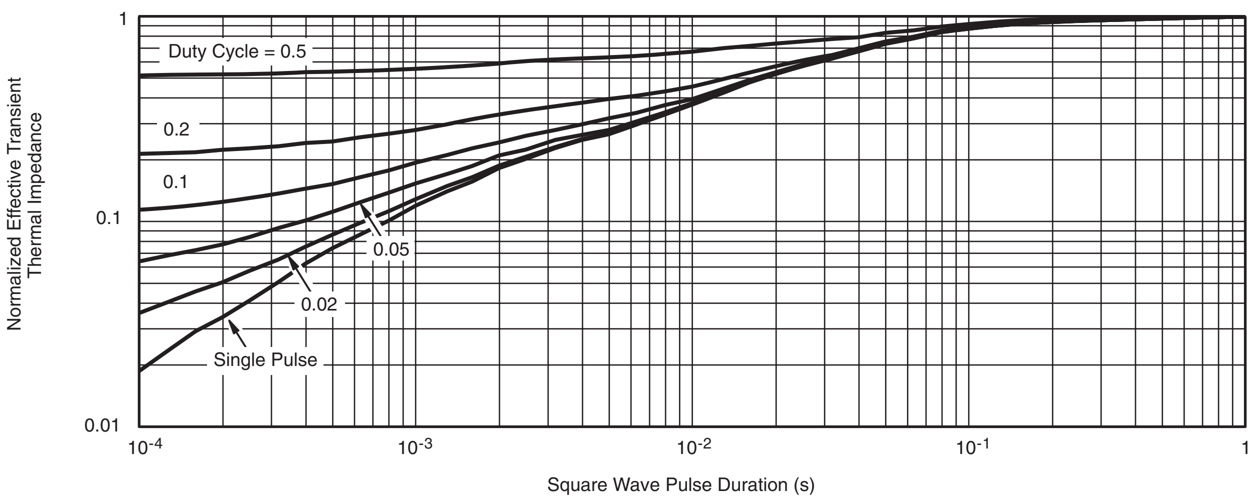
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

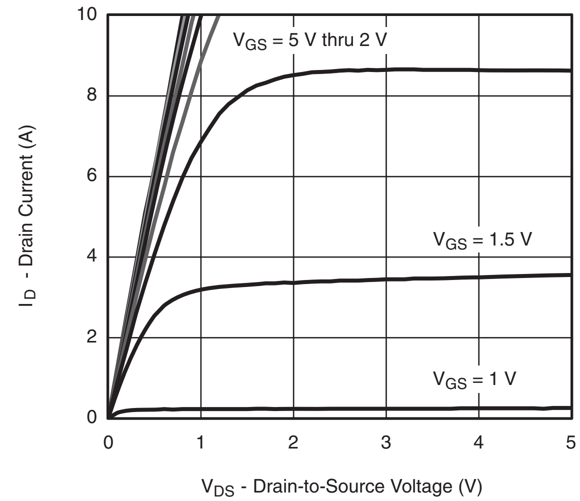


Normalized Thermal Transient Impedance, Junction-to-Ambient

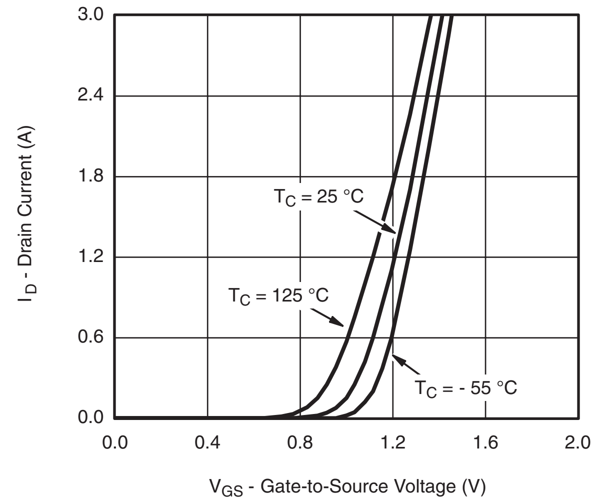


Normalized Thermal Transient Impedance, Junction-to-Foot

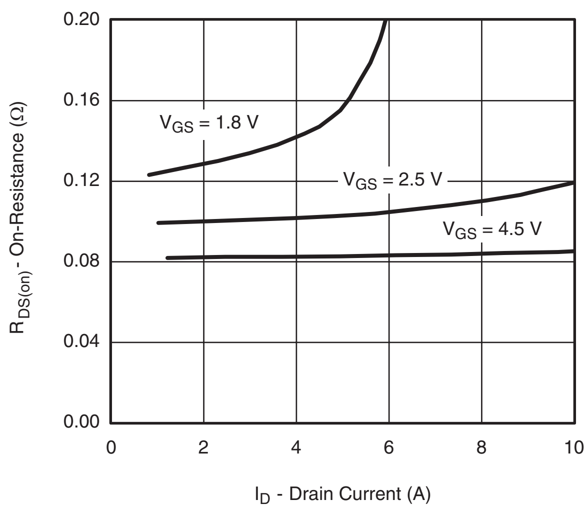
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



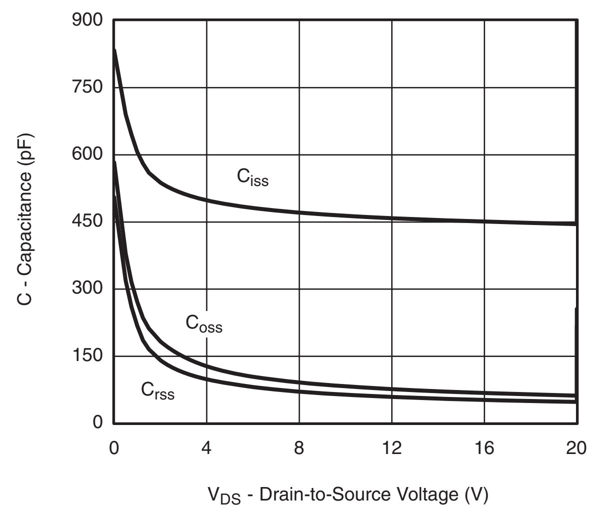
Output Characteristics



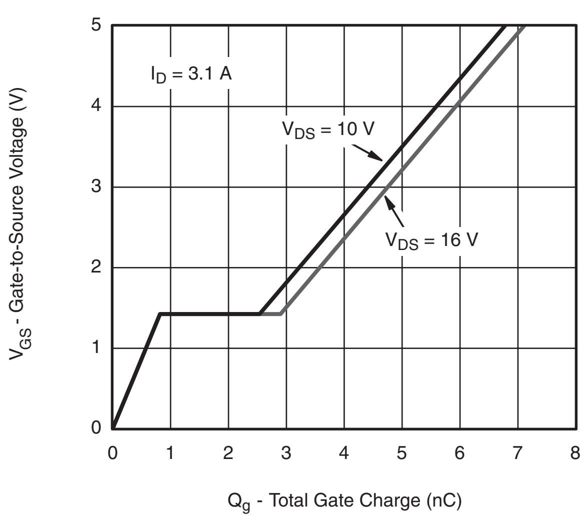
Transfer Characteristics



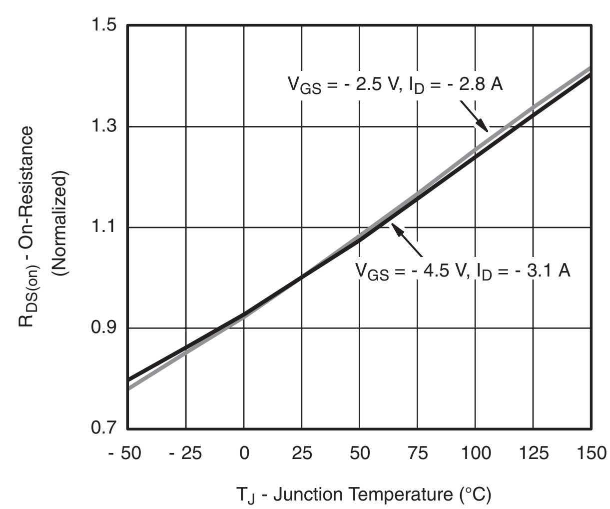
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

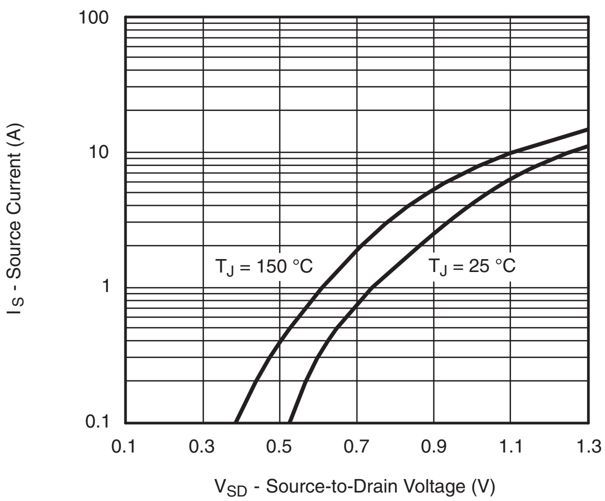


Gate Charge

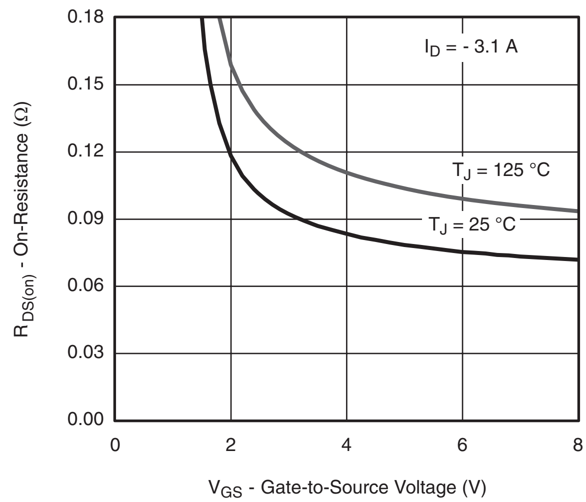


On-Resistance vs. Junction Temperature

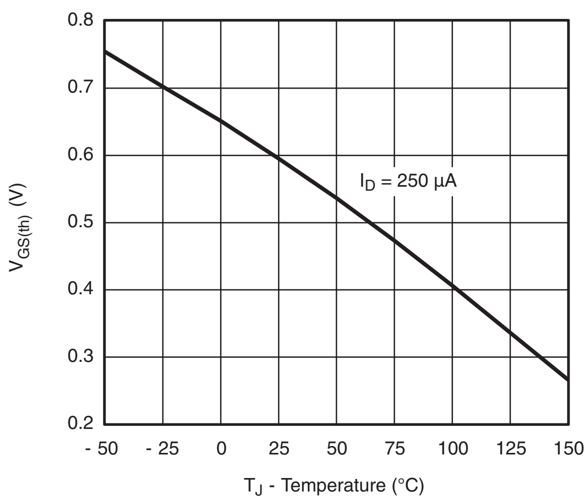
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



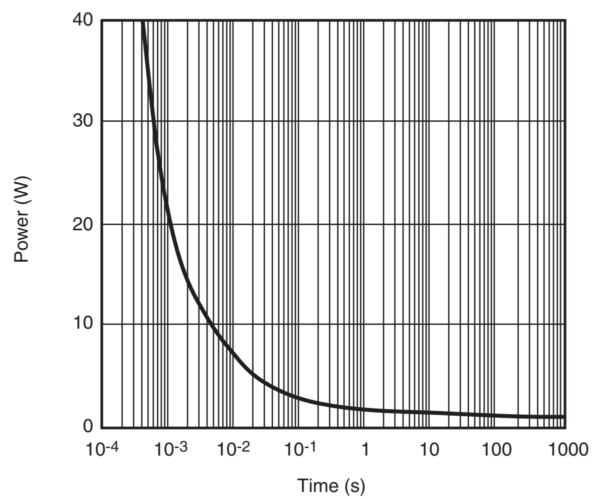
Source-Drain Diode Forward Voltage



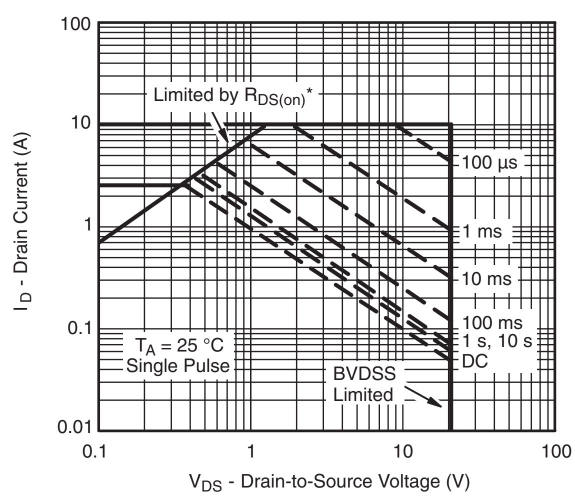
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



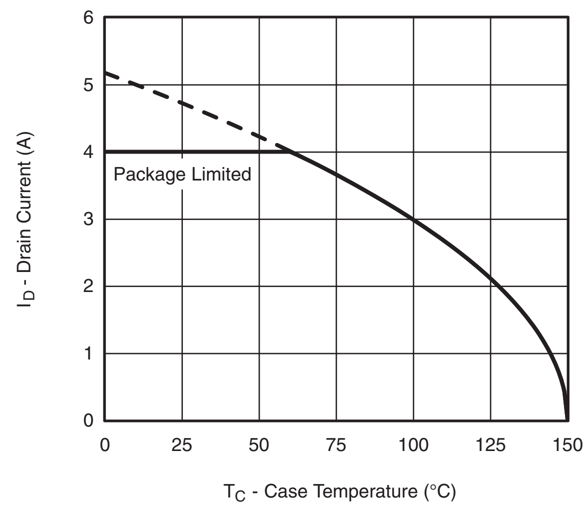
Single Pulse Power



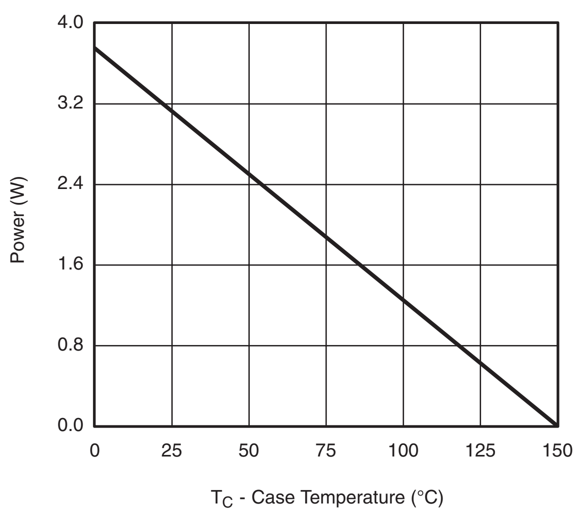
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

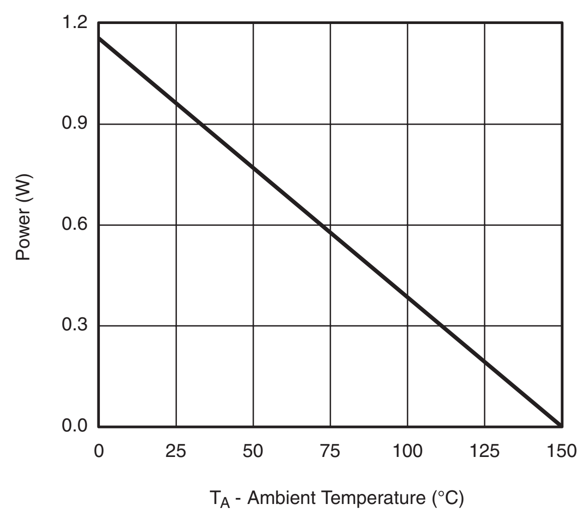
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



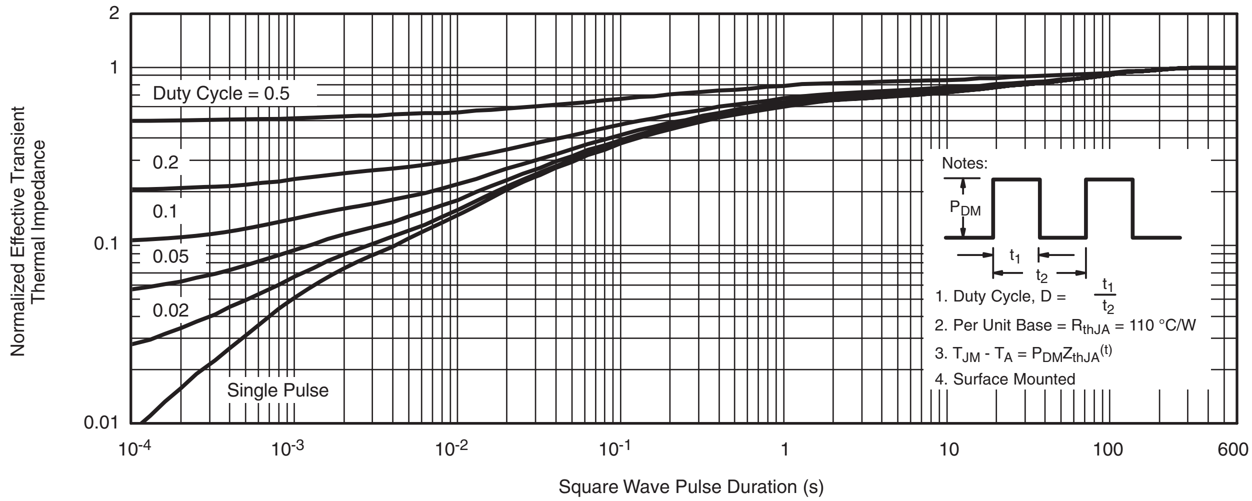
Power Derating, Junction-to-Foot



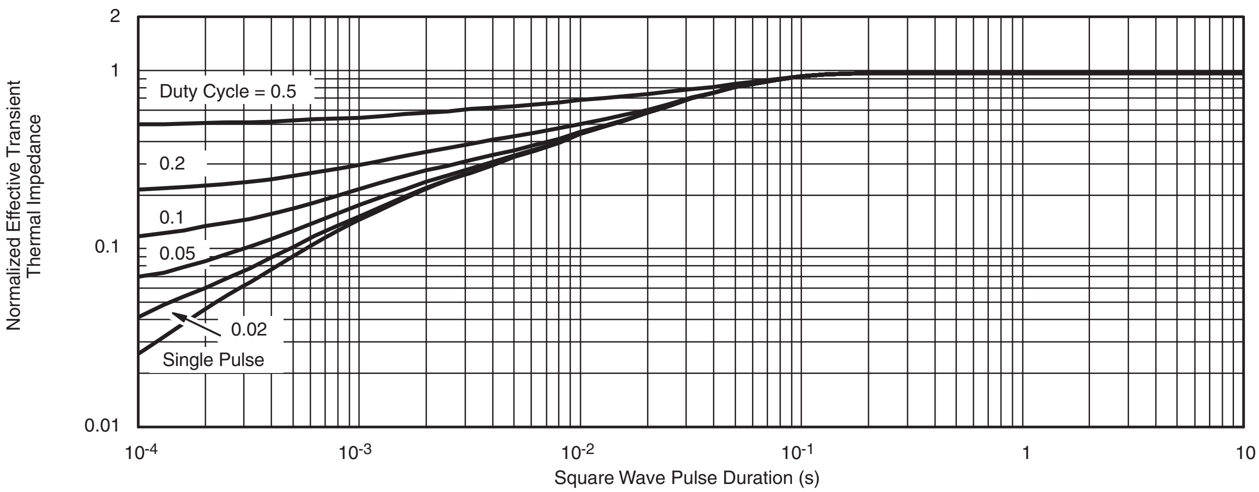
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



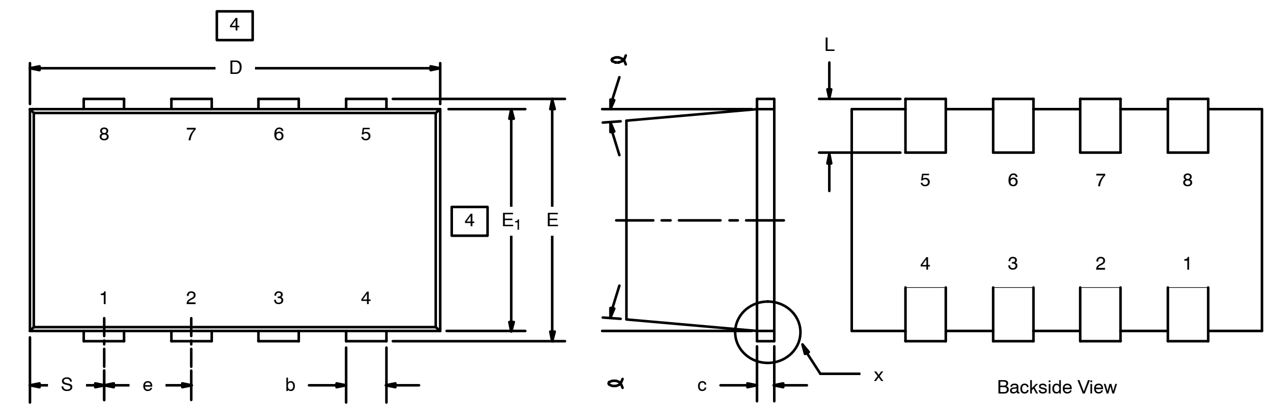
Normalized Thermal Transient Impedance, Junction-to-Ambient

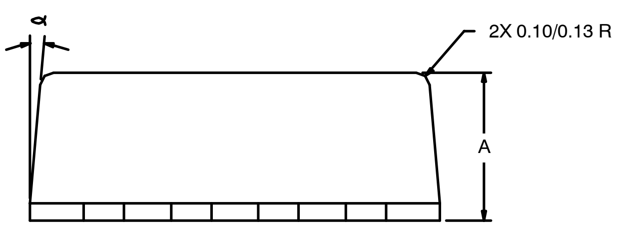


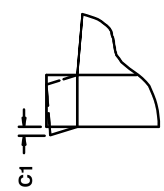
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68747.

1206-8 ChipFET®







DETAIL X

NOTES:

1. All dimensions are in millimeaters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04 DWG: 5547						

Dual-Channel 1206-8 ChipFET® Power MOSFET Recommended Pad Pattern and Thermal Performance

INTRODUCTION

New Vishay Siliconix ChipFETs in the leadless 1206-8 package feature the same outline as popular 1206-8 resistors and capacitors but provide all the performance of true power semiconductor devices. The 1206-8 ChipFET has the same footprint as the body of the LITTLE FOOT® TSOP-6, and can be thought of as a leadless TSOP-6 for purposes of visualizing board area, but its thermal performance bears comparison with the much larger SO-8.

This technical note discusses the dual ChipFET 1206-8 pin-out, package outline, pad patterns, evaluation board layout, and thermal performance.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel 1206-8 ChipFET device. The pin-out is similar to the TSOP-6 configuration, with two additional drain pins to enhance power dissipation and thus thermal performance. The legs of the device are very short, again helping to reduce the thermal path to the external heatsink/pcb and allowing a larger die to be fitted in the device if necessary.

Dual 1206-8 ChipFET

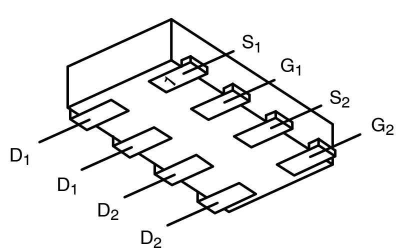


FIGURE 1.

For package dimensions see the 1206-8 ChipFET package outline drawing (http://www.vishay.com/doc?71151).

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286). This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

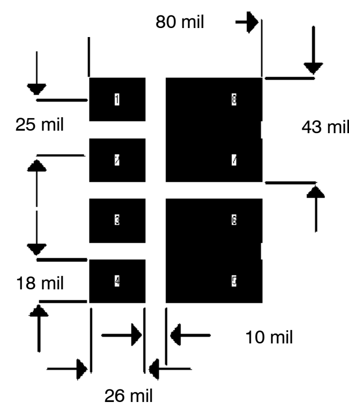


FIGURE 2. Footprint With Copper Spreading

The pad pattern with copper spreading shown in Figure 2 improves the thermal area of the drain connections (pins 5 and 6, pins 7 and 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0019 sq. in. or 1.22 sq. mm. This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the dual device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further. An example of this method is implemented on the Vishay Siliconix Evaluation Board described in the next section (Figure 3).

THE VISHAY SILICONIX EVALUATION BOARD FOR THE DUAL 1206-8

The dual ChipFET 1206-08 evaluation board measures 0.6 in by 0.5 in. Its copper pad pattern consists of an increased pad area around each of the two drain leads on the top-side—approximately 0.0246 sq. in. or 15.87 sq. mm—and vias added through to the underside of the board, again with a maximized copper pad area of approximately the board-size dimensions, split into two for each of the drains. The outer package outline is for the 8-pin DIP, which will allow test sockets to be used to assist in testing.

The thermal performance of the 1206-8 on this board has been measured with the results following on the next page. The testing included comparison with the minimum recommended footprint on the evaluation board-size pcb and the industry standard one-inch square FR4 pcb with copper on both sides of the board.

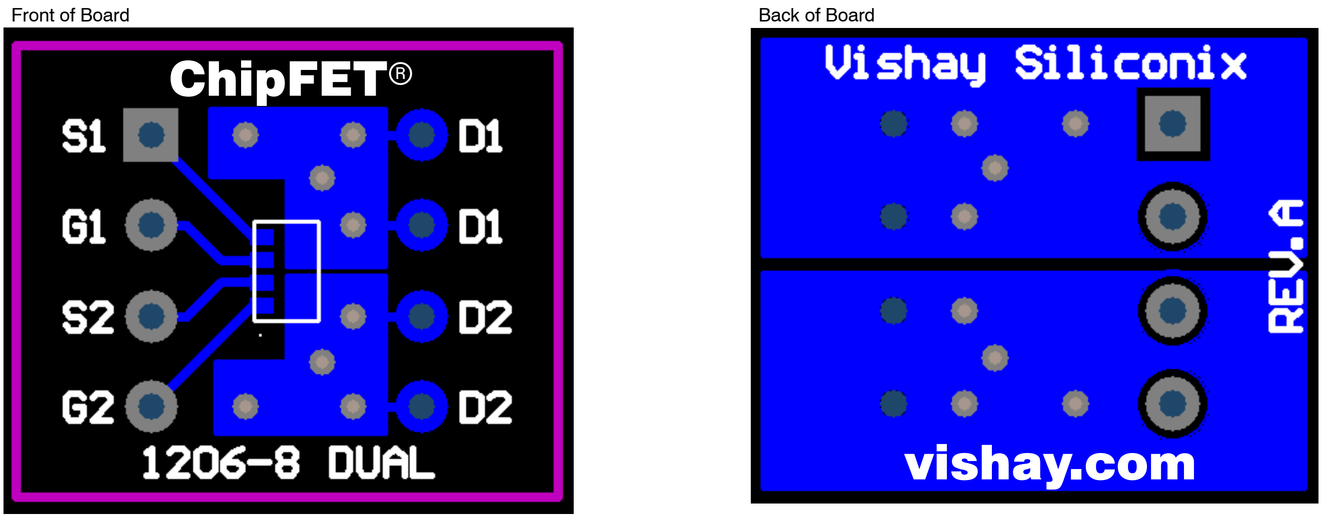


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the 1206-8 ChipFET measured as junction-to-foot thermal resistance is 30°C/W typical, 40°C/W maximum for the dual device. The "foot" is the drain lead of the device as it connects with the body. This is identical to the dual SO-8 package $R_{\Theta jf}$ performance, a feat made possible by shortening the leads to the point where they become only a small part of the total footprint area.

Junction-to-Ambient Thermal Resistance (dependent on pcb size)

The typical $R_{\Theta ja}$ for the dual-channel 1206-8 ChipFET is 90°C/W steady state, identical to the SO-8. Maximum ratings are 110°C/W for both the 1206-8 and the SO-8. Both packages have comparable thermal performance on the 1" square pcb footprint with the 1206-8 dual package having a quarter of the body area, a significant factor when considering board area.

Testing

To aid comparison further, Figure 4 illustrates ChipFET 1206-8 dual thermal performance on two different board sizes and three different pad patterns.The results display the thermal performance out to steady state and produce a graphic account on how an increased copper pad area for the drain connections can enhance thermal performance. The measured steady state values of $R_{\Theta ja}$ for the Dual 1206-8 ChipFET are :

1) Minimum recommended pad pattern (see Figure 2) on the evaluation board size of 0.5 in x 0.6 in.	185°C/W
2) The evaluation board with the pad pattern described on Figure 3.	128°C/W
3) Industry standard 1" square pcb with maximum copper both sides.	90°C/W

The results show that a major reduction can be made in the thermal resistance by increasing the copper drain area. In this example, a 57°C/W reduction was achieved without having to increase the size of the board. If increasing board size is an option, a further 38°C/W reduction was obtained by maximizing the copper from the drain on the larger 1" square PCB.

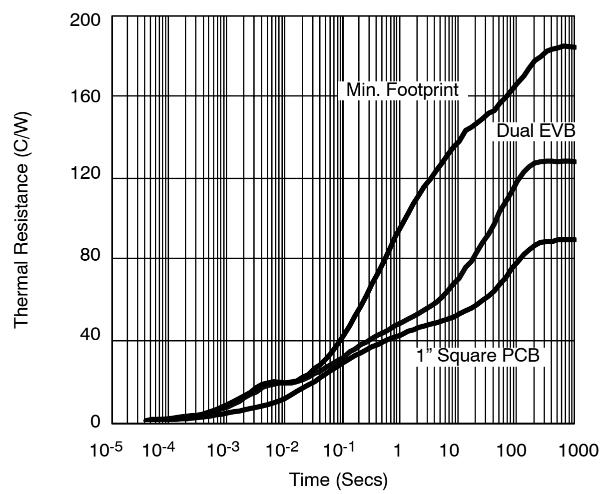


FIGURE 4. Dual 1206-8 ChipFET

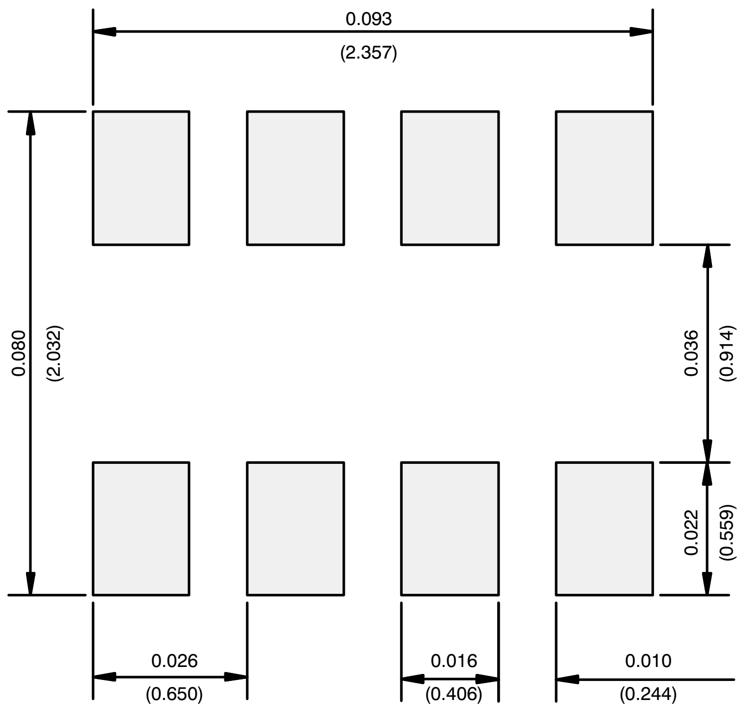
SUMMARY

The thermal results for the dual-channel 1206-8 ChipFET package display identical power dissipation performance to the SO-8 with a footprint reduction of 80%. Careful design of the package has allowed for this performance to be achieved. The short leads allow the die size to be maximized and thermal resistance to be reduced within the confines of the TSOP-6 body size.

ASSOCIATED DOCUMENT

1206-8 ChipFET Single Thermal performance, AN811, (http://www.vishay.com/doc?71126).

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

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