Preliminary **64Mx72 One Bank Registered DDR SDRAM Module**

Features

- 184-Pin Registered 8-Byte Dual In-Line Memory Module
- 64Mx72 Double Data Rate (DDR) SDRAM DIMM (64M x 4 SDRAMs)
- Performance:

		PC1600		Units
DIMM $\overline{CAS}$ Latency		3	3.5	
f_{CK}	Clock Frequency	100	125	MHz
t_{CK}	Clock Cycle	10	8.0	ns
f_{DQ}	DQ Burst Frequency	200	250	MHz

- Intended for 100 MHz applications
- Inputs and outputs are SSTL-2 compatible
- V_{DD} = 2.5Volt ± 0.2, V_{DDQ} = 2.5Volt ± 0.2
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have four internal banks for concurrent operation
- Module has one physical bank
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Differential clock inputs
- Data is read or written on both clock edges
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 3, 3.5
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- Power Down Mode
- 13/11/2 Addressing (row/column/bank)
- 7.8 µs Max. Average Periodic Refresh Interval
- Card size: 5.25" x 0.157" x 1.70"
- Gold contacts
- SDRAMs in 66-pin TSOP-II Package
- Serial Presence Detect

Description

IBMB6M64734BGA is a registered 184-Pin Double Data Rate (DDR) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as a one-bank high-speed memory array. The 64Mx72 module is a single-bank DIMM that uses eighteen 64Mx4 DDR SDRAMs in 400 mil TSOP packages. This DIMM achieves high-speed data transfer rates of up to 200 MHz.

The DIMM is intended for use in applications operating from 100 MHz to 125 MHz clock speeds with data rates of 200 to 250 MHz. All control and address signals are re-driven through registers to the DDR SDRAM devices. The control and address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge.

A phase-locked loop (PLL) on the DIMM is used to re-drive the differential clock signals to both the DDR SDRAM devices and the registers, thus minimizing system clock loading. Clock enable (CKE0) controls all devices on the DIMM.

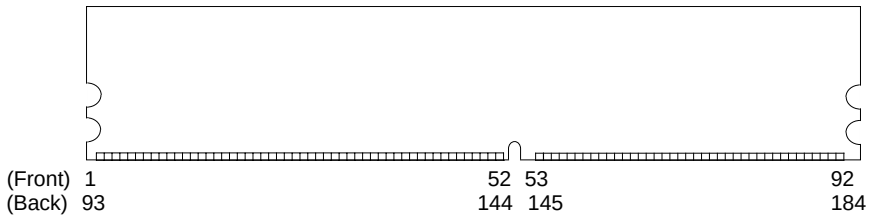
Prior to any access operation, the device $\overline{CAS}$ latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A12 and I/O inputs BA0 and BA1 using the mode register set cycle. The DIMM $\overline{CAS}$ latency exceeds the SDRAM device specification by one clock due to the address and control signals being clocked to the SDRAM devices.

These DIMMs are manufactured using raw cards developed for broad industry use by IBM as reference designs. The use of these common design files will minimize electrical variation between suppliers.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The last 128 bytes are available to the customer.

All IBM 184 DDR SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

Card Outline



Pin Description

CK0, $\overline{CK0}$	Differential Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0	Clock Enable	CB0 - CB7	Check Bit Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQS0-DQS17	Bidirectional data strobes
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power (2.5V)
$\overline{WE}$	Write Enable	V_{DDQ}	Supply voltage for DQs (2.5V)
$\overline{S}0$	Chip Select	V_{SS}	Ground
A0 - A9, A11, A12	Address Inputs	NC	No Connect
A10/AP	Address Input/Autoprecharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data Input/Output
$\overline{RESET}$	Reset pin	SA0-SA2	Serial Presence Detect Address Inputs
V_{REF}	Reference voltage for SSTL_2 inputs	V_{DDSPD}	Serial EEPROM positive power supply (2.5 V)

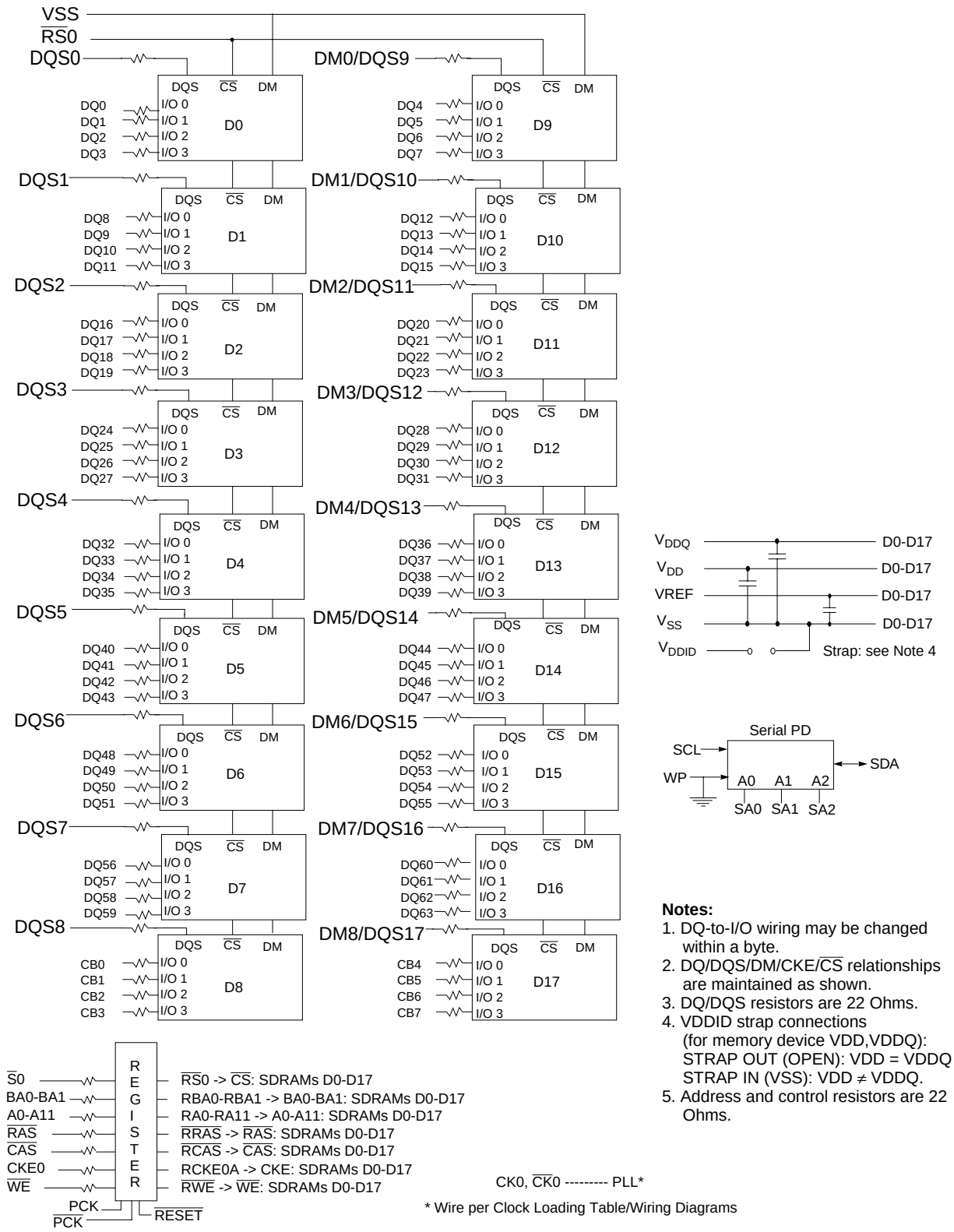
184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)				Back Side (left side 93 -144, right side 145 -184)			
Pin #	x72 ECC	Pin #	x72 ECC	Pin #	x72 ECC	Pin #	x72 ECC
1	VREF	48	A0	93	VSS	140	DQS17
2	DQ0	49	CB2	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	CB6
4	DQ1	51	CB3	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DSQ9	144	CB7
6	DQ2	KEY		98	DQ6	KEY	
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	RESET	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DQS10	153	DQ44
16	NC	62	VDDQ	108	VDD	154	$\overline{RAS}$
17	NC	63	$\overline{WE}$	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	$\overline{CAS}$	111	NC	157	$\overline{S0}$
20	DQ11	66	VSS	112	VDDQ	158	NC
21	CKE0	67	DQS5	113	BA2	159	DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	NC	121	DQ22	167	NC
30	VDDQ	76	NC	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	CB4	180	VDDQ
43	A1	89	VSS	135	CB5	181	SA0
44	CB0	90	NC	136	VDDQ	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	$\overline{CK0}$	184	VDDSPD
47	DQS8			139	VSS		
NC = No Connect; NU = Not Useable; DU = Do Not Use							

Ordering Information

Part Number	Organization	Speed	SDRAM CAS Latency	Leads	Dimension	Power V_{DD}/V_{DDQ}
IBMB6M64734BGA - 8NT	64Mx72	PC1600	3	Gold	5.25" x 1.7" x 0.157"	2.5 V/2.5 V

64x72 ECC DDR Registered SDRAM DIMM Block Diagram (1 Bank, x4 DDR SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS resistors are 22 Ohms.
4. VDDID strap connections (for memory device VDD,VDDQ): STRAP OUT (OPEN): VDD = VDDQ STRAP IN (VSS): VDD ≠ VDDQ.
5. Address and control resistors are 22 Ohms.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK}$0	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}$0	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0,1	(SSTL)	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11, A12, A10/AP	(SSTL)	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	(SSTL)	—	Data and Check Bit Input/Output pins. Check bits are only applicable on the x72 DIMM configurations.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0-DQS17	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
$\overline{RESET}$	(LVCMOS)	Active Low	Asynchronously forces all register outputs low when $\overline{RESET}$ is low. This signal can be used during power up to ensure CKE0 and CKE1 are low and SDRAM DQSs are Hi-Z.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Serial Presence Detect (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total number of bytes in Serial PD Device	256	08	
2	Fundamental Memory Type	SDRAM DDR	07	
3	Number of Row Addresses on Assembly	13	0D	
4	Number of Column Addresses on Assembly	11	0B	
5	Number of Physical Banks on DIMM	1	01	
6-7	Data Width of Assembly	x72	4800	
8	Voltage Interface Level of this Assembly	SSTL 2.5V	04	
9	SDRAM Device Cycle Time at Maximum CL (CLX = 2.5)	8.0ns	80	1
10	SDRAM Device Access Time from Clock at CL=2.5	0.8ns	80	
11	DIMM Configuration Type	ECC	02	
12	Refresh Rate/Type	7.8µs/SR	82	
13	Primary SDRAM Device Width	x4	04	
14	Error Checking SDRAM Device Width	x4	04	
15	SDRAM Device Attributes: Minimum Clock Delay, Random Column Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	2, 4, 8	0E	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	2, 2.5	0C	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	1	02	
21	SDRAM Module Attributes	Registered with PLL, Differential clock	26	
22	SDRAM Device Attributes: General	$V_{DD} \pm 0.2V$	80	
23	Minimum Clock Cycle at CLX-0.5 (CL = 2)	10.0ns	A0	1
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-0.5 (CL = 2)	$\pm$ 0.8ns	80	
25	Minimum Clock Cycle Time at CLX-1 (CL = 1.5)	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 1.5)	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	20.0ns	50	
28	Minimum Row Active to Row Active Delay (t_{RRD})	15.0ns	3C	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})	20.0ns	50	
30	Minimum Active to Precharge Time (t_{RAS})	50.0ns	32	
31	Module Bank Density - 64Mx72	512MB	80	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. “R” = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte “R”.
5. ww = Binary coded decimal week code, 01-52 (Decimal) → 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).
8. Setup and hold values assume a 1 Volt/ns slew rate.

Serial Presence Detect (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
32	Address and Command Setup Time before Clock	1.1ns	B0	8
33	Address and Command Hold Time after Clock	1.1ns	B0	
34	Data/Data Mask Input Setup Time before Clock	0.6ns	60	
35	Data/Data Mask Input Hold Time after Clock	0.6ns	60	
36-61	Reserved	Undefined	00	
62	SPD Revision	0	00	
63	Checksum for Bytes 0 - 62	Checksum Data	cc	2
64-71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location		xx	
73-90	Module Part Number	ASCII 'B6M64734BGA -8NT'	42364D3634373334424741 2D384E54202020	3, 4
91-92	Module Revision Code	"R" plus ASCII blank	rr20	4
93-94	Module Manufacturing Date	Year/Week Code	yyww	5, 6
95-98	Module Serial Number	Serial Number	ssssssss	7
99-127	Reserved	Undefined	00	
128-255	Open for Customer Use	Undefined	00	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. "R" = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte "R".
5. ww = Binary coded decimal week code, 01-52 (Decimal) → 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).
8. Setup and hold values assume a 1 Volt/ns slew rate.

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}		–0.5 to V_{DDQ}+ 0.5	V
V_{IN}	Voltage on Inputs relative to V_{SS}	SDRAM device	–0.5 to +2.7	V
		Serial PD device	-0.3 to +6.5	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}		–0.5 to +2.7	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}		–0.5 to +2.7	V
V_{DDSPD}	Voltage on V_{DDSPD} supply relative to V_{SS}		–0.3 to +5.5	V
T_A	Operating Temperature (Ambient)		0 to +70	°C
T_{STG}	Storage Temperature (Plastic)		–55 to +150	°C
P_D	Power Dissipation		TBD	W
I_{OUT}	Short Circuit Output Current		50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: CK0, $\overline{CK}$0	C_{I1}	7	pF	1
Input Capacitance: A0-A12, BA0, BA1, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, CKE0, $\overline{SO}$	C_{I2}	7	pF	1
Input Capacitance: $\overline{RESET}$	C_{I3}	7	pF	1
Input Capacitance: SA0-SA2, SCL	C_{I4}	9	pF	1
Input/Output Capacitance: DQ0-63, DQS0-17, CB0-7	C_{IO1}	10	pF	1, 2
Input/Output Capacitance: SDA	C_{IO2}	11	pF	

1. V_{DDQ} = V_{DD} = 2.5V 0.2V, f = 100 MHz, T_A = 25°C, V_{OUT} (DC) = $V_{DDQ/2}$, V_{OUT} (Peak to Peak) = 0.2V.
2. DM inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

Electrical Characteristics and DC Operating Conditions

($0^{\circ}C \leq T_A \leq 70^{\circ}C$; V_{DDQ} = 2.5V ± 0.2V, V_{DD} = + 2.5V ± 0.2V, see AC Characteristics)

Symbol	Parameter		Min	Max	Units	Notes
V_{DD}	Supply Voltage		2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage		2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage I/O Supply Voltage		0	0	V	
V_{REF}	I/O Reference Voltage		$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	1, 2
V_{TT}	I/O Termination Voltage (System)		$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	1, 3
V_{DDSPD}	Supply Voltage SPD Supply Voltage		2.3	2.7	V	
$V_{IH(DC)}$	Input High (Logic1) Voltage	DQ0-63, CB0-7, DQS0-17	$V_{REF} + 0.15$	$V_{DDQ} + 0.3$	V	1
		Address and control inputs	$V_{REF} + 0.18$	$V_{DDQ} + 0.3$		
		$\overline{RESET}$	1.7	$V_{DDQ} + 0.3$		
$V_{IL(DC)}$	Input Low (Logic0) Voltage	DQ0-63, CB0-7, DQS0-17	– 0.3	$V_{REF} - 0.15$	V	1
		Address and control inputs	– 0.3	$V_{REF} - 0.18$		
		$\overline{RESET}$	– 0.3	0.8		
$V_{IN(DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs		– 0.3	$V_{DDQ} + 0.3$	V	1
$V_{ID(DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs		0.36	$V_{DDQ} + 0.6$	V	1, 4
I_I	Input Leakage Current Any input $0V \leq V_{IN} \leq V_{DD}$ (All other pins not under test = 0V)	Address and control inputs	– 5	5	µA	1
		DQ0-63, CB0-7, DQS0-17	– 5	5		
		CK and $\overline{CK}$	– 10	10		
I_{OZ}	Output Leakage Current (DQs are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$	DQ0-63, CB0-7, DQS0-17	– 5	5	µA	1
		SDA	– 1	1		
I_{OH}	Output High Current (V_{OUT} = 1.95V)		– 16.8		mA	1
I_{OL}	Output Low Current (V_{OUT} = 0.35V)		16.8		mA	1

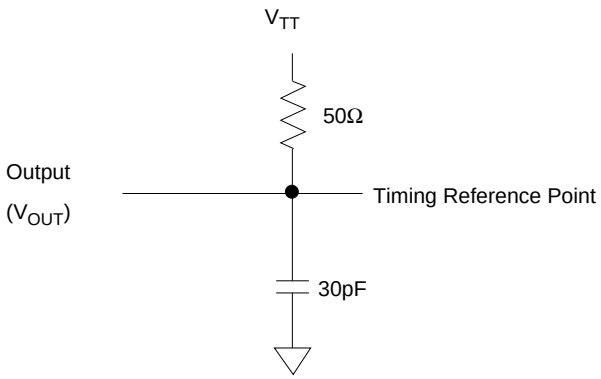
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuit Diagram



AC Operating Conditions ($0\,^{\circ}C \le T_A \le 70\,^{\circ}C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter/Condition		Min	Max	Unit	Notes
$V_{IH(AC)}$	Input High (Logic 1) Voltage.	DQ0-63, CB0-7, DQS0-17	V_{REF} + 0.31		V	1, 2
		Address and control inputs	V_{REF} + 0.35			
$V_{IL(AC)}$	Input Low (Logic 0) Voltage.	DQ0-63, CB0-7, DQS0-17		V_{REF} – 0.31	V	1, 2
		Address and control inputs		V_{REF} – 0.35		
$V_{ID(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs		0.7	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX(AC)}$	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs		$(0.5 \times V_{DDQ}) - 0.2$	$(0.5 \times V_{DDQ}) + 0.2$	V	1, 2, 4
f_{SSC}	SSC modulation frequency		30	50	KHz	
Δ_{SSC}			0	-.50	%	

1. Input slew rate = 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal $0.5 \times V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents ($0\ ^\circ C \le T_A \le 70\ ^\circ C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics)

Symbol	Parameter/Condition	mA	Notes
I_{DD0}	**Operating Current**: one logical bank; active / precharge; $t_{RC} = t_{RC\ MIN}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	2190	1
I_{DD1}	**Operating Current**: one bank; active / read / precharge; Burst = 2; $t_{RC} = t_{RC\ MIN}$; CL = 2.5; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	2460	1
I_{DD2P}	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE ≤ $V_{IL\ MAX}$	1100	1
I_{DD2N}	**Idle Standby Current:** $\overline{CS} \ge V_{IH\ MIN}$; all banks idle; CKE ≥ $V_{IH\ MIN}$; address and control inputs changing once per clock cycle	1380	1
I_{DD3P}	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE ≤ $V_{IL\ MAX}$	1110	1
I_{DD3N}	**Active Standby Current**: one bank; active / precharge; $\overline{CS} \ge V_{IH\ MIN}$; CKE ≥ $V_{IH\ MIN}$; $t_{RC} = t_{RAS\ MAX}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1740	1
I_{DD4R}	**Operating Current:** one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; I_{OUT} = 0mA	3180	1
I_{DD4W}	**Operating Current**: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 2.5	2910	1
I_{DD5}	**Auto-Refresh Current**: $t_{RC} = t_{RFC\ MIN}$	3720	1, 3
	t_{RC} = 7.8 µs	1144	
I_{DD6}	**Self-Refresh Current**: CKE ≤ 0.2V	61	1, 2
I_{DD7}	**Operating current**: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC\ MIN}$; I_{OUT} = 0mA.	TBD	1

1. I_{DD} specifications are valid after the SDRAMs are properly initialized.
2. Enables on-chip refresh and address counters.
3. Current at 7.8 µs is time averaged value of I_{DD5} at $t_{RFC\ MIN}$ and I_{DD2P} over 7.8 µs.

Electrical Characteristics and AC Timing - Absolute Specifications

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		PC 1600		Unit	Notes
			Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.8	+ 0.8	ns	1, 2, 3, 4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.8	+ 0.8	ns	1, 2, 3, 4
t_{CH}	CK high-level width		0.45	0.55	t_{CK}	1, 2, 3, 4
t_{CL}	CK low-level width		0.45	0.55	t_{CK}	1, 2, 3, 4
t_{CK}	Clock cycle time	CL = 3.5	8	12	ns	1, 2, 3, 4
		CL = 3.0	10	12	ns	1, 2, 3, 4
t_{DH}	DQ and DM input hold time		0.6		ns	1, 2, 3, 4, 18, 19
t_{DS}	DQ and DM input setup time		0.6		ns	1, 2, 3, 4, 18, 19
t_{DIPW}	DQ and DM input pulse width (each input)		2		ns	1, 2, 3, 4
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$		– 0.8	+ 0.8	ns	1, 2, 3, 4, 5
t_{LZ}	Data-out low-impedance time from CK/$\overline{CK}$		– 0.8	+ 0.8	ns	1, 2, 3, 4, 5
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)			+ 0.6	ns	1, 2, 3, 4
t_{DQSQA}	DQS-DQ skew (DQS & all DQ signals)			+ 0.6	ns	1, 2, 3, 4
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time		t_{CH} or t_{CL}		t_{CK}	1, 2, 3, 4
t_{QH}	Data output hold time from DQS		t_{HP} – 1.0ns		t_{CK}	1, 2, 3, 4
t_{DQSS}	Write command to first DQS latching transition		0.75	1.25	t_{CK}	1, 2, 3, 4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		t_{CK}	1, 2, 3, 4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		t_{CK}	1, 2, 3, 4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		t_{CK}	1, 2, 3, 4
t_{MRD}	Mode register set command cycle time		16		ns	1, 2, 3, 4
t_{WPRES}	Write preamble setup time		0		ns	1, 2, 3, 4, 7
t_{WPST}	Write postamble		0.40	0.60	t_{CK}	1, 2, 3, 4, 6
t_{WPRE}	Write preamble		0.25		t_{CK}	1, 2, 3, 4
t_{IH}	Address and control input hold time (fast slew rate)		1.1		ns	2, 3, 4, 11, 13, 14
t_{IS}	Address and control input setup time (fast slew rate)		1.1		ns	2, 3, 4, 11, 13, 14
t_{IH}	Address and control input hold time (slow slew rate)		1.1		ns	2, 3, 4, 12, 13, 14, 17
t_{IS}	Address and control input setup time (slow slew rate)		1.1		ns	2, 3, 4, 12, 13, 14, 17
t_{IPW}	Input pulse width				ns	2, 3, 4, 14
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}	1, 2, 3, 4
t_{RPST}	Read postamble		0.40	0.60	t_{CK}	1, 2, 3, 4

Electrical Characteristics and AC Timing - Absolute Specifications

($0\ °C \le T_A \le 70\ °C$; $V_{DDQ} = 2.5V \pm 0.2V$; $V_{DD} = 2.5V \pm 0.2V$, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	PC 1600		Unit	Notes
		Min	Max		
t_{RAS}	Active to Precharge command	50	120,000	ns	1, 2, 3, 4
t_{RC}	Active to Active/Auto-refresh command period	70		ns	1, 2, 3, 4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period	80		ns	1, 2, 3, 4
t_{RCD}	Active to Read or Write delay	20		ns	1, 2, 3, 4
t_{RAP}	Active to Read Command with Autoprecharge	20		ns	1, 2, 3, 4
t_{RP}	Precharge command period	20		ns	1, 2, 3, 4
t_{RRD}	Active bank A to Active bank B command	15		ns	1, 2, 3, 4
t_{WR}	Write recovery time	15		ns	1, 2, 3, 4
t_{DAL}	Auto precharge write recovery + precharge time	$(t_{WR} \div t_{CK}) + (t_{RP} \div t_{CK})$		t_{CK}	1, 2, 3, 4, 16
t_{WTR}	Internal write to read command delay	1		t_{CK}	1, 2, 3, 4
t_{XSNR}	Exit self-refresh to non-read command	80		ns	1, 2, 3, 4
t_{XSRD}	Exit self-refresh to read command	200		t_{CK}	1, 2, 3, 4
t_{REFI}	Average Periodic Refresh Interval		7.8	µs	1, 2, 3, 4, 8
t_{QCS}	$\overline{QFC}$ setup time on Read	0.9	1.1	t_{CK}	1, 2, 3, 4, 15
t_{QCH}	$\overline{QFC}$ hold time on Read	0.4	0.6	t_{CK}	1, 2, 3, 4, 15
t_{QCSW}	Delay from CK edge of write command to $\overline{QFC}$ low on write		4.0	ns	1, 2, 3, 4, 9, 15
t_{QCHW}	$\overline{QFC}$ hold time on write	1.25	2.0	ns	1, 2, 3, 4, 10, 15

Electrical Characteristics and AC Timing - Absolute Specifications Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. $\overline{QFC}$ is enabled as soon as possible after the rising CK edge that registers the Write command.
10. $\overline{QFC}$ is disabled as soon as possible after the last valid DQS edge transitions Low.
11. For command/address input slew rate ≥ 1.0V/ns. Slew rate is measured between V_{OH}(AC) and V_{OL}(AC).
12. For command/address input slew rate ≥ 0.5V/ns and < 1.0V/ns. Slew rate is measured between V_{OH}(AC) and V_{OL}(AC).
13. CK/$\overline{CK}$ slew rates are ≥ 1.0V/ns.
14. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
15. The specified timing is guaranteed assuming $\overline{QFC}$ is connected to a test load consisting of 20pF to ground and a pull up resistor of 150 ohms to V_{ddq}.
16. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

(Notes continue on the following page.)

17. An input setup and hold time derating table is used to increase t_{IS} and t_{IH} in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Δt_{IS}	Δt_{IH}	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+ 50	0	ps	1, 2
0.3 V/ns	+ 100	0	ps	1, 2

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

18. An input setup and hold time derating table is used to increase t_{DS} and t_{DH} in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Δt_{DS}	Δt_{DH}	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+ 75	+ 75	ps	1, 2
0.3 V/ns	+ 150	+ 150	ps	1, 2

1. I/O slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

19. An I/O Delta Rise, Fall Derating table is used to increase t_{DS} and t_{DH} in the case where DQ, DM, and DQS slew rates differ.

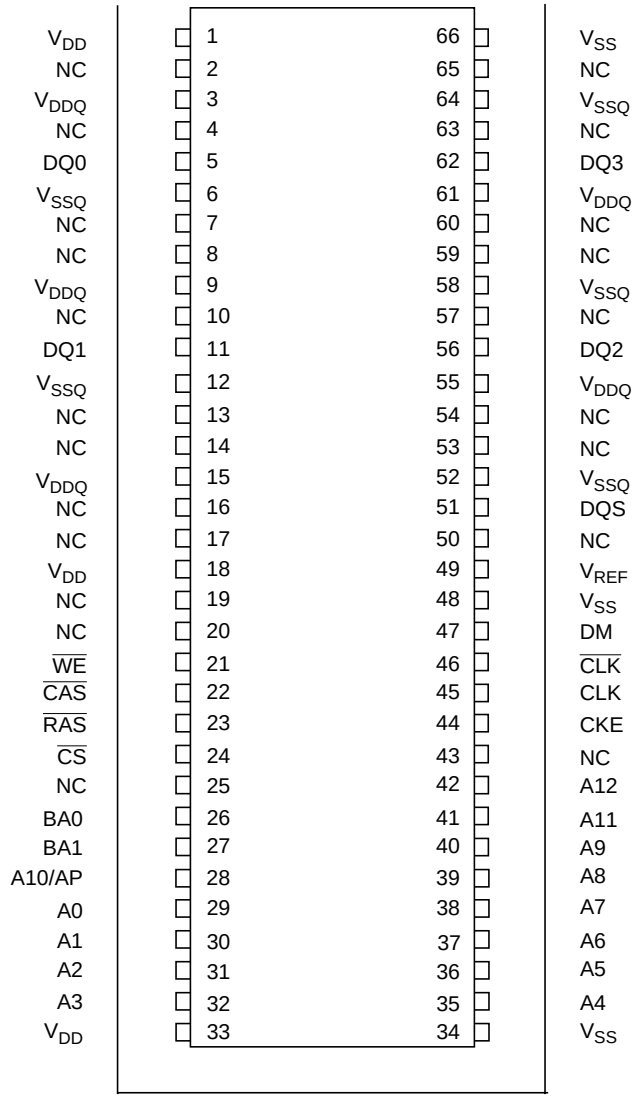
Delta Rise and Fall Rate	Δt_{DS}	Δt_{DH}	Unit	Note
0.0 ns/V	0	0	ps	1, 2, 3, 4
0.25 ns/V	+ 50	+ 50	ps	1, 2, 3, 4
0.5 ns/V	+ 100	+ 100	ps	1, 2, 3, 4

1. Input slew rate is based on the lesser of the slew rates determined by either $V_{IH\ (AC)}$ to $V_{IL\ (AC)}$ or $V_{IH\ (DC)}$ to $V_{IL\ (DC)}$, similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns
   Delta rise, fall = (1/0.5) - (1/0.4) [ns/V]
   = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

Wiring and Topology

This section contains the information needed to understand the timing relationships presented in the AC Characteristics section. Because the system designer must measure all signals at the first receiving device (SDRAM DQ pin for data, register input pin for address and controls, and PLL check input pin for clock), the following pages provide detailed information on these inputs. In some cases DIMM timing adjustments are listed in the specifications, and in some cases it is recommended that the customer determine this information via simulation. This section enables the customer to understand the device pinouts on the DIMM, the net structures, and the loading associated with these devices. For detailed timing analysis, contact an IBM Marketing Representative for simulation models. System-level modeling is strongly recommended to determine delay adders of the entire net structure in the customer's application.

Pin Assignments for the 256 Mb DDR SDRAM Planar Component (top view)



64M x 4 x 4 Bank

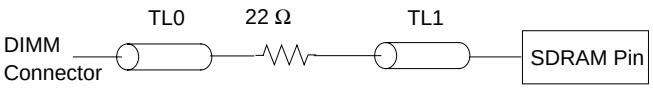
The table below describes the DQ and CB wiring information for each SDRAM on the DIMM. Note that the DQ wiring is different from that described in the Block Diagram.

SDRAM Wiring Information

DQ SDRAM Designator	DQ SDRAM Pin Number	Device Position to DIMM Tab I/O[1]																
		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17
DQ0	5	3	11	19	27	35	43	51	59	CB3	4	12	20	28	36	44	52	60	CB4
DQ1	11	2	10	18	26	34	42	50	58	CB2	5	13	21	29	37	45	53	61	CB5
DQ2	56	1	9	17	25	33	41	49	57	CB1	6	14	22	30	38	46	54	62	CB6
DQ3	62	0	8	16	24	32	40	48	56	CB0	7	15	23	31	39	47	55	63	CB7

1. These numbers can be associated with the corresponding DIMM tab pin by referencing the DIMM connector pinout on pages 2 and 3 of this document. Example: DQ7 at the DIMM tab (pin 99) is wired to SDRAM device position D9, pin 62.

Data, CB, DQS, and DM Net Structures



Note: Transmission Lines (TL) are represented as cylinders and are labeled with length designators. These are the only lines which represent physical trace segments. For more detailed topology information please refer to the DDR SDRAM Registered DIMM Design Specification.

Trace Lengths for Data Net Structure

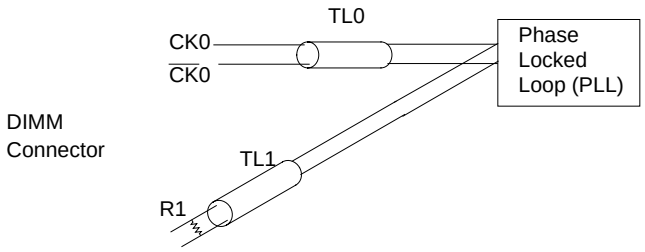
TL0		TL1		Total		Unit
Min	Max	Min	Max	Min	Max	
0.13	0.19	0.95	1.02	1.13	1.15	inches

The table below describes the input wiring for each clock on the DIMM.

Clock Input Wiring

CK0, $\overline{CK0}$
PLL CLK input pin 13, 14

Clock Topology



Trace Lengths

TL0	TL1	R1 [ohms]	Unit
1.00	0.20	120	inches

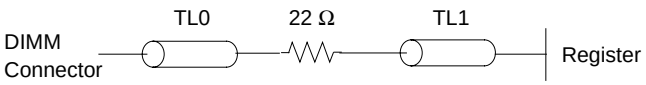
The table below describes the address and control information for each signal on the DIMM.

Register Input Wiring

Register Pin Number	Register 1 Signal	Register 2 Signal	Notes
25	NC	A0	1
26	NC	A10	1
29	CKE0	BA1	
30	A12	NC	1
31	A11	BA0	
32	A9	$\overline{RAS}$	
33	A7	$\overline{WE}$	
40	A8	NC	1
41	A5	NC	1
42	A6	NC	1
43	A4	NC	1
44	A3	$\overline{CAS}$	
47	A2	$\overline{S}0$	
48	A1	NC	1

1. Register signals corresponding to NC inputs are tied to ground.

Address/Control Signal Net Structure



Trace Lengths

TL0		TL1		Units
Min	Max	Min	Max	
0.13	0.26	0.56	0.66	inches

Note: Each signal has one register input load in order to aid in system level timings.

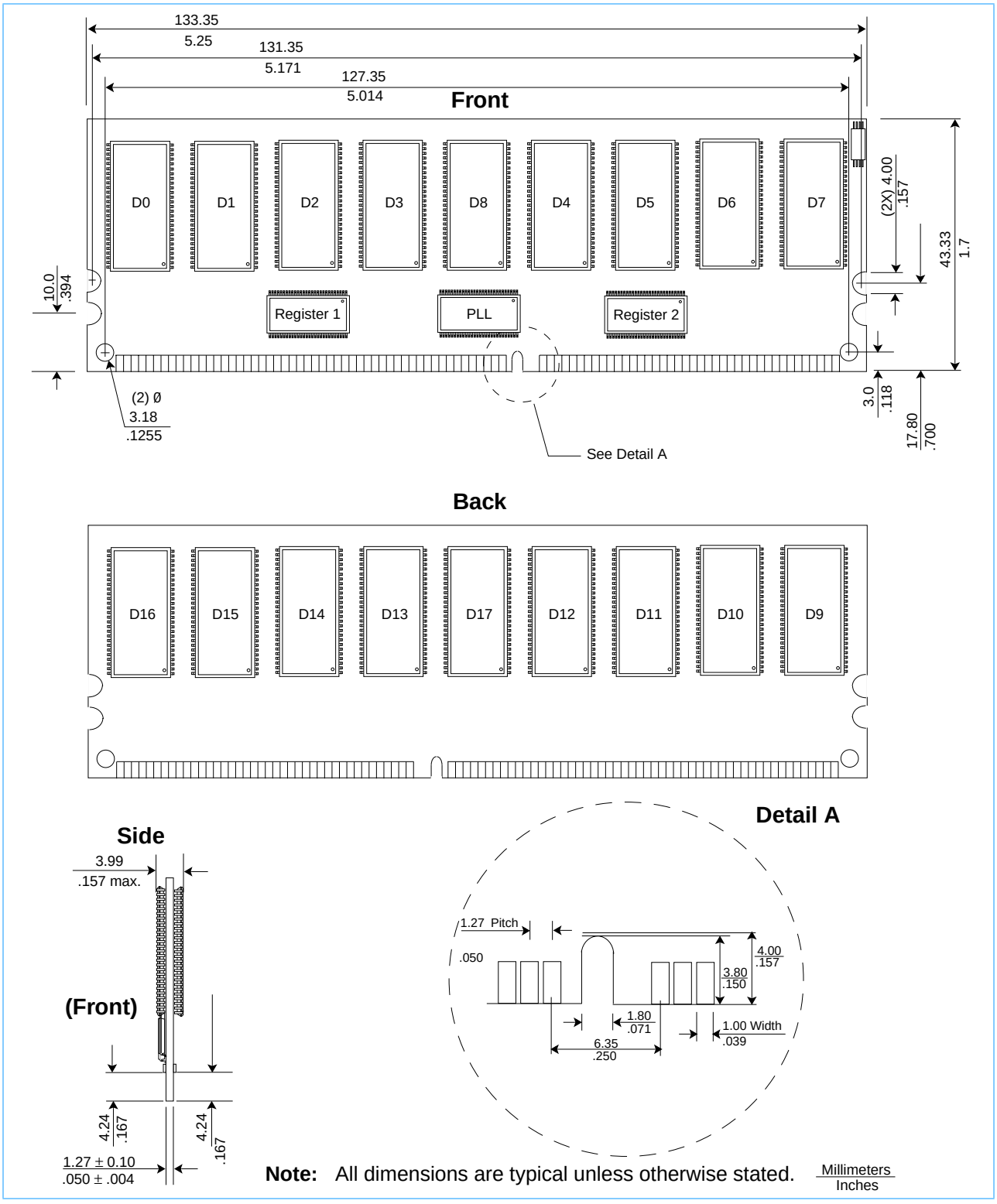
Functional Description and Timing Diagrams

Refer to IBM 256Mb Synchronous DDR DRAM datasheet (29L0011.E36997A) for functional description and timing diagrams.

Refer to the IBM Application Note *Power Up and Power Management on DDR RDIMMs* for new DDR DIMM features that facilitate controlled power up and minimize power consumption.

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Layout Drawing for 64Mx72 One Bank Registered DIMM



Revision Log

Rev	Contents of Modification
3/00	Initial release
1/01	upates to spec.

Printed in the United States of America January 2001

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06K6597.H02812A
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