F71808A

Smart LPC IO With CIR & Power Saving Function

Release Date: Dec, 2010
Version: V0.18P

F71808A Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2010/2	-	Preliminary Version
V0.11P	2010/3	-	Add Application Circuit and Register Description
V0.12P	2010/4	7 11-15 16	Update GPIO description Update pin assignment Update strapping setting
V0.13P	2010/5	106 42-110 15 39, 40 12, 14	1. Add Application Circuits 2. Update Register 3. Modify pin21 to OD pin 4. Add CIR and CPT function descriptions 5. GPIO 05, 30, 31 support scan code
V0.14P	2010/5	116 15 9, 12, 14,15 39	1. Update reference circuit 2. Modify pin17 description 3. Add SUS_ACK# and SUS_WARN# multi function on pin 19, 45, 49 4. Add scan code function description
V0.15P	2010/6	9, 15, 16 12, 14 12, 17 12-16 46 48, 49 49, 50 50, 51 53 54 58 74 94 100 102 112 117-125 10	1. Remove SUS_ACK# (pin 19), Add WDTRST# (pin 23) 2. Rename SUS_WARN2# and SUS_ACK2# (pin 45, 49) 3. Correct STRAP_PWOK default setting 4. Update Pin Type 5. Update LDN Register – Index 07h 6. Update Multi-Function Select Register 0 – Index 28h 7. Update Multi-Function Select Register 1 – Index 29h 8. Update Multi-Function Select Register 2 – Index 2Ah 9. Update Multi-Function Select Register 3 – Index 2Bh 10. Update Multi-Function Select Register 4 – Index 2Ch 11. Update RS485 Enable Register – Index F0h 12. Update Fan Temperature Adjust Select Register – Index 96h 13. Update GPIO 23 description 14. Update Watchdog Timer Configuration Register 2 – Index 06h 15. Update EuP Enable Register – Index E0h 16. Update Intel DSW Delay Select Register – Index FCh 17. Update Reference Circuits 18. Correct Pin Type
V0.16P	2010/8	93 13, 15 96 96, 97 91 91, 92 92 14, 36-38 110 53 55, 56 12-15	1. Correct Typo 2. Update Pin Description for GPIO05, 30 and 31 3. Update GPIO2 Input Detection Select Register – Index D5h 4. Update GPIO2 Event Status Register – Index D6h 5. Update Event PME Enable Register – Index C4h 6. Add GPIO3 Input Detection Select Register – Index C5h 7. Add GPIO3 Event Status Register – Index C6h 8. Correct “S3_Gate” name 9. Correct Power Sequence Control Register – Index F7h bit 1 name 10. Update Multi-Function Select Register 2 – Index 2Ah 11. Update Multi-Function Select Register 4 – Index 2Ch 12. Correct PWR name VCC to 3VCC
V0.17P	2010/9	52	1. Update Multi-Function Select Register 2 – Index 2Ah

		15	2. Correct PWOK Pin Type
V0.18P	2010/12	89 50	1. Add Auto Swap Register — Index FEh (Powered by VBAT) bit 3 2. Update Multi-Function Select Register 1 — Index 29h bit 5 description

Table of Content

1. General Description

The F71808A which is the featured IO chip for PC system equippes one UART Port, Hardware Keyboard Controller, Hardware Monitor, ACPI management function, CIR with RC6 and SMK QP protocols supported and 27 GPIO pins. The F71808A integrated with hardware monitor, 6 sets of voltage sensor, 3 sets of creative auto-controlling fans and temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external for temperature sensing. Besides, HWM also integrated AMD TSI interface and Intel PECI/Ibex SMBus interfaces for new platform temperature reading. F71808A also fully supports PECI 3.0. For AMD platform, the F71808A provides the power sequence controller function which is selected by pin power on strapping.

The F71808A provides flexible features for multi-directional application. For instance, provides GPIO pins which can be programmed by register setting, accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Auto-Linear, Auto-Stage and Manual Mode for users' selection.

A power saving function which is in order to save the current consumption when the system is in the soft off state is also integrated a power saving function. The power saving function supports that system boot-on not only by pressing the power button but also by the wake-up event. When the system enters the S4/S5 state, F71808A can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be simulated to G3-like state when system enters the S4/S5 states. At the G3-like state, the F71808A consumes the 5VSB power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfil a low power consumption system which supports a wake up function.

The F71808A is powered by 3.3V and 5VSB voltage, with the LPC interface in 64-TQFP green package.

2. Feature List

- **General Functions**
  - Comply with LPC Spec. 1.1
  - Support DPM (Device Power Management), ACPI
  - Support AMD power sequence controller
  - Provides one UART, Hardware KBC
  - H/W monitor functions
  - Watch Dog Timer function
  - LED blink funciton
  - Support AMD TSI interface

- Intel PECI 3.0 and Ibex SMBus interface
- 24/48 MHz clock input
- Packaged in 64-TQFP and powered by 3.3VCC
- Support CIR with RC6 and SMK QP protocols
- Support Intel Cougar Point Timing
- BEEP function
- 27 GPIO Pins

UART

- High-speed 16C550 compatible UART with 16-byte FIFOs
- Fully programmable serial-interface characteris
- Baud rate up to 115.2K

Keyboard Controller

- LPC interface support serial interrupt channel 1, 12.
- Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
- Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.
- Keyboard's scan code support set1, set2.
- Programmable compatibility with the 8042.
- Support both interrupt and polling modes.
- Hardware Gate A20 and Hardware Keyboard Reset.

Hardware Monitor Functions

- 2 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- Temperature range -40℃~127℃
- Integrate AMD TSI interface
- Integrate PECI 3.0 spec.
- Integrate Ibex SMBus interface
- 6 sets voltage monitoring (3 external and 3 internal powers)
- 3 fan speed monitoring inputs
- 1 PWM fan (CPU) and 2 PWM/DC fan outputs (support 3 wire and 4 wire fans)
- Support 2 sets auto fan control and 1 set manual fan control.
- Auto Stage mode (4-Limit and 5-Stage)/Auto Linear mode/Manual mode
- Issue PME# and OVT# hardware signals output
- WATCHDOG comparison of all monitored values

Watch Dog Timer

- Time resolution minute/second by option
- Maximum 256 minutes or 256 seconds
- Output signal from WDTRST# pin

- **GPIO**
  - GPIO 00 and GPIO 01 can control the duty of PWM pin
  - GPIO 20-26 support event input for wakeup function
  - GPIO22-25 supports High/Low/Pulse/Level mode option
  - GPIO22-25 supports interrupt event by PME/SERIRQ
  - 27 GPIO pins for flexible application
  - GPIO05, GPIO 30 and GPIO 31 support scan code

- **Support AMD Power Sequence Controller**

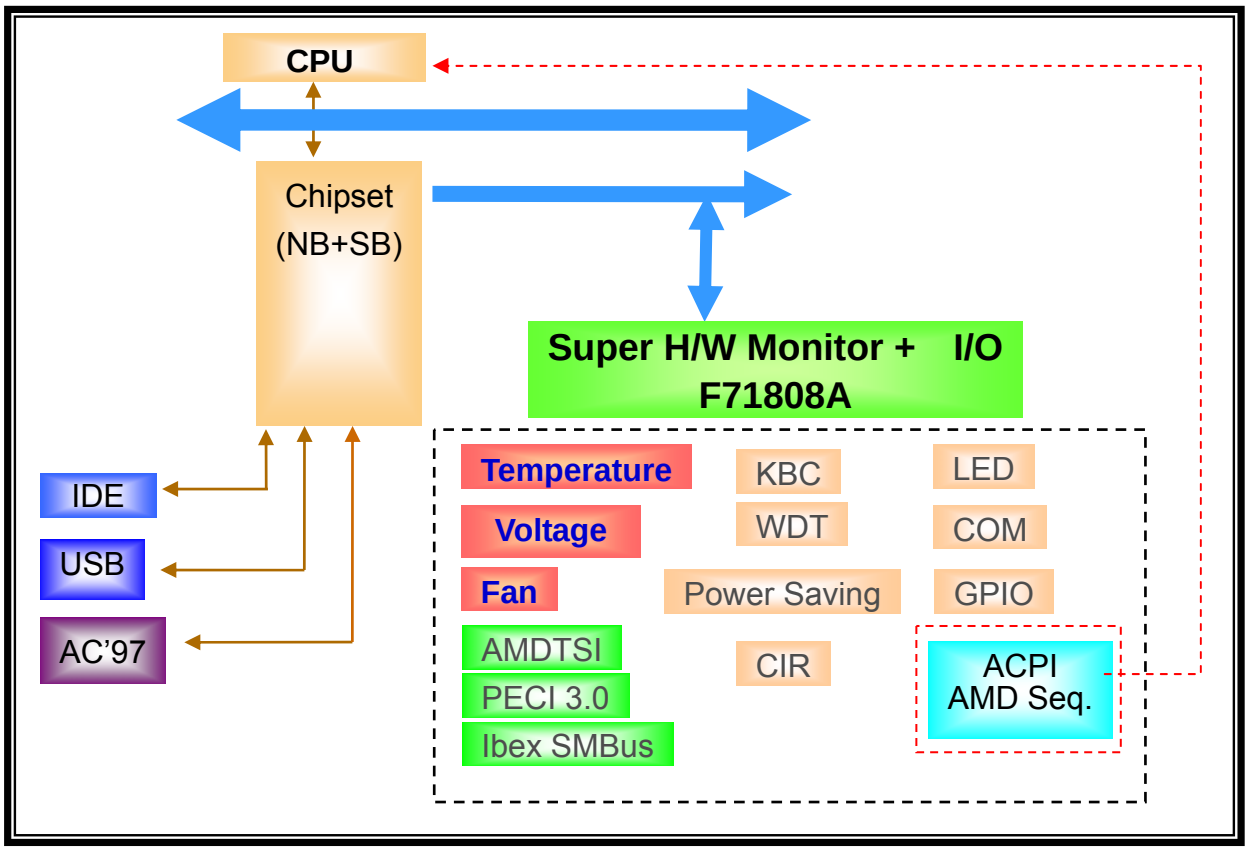
- **Power Saving Controller**
  - ACPI Timing and Power Control
  - Wake-up Supported

- **Package**
  - 64-pin TQFP Green Package

3. Key Specification

Supply Voltage	4.5V to 5.5V
Average Operating Supply Current	8 mA typ.

4. Block Diagram



5. Pin Configuration

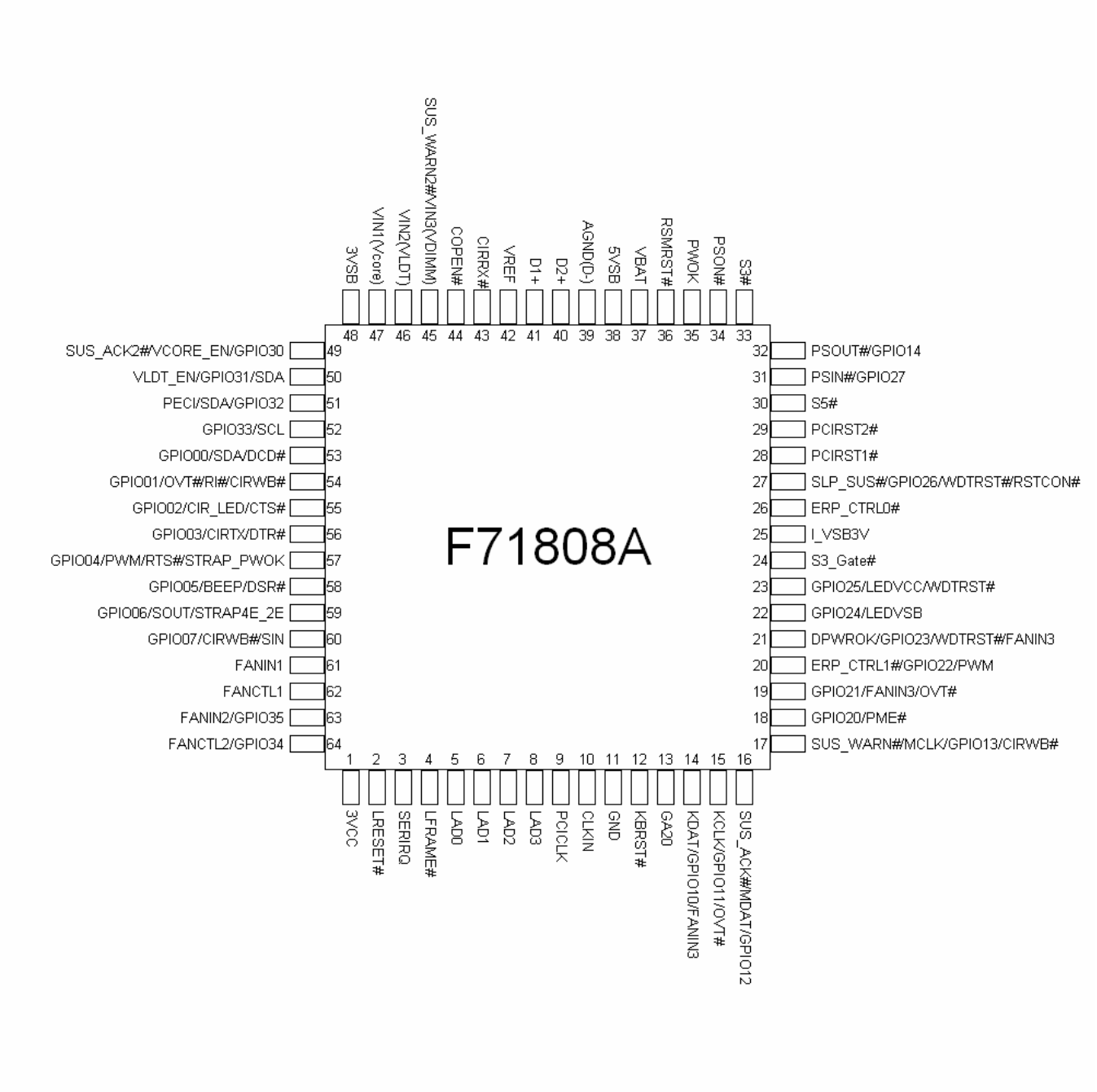


Figure1. F71808A pin configuration

6. Pin Description

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink cap ability.
I/O_{12ts5v} - TTL level bi-directional pin with schmitt trigger, 12 mA source-sink capability and 5V tolerance.
I/O_{16ts} - TTL level bi-directional pin with schmitt trigger, 16 mA source-sink capability.
I/OOD_{8ts5v} - TTL level bi-directional pin with schmitt trigger, Open-drain output with 8 mA sink capability, 5V tolerance.
I/OOD_{12ts5v} - TTL level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability and and 5V tolerance
I/OOD_{16ts5v} - TTL level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 16 mA source-sink capability and and 5V tolerance
I/OD_{12ts5v} - TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
I/OD_{16ts5v} - TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.
I_{LV}/O_{D8-S1} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability.
$O_{8-u47-5v}$ - Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
O_{12} - Output pin with 12 mA source-sink capability.
O_{12-5v} - Output pin with 12 mA source-sink capability, 5V tolerance.
O_{16-5v} - Output pin with 16 mA source-sink capability, 5V tolerance.
O_{20} - Output pin with 20 mA source-sink capability.
O_{24} - Output pin with 24 mA source-sink capability.
OOD_{12-5v} - OD or OUT selected by register with 12 mA sink capability, 5V tolerance.
OOD_{16-5v} - OD or OUT selected by register with 16 mA sink capability, 5V tolerance.
AOUT - Output pin(Analog).
OD_{12} - Open-drain output pin with 12 mA sink capability.
OD_{12-5v} - Open-drain output pin with 12 mA sink capability, 5V tolerance.
$OD_{16-u10-5v}$ - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
IN_{t5v} - TTL level input pin,5V tolerance.
IN_{ts} - TTL level input pin and schmitt trigger.
IN_{ts-lv} - TTL low level input pin (VIH → 0.9V, VIL → 0.6V.)
IN_{ts5v} - TTL level input pin with schmitt trigger, 5V tolerance.
AIN - Input pin(Analog).
AOUT - Output pin(Analog).
P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
1	3VCC	P	Power supply voltage input with 3.3V
11	GND	P	Digital GND
25	I_VSB3V	P	3.3V internal standby power regulates from 5VSB, couple this pin with capacitor (0.1u) to ground for inter capacitance compensation. Besides, this pin can be an output pin to provide little current for Battery application when system enters ERP (G3' like) state. (Detail pleaser refer application circuit)
37	VBAT	P	Battery voltage input
38	5VSB (5VA)	P	5V stand by power input. Nomally the 5V stand by power source is from ATX Power directly.

39	AGND(D-)	P	Analog GND
48	3VSB	P	Analog Stand-by power supply voltage input 3.3V

6.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
2	LRESET#	IN_{ts}	3VCC	Reset signal. It can connect to PCIRST# signal on the host.
3	SERIRQ	I/O_{12t}	3VCC	Serial IRQ input/Output. Internal pull high 47k ohms.
4	LFRAME#	IN_{ts}	3VCC	Indicates start of a new cycle or termination of a broken cycle. Internal pull high 47k ohms.
8-5	LAD[3:0]	I/O_{16ts}	3VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral. Internal pull high 47k ohms.
9	PCICLK	IN_{ts}	3VCC	33MHz PCI clock input.
10	CLKIN	IN_{ts}	3VCC	System clock input. According to the input frequency 24/48MHz.

6.3 UART Function

Pin No.	Pin Name	Type	PWR	Description
53	GPIO00	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting. GPIO00/GPIO01 can be selected to control PWM duty (220Hz) of PWM pin.
	SDA	I/OD_{12ts5v}		SMBUS Interface DATA pin.
	DCD#	IN_{ts5v}		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
54	GPIO01	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting. GPIO00/GPIO01 can be selected to control PWM duty (220Hz) of PWM pin.
	OVT#	$OD_{12\text{-}5v}$		Over temperature signal output. OVT# function selected by register setting.
	RI#	IN_{ts5v}		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	CIRWB#	IN_{ts5v}		CIR wide-band receiver input (For Learning use)
55	GPIO02	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting.
	CIR_LED	$OD_{12\text{-}5v}$		LED for CIR to indicate receiver is receiving data.
	CTS#	IN_{ts5v}		Clear To Send is the modem control input.
56	GPIO03	I/OOD_{16ts5v}	3VCC	General purpose IO. GPIO function selected by register setting.
	CIRTX	O_{20}		CIR Transmitter to transmit data.
	DTR#	$O_{16\text{-}5v}$		UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.

57	GPIO04	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting.
	PWM	$OOD_{12\text{-}5v}$ AOUT		PWM or Voltage output pin. The PWM output frequency can be selected from 220Hz to 23.5KHz or selected Voltage output from 0V to 3.3V by register setting. It can support manual fan control or backlight control application.
	RTS#	$O_{12\text{-}5v}$		UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	STRAP_PWOK	IN_{t5v}		Strapping pin for AMD and Intel PWOK. 1 Default PWOK (pin 35) for AMD 0 PWOK (pin 35) for Intel
58	GPIO05	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting. Add Mute function (Support scan code setting). Low Active.
	BEEP	OD_{12}		Beep pin.
	DSR#	IN_{ts5v}		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
59	GPIO06	I/OOD_{8ts5v}	3VCC	General purpose IO. GPIO function selected by register setting.
	SOUT	$O_{8\text{-}u47,5v}$		UART Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	STRAP4E_2E	IN_{t5v}		Power on strapping: (Default internal pull hight to 4E) 1 Configuration register:4E (Default) 0 Configuration register:2E
60	GPIO07	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting.
	CIRWB#	IN_{ts5v}		CIR wide-band receiver input (For Learning use)
	SIN	IN_{ts5v}		Serial Input. Used to receive serial data through the communication link.

6.4 Hardware Monitor

Pin No.	Pin Name	Type	PWR	Description
40	D2+	AIN	3VSB	Thermal diode/transistor temperature sensor input2.
41	D1+	AIN	3VSB	Thermal diode/transistor temperature sensor input1. This pin is for CPU use.
42	VREF	AOUT	3VSB	Voltage sensor output. Power down by VCC.
45	SUS_WARN2#	IN_{ts5v}	3VSB	This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported. Should set index 2Ch bit 7 to 1 for using this pin along with Pin 49 for DSW function.
	VIN3(VDIMM)	AIN		Voltage Input 3. Voltage Input for VDIMM DUAL STR

				(2.5V/1.8V). 0.9V power ok.
46	VIN2(VLDT)	AIN	3VSB	Voltage Input 2. Voltage Input for VLDT (1.2V). 0.9V power ok.
47	VIN1(Vcore)	AIN	3VSB	Voltage Input for Vcore. 0.6V power ok.
61	FANIN1	IN_{ts5v}	3VCC	Fan 1 for CPU Fan tachometer input.
62	FANCTL1	$OD_{12\text{-}5v}$	3VCC	Fan 1 control output for CPU Fan. This pin provides only PWM duty-cycle output.
63	FANIN2	IN_{ts5v}	3VCC	Fan 2 tachometer input.
	GPIO35	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
64	FANCTL2	$OOD_{12\text{-}5v}$ AOUT	3VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output. Pull up 4.7K to VCC to for PWM mode option.
	GPIO34	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
51	PECI	$I_{LV}/O_{D8\text{-}S1}$	3VCC	Intel PECI hardware monitor interface.
	SDA	I/OD_{12ts5v}		SMBUS Interface DATA pin.
	GPIO32	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
52	GPIO33	I/OOD_{12ts5v}	3VCC	General purpose IO. GPIO function selected by register setting.
	SCL	I/OD_{12ts5v}		SMBUS Interface CLOCK pin.

6.5 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
24	S_3_Gate	O_{12}	I_VSB3V	Switch 3VSB power to memory when in S3 state In S0# (Low level In S3# (Drive high In S5# (Default is Low level, and can be programmed to drive high
27	SLP_SUS#	$IN_{st\text{-}lv}$	I_VSB3V	For Intel CPT DSW function. Connect to PCH SLP_SUS pin.
	GPIO26	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
	WDTRST#	$OD_{12\text{-}5v}$		Watch dog timer signal output. WDTRST# function selected by register setting.
	RSTCON#	IN_{ts5v}		Connect to reset button. Internal with de-bounce circuit which is at least 50ms. Pull-high 10Kohm to VSB3V internally.
28	PCIRST1#	$OD_{12\text{-}5v}$	I_VSB3V	It is an output buffer of LRESET#. This pin supports software reset by program.
29	PCIRST2#	O_{24}	I_VSB3V	It is an output buffer of LRESET#. This pin supports software reset by program.
30	S5#	IN_{ts5v}	I_VSB3V	S5# signal input.

31	PSIN#	IN_{ts5v}	I_VSB3V	Main power switch button input.
	GPIO27	I/OOD_{12ts5v}		General purpose IO. Support High/Low/Pulse/Level selection. GPIO function selected by register setting.
32	PSOUT#	OD_{12-5v}	I_VSB3V	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO14	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
33	S3#	IN_{ts5v}	I_VSB3V	S3# Input is Main power on-off switch input.
34	PSON#	OD_{12-5v}	I_VSB3V	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
35	PWOK	I/OD_{12}	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.
36	RSMRST#	OD_{12}	VBAT	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.8V.
49	SUS_ACK2#	OOD_{16-5v}	3VSB	This pin must wait SUS_WARN2# signal for entering DSW power state. Should set index 2Ch bit 7 to 1 for using this pin along with Pin 45 for DSW function.
	VCORE_EN	OD_{12-5v}		Active high. The function of this pin is to enable the PWM for CPU Vcore. The external pull high resistor is required.
	GPIO30	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting. It can control the system volume from LPC interface (Support scan code setting). Low Active.
50	VLDT_EN	OD_{12-5v}	3VSB	Active high. The function of this pin is to enable the VLDT voltage. The external pull high resistor is required.
	GPIO31	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting. It can control the system volume from LPC interface (Support scan code setting). Low Active.
	SDA	I/OD_{12ts5v}		SMBUS Interface DATA pin.

6.6 KBC Function

Pin No.	Pin Name	Type	PWR	Description
12	KBRST#	$OD_{16-u10,5v}$	3VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
13	GA20	$OD_{16-u10,5v}$	3VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
14	KDAT	I/OD_{16ts5v}	I_VSB3V	Keyboard Data.
	GPIO10	I/OOD_{16ts5v}		General purpose IO. GPIO function selected by register setting.
	FANIN3	IN_{ts5v}		Fan 3 tachometer input. Selected by register setting.
15	KCLK	I/OD_{16ts5v}	I_VSB3V	Keyboard Clock.
	GPIO11	I/OOD_{16ts5v}		General purpose IO. GPIO function selected by register setting.
	OVT#	OD_{12-5v}		Over temperature signal output. OVT# function selected by register setting.
16	SUS_ACK#	OOD_{16-5v}		This pin must wait SUSWARN# signal for entering

			I_VSB3V	DSW power state.
	MDAT	I/OD_{16ts5v}		PS2 Mouse Data. Use with Pin 17 for DSW
	GPIO12	I/OOD_{16ts5v}		General purpose IO. GPIO function selected by register setting.
17	SUS_WARN#	IN_{ts5v}	I_VSB3V	This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported. Use with Pin 16 for DSW.
	MCLK	I/OD_{16ts5v}		PS2 Mouse Clock.
	GPIO13	I/OOD_{16ts5v}		General purpose IO. GPIO function selected by register setting.
	CIRWB#	IN_{ts5v}		CIR wide-band receiver input. (For Learning use)

6.7 Others

Pin No.	Pin Name	Type	PWR	Description
18	GPIO20	I/OOD_{12ts5v}	I_VSB3V	General purpose IO. GPIO function selected by register setting.
	PME#	$OD_{12\text{-}5v}$		Generated PME event. It supports the PCI PME# nterface. This signal allows the peripheral to request the system to wake up from the S3 state.
19	GPIO21	I/OOD_{12ts5v}	I_VSB3V	General purpose IO. GPIO function selected by register setting.
	FANIN3	IN_{ts5v}		Fan 3 tachometer input. Selected by register setting.
	OVT#	$OD_{12\text{-}5v}$		Over temperature signal output. OVT# function selected by register setting.
20	ERP_CTRL1#	$OD_{12\text{-}5v}$	I_VSB3V	Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
	PWM	$OOD_{12\text{-}5v}$ AOUT		PWM or Voltage output pin. The PWM output frequency can be selected from 220Hz to 23.5KHz or selected Voltage output from 0V to 3.3V by register setting. It can support manual fan control or backlight control application.
	GPIO22	I/OOD_{12ts5v}		General purpose IO. Support High/Low/Pulse/Level selection.
21	DPWROK	$OD_{12\text{-}5v}$	I_VSB3V	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.
	GPIO23	$OD_{12\text{-}5v}$		General purpose pin. Support High/Low/Pulse/Level selection.
	WDTRST#	$OD_{12\text{-}5v}$		Watch dog timer signal output. WDTRST# function selected by register setting.
	FANIN3	IN_{ts5v}		Fan 3 tachometer input. Selected by register setting.
22	GPIO24	I/OOD_{12ts5v}	I_VSB3V	General purpose pin. Support High/Low/Pulse/Level selection.

	LEDVSB	$OD_{12\text{-}5v}$		Power LED for VSB. Blink frequency selection. LEDVSB function selected by register setting.
23	GPIO25	I/OOD_{12ts5v}	I_VSB3V	General purpose pin. Support High/Low/Pulse/Level selection.
	LEDVCC	$OD_{12\text{-}5v}$		Power LED for VCC. Blink frequency selection. LEDVCC function selected by register setting.
	WDTRST#	$OD_{12\text{-}5v}$		Watch dog timer signal output. WDTRST# function selected by register setting.
26	ERP_CTRL0#	OD_{12}	I_VSB3V	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
43	CIRRX#	IN_{ts5v}	I_VSB3V	CIR long-range receiver input
44	COPEN#	IN_{ts5v}	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop back by the battery for case open state preservation during power loss.

7. Function Description

7.1 Power on Strapping Option

The F71808A provides one pin for power on hardware strapping to select the function. There is a form to describe how to set the function you want.

Table1. Power on trap configuration

Pin No.	Symbol	Value	Description
57	STRAP_PWOK	1	PWOK (pin 35) for AMD (Default)
		0	PWOK (pin 35) for Intel
59	STRAP4E_2E	1	Configuration Register I/O port is 4E. (Default)
		0	Configuration Register I/O port is 2E.

7.2 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60H. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60H or 64H. Writing to address 60H sets a flag to indicate a data write; writing to address 64H sets a flag to indicate a command write. Data written to I/O address 60H is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

Status Register

The status register is an 8-bit read-only register at I/O address 64H, that holds information about the status of the keyboard controller and interface. It may be read at any time.

Bit	Bit Function	Description
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

Commands

<table>
<tr><th>Command</th><th>Fucntion</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
</table>

A9h	Auxiliary Interface Test 8'h00: indicate Auxiliary interface is ok. 8'h01: indicate Auxiliary clock is low. 8'h02: indicate Auxiliary clock is high 8'h03: indicate Auxiliary data is low 8'h04: indicate Auxiliary data is high
AAh	Self-test Returns 055h if self test succeeds
ABh	keyboard Interface Test 8'h00: indicate keyboard interface is ok. 8'h01: indicate keyboard clock is low. 8'h02: indicate keyboard clock is high 8'h03: indicate keyboard data is low 8'h04: indicate keyboard data is high
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
C0h	Read Input Port(P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into STATUS register
C2h	Continuously puts the upper four bits of Port1 into STATUS register
CAh	Read the data written by CBh command.
CBh	Written a scratch data. This byte could be read by CAh command.
D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Pulse only RC(the reset line) low for 6μS if Command byte is even

KBC Command Description

PS2 wakeup function

The KBC supports keyboard and mouse wakeup function, keyboard wakeup function has 4 kinds of conditions, when key is pressed combinational key (1) CTRL +ESC (2) CTRL+F1 (3) CTRL+ User Defined Code (4) ANY KEY (5) windows 98 wakeup up key (6) windows 98 power key (7) CTRL + ALT + User Defined Code (8) User Defined Code, KBC will assert PME signal. Mouse wakeup function has 2 kinds of conditions, when mouse (1) BUTTON CLICK or (2) BUTTON CLICK AND MOVEMENT, KBC will assert PME signal. Those wakeup conditions are controlled by configuration register.

7.3 Hardware Monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex: 1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC/VSB/VBAT is an exception for it is main power of the F71808A. Therefore 3VCC/VSB/VBAT can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F71808A and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are three voltage inputs in the F71808A and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

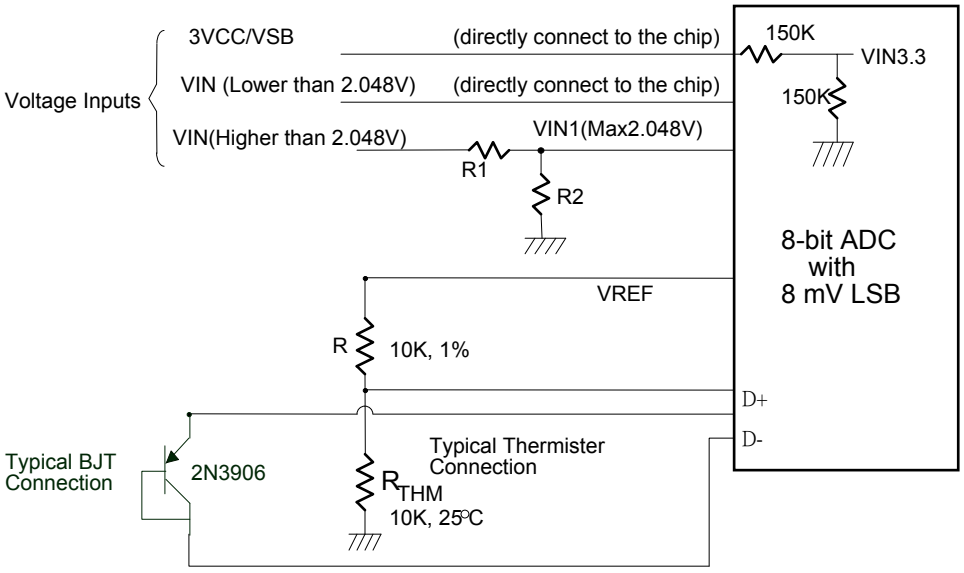


Figure2. Hardware monitor configuration

The F71808A monitors two remote temperature sensors.These sensors can be measured from -40°C to 127°C. More detail, please refer register description.

Table2. Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

Table Range:

Table3. Display range is from -40°C to 127°C in 2's complement format.

Temperature	Digital Output
-40°C	1101 1000
-1°C	1111 1111
1°C	0000 0001
90°C	0101 1010
127°C	0111 1111
Open	1000 0000

Monitor Temperature from "Thermistor"

The F71808A can connect two thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 6-1, the thermistor is connected by a serial resistor with 10K ohm, and then connected to VREF. The temperature measurement range is 0~127°C.

Monitor Temperature from "Thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71808A is capable to these situations. The build-in reference table is for PNP 2N3906 transistor. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Monitor Temperature from "SMbus device"

F71808A provides SMbus "BLOCK READ" compatible PCH EC SMbus protocol and provides "SEND/RECEIVE BYTE" protocol to read CPU and chipset thermal temperature information.

Monitor Temperature from "PECI"

F71808A support Intel PECI 3.0 interface to read temperature from PECI 3.0 device.

Temperature HM_IRQ Signal (HM_IRQ# and PME#)

Over temperature event will trigger HM_IRQ# that shown as figure. When monitored temperature exceeds the high temperature threshold value, HM_IRQ# will be asserted until the temperature goes below the hysteresis temperature.

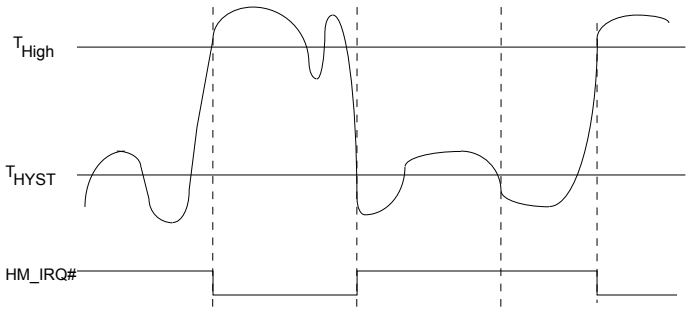
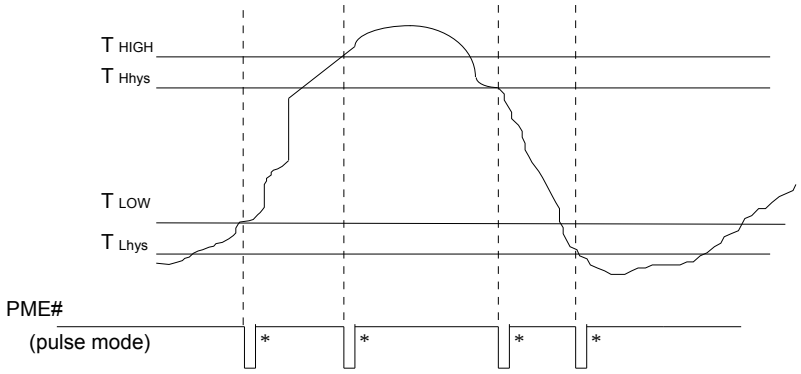


Figure 3

PME# interrupt for temperature is shown as figure. Temperature exceeding high limit (low limit) or going below high hysteresis (low hysteresis) will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Figure 4 Hysteresis mode illustration

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

Fan speed control

The F71808A provides 2 fan speed control methods:

1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

Only FANCTL2/FANCTL3 support DAC (Voltage) Fan control. The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

And the suggested application circuit for linear fan control would be:

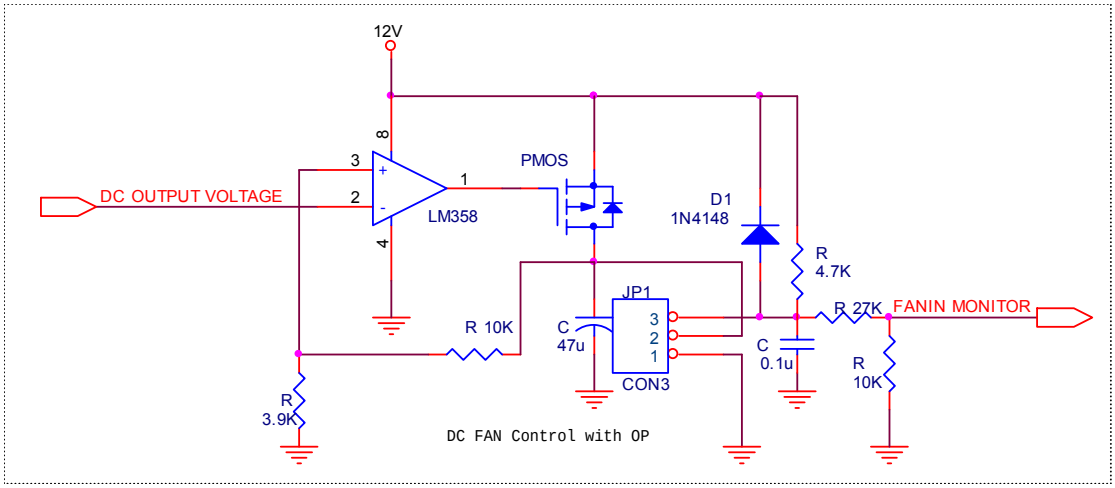


Figure 5 DAC fan control application circuit

PWM duty Fan Control

The duty cycle of PWM can be programmed by an 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle}(\%) = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

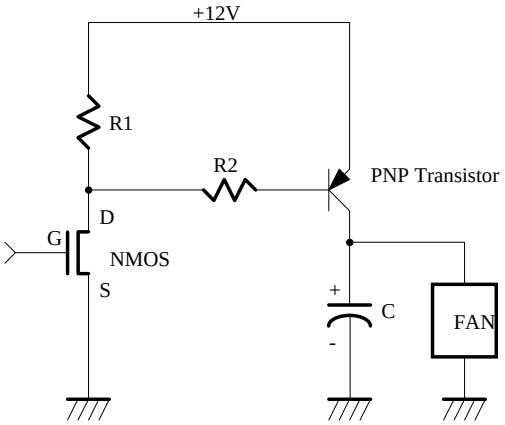


Figure 6 +12/5V PWM fan control application circuit

Fan speed control mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode 3. Linear auto mode. More detail, please refer the description of registers.

Each fan can be controlled by up to 7 kinds of temperature input. (1)D1+ temperature (2)D2+ temperature (3) PECI temperature (4) 4 suits SMBus master temperature. Please refer below structure diagram.

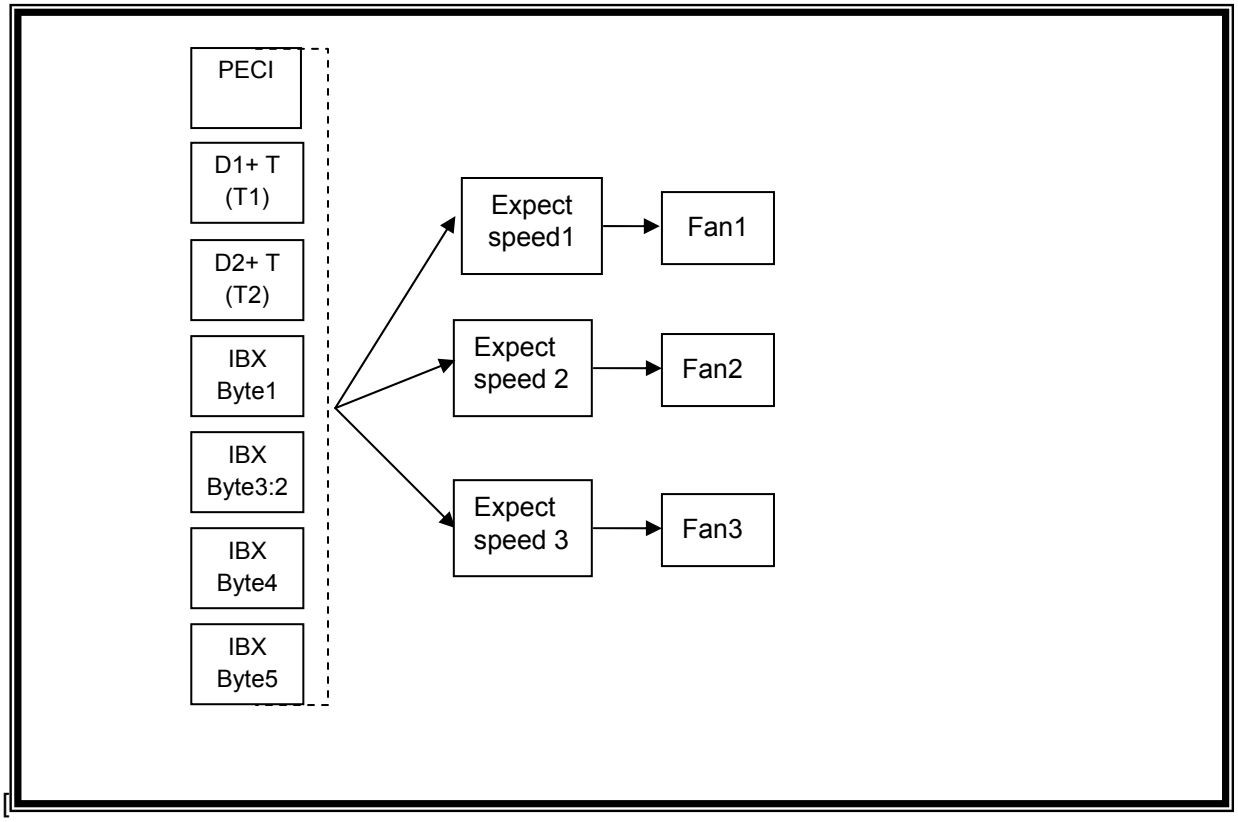


Figure 7 Relative temperature fan control

Manual mode

For manual mode, it generally acts as software fan speed control.

Auto mode

In auto mode, the F71808A provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F71808A can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE. And the hysteresis setting (0 ~ 15°C) could also be found in register 0x98.

The Manual Mode and Auto Mode could be selected by register 0x96h.

There are two kinds of auto mode: stage auto mode and linear auto mode. The “FAN1_

INTERPOLATION_EN” in register 0xAFh is used for linear auto mode enable. The following examples explain the differences for stage auto mode and linear auto mode.

Stage auto mode

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting: PWM Duty and RPM %.

A. Stage auto mode (PWM Duty)

Set the temperature limits as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

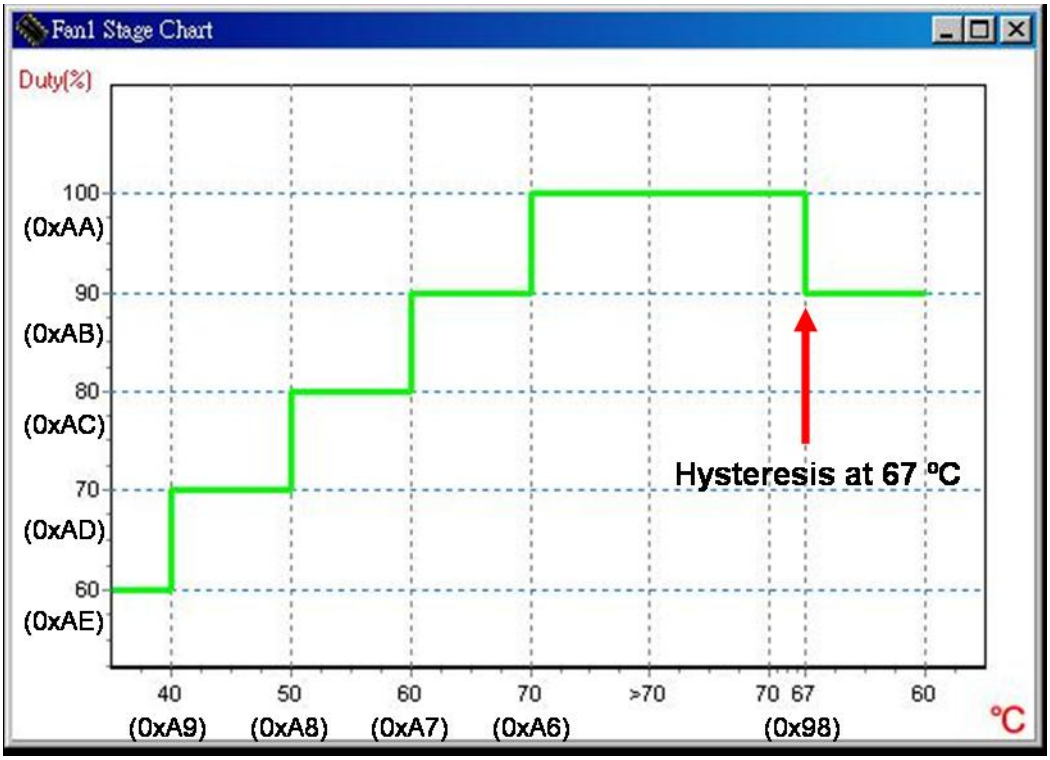


Figure 8 Stage mode fan control illustration-2

a. Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.
b. Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.
d. If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would reduce to 90% PWM duty.

B. Stage auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 5,400 rpm, 4,800 rpm, 4,200 rpm, and 3,600 rpm (assume the Max Fan Speed is 6,000 rpm).

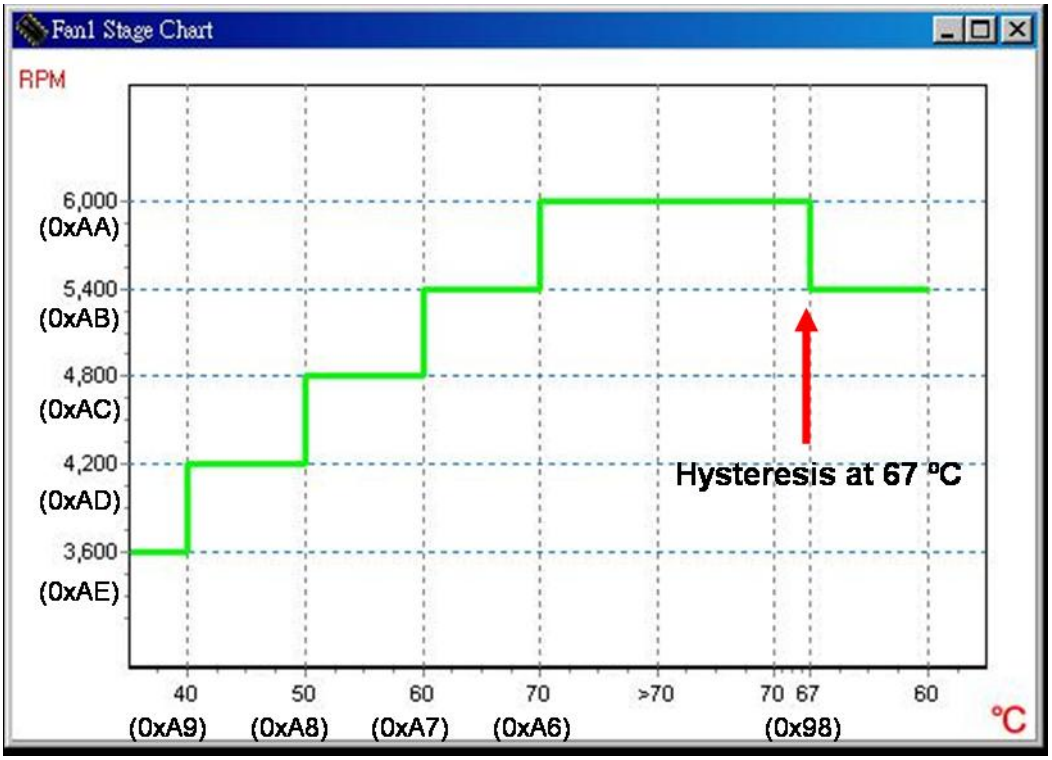


Figure 9 Stage mode fan control illustration-3

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 rpm (60% of full speed).
b. Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 rpm to 5,400 rpm and increasing with the temperature level.
c. For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 rpm.
d. If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 rpm.

Linear auto mode

F71808A also supports linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

A. Linear auto mode (PWM Duty)

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

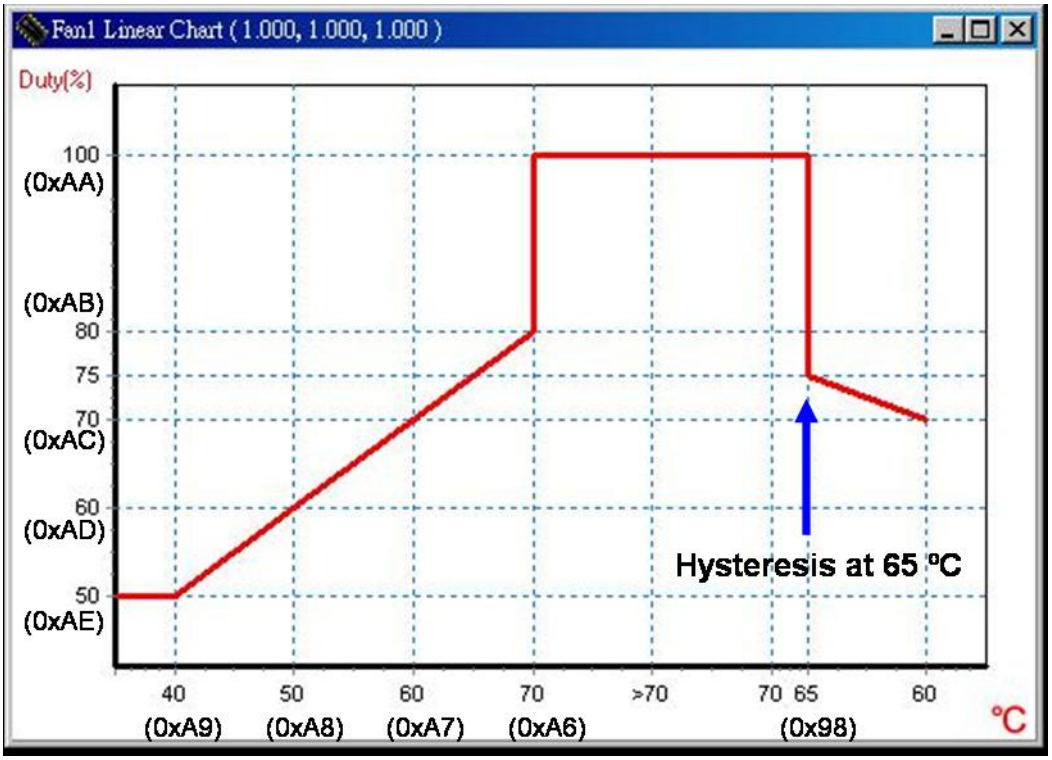


Figure 10 Linear mode fan control illustration-1

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty
b. Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the tempreature variation. The temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).
d. If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

B. Linear auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 4,800 rpm, 4,200 rpm, 3,600 rpm and 3,000 rpm (assume the Max Fan Speed is 6,000 rpm).

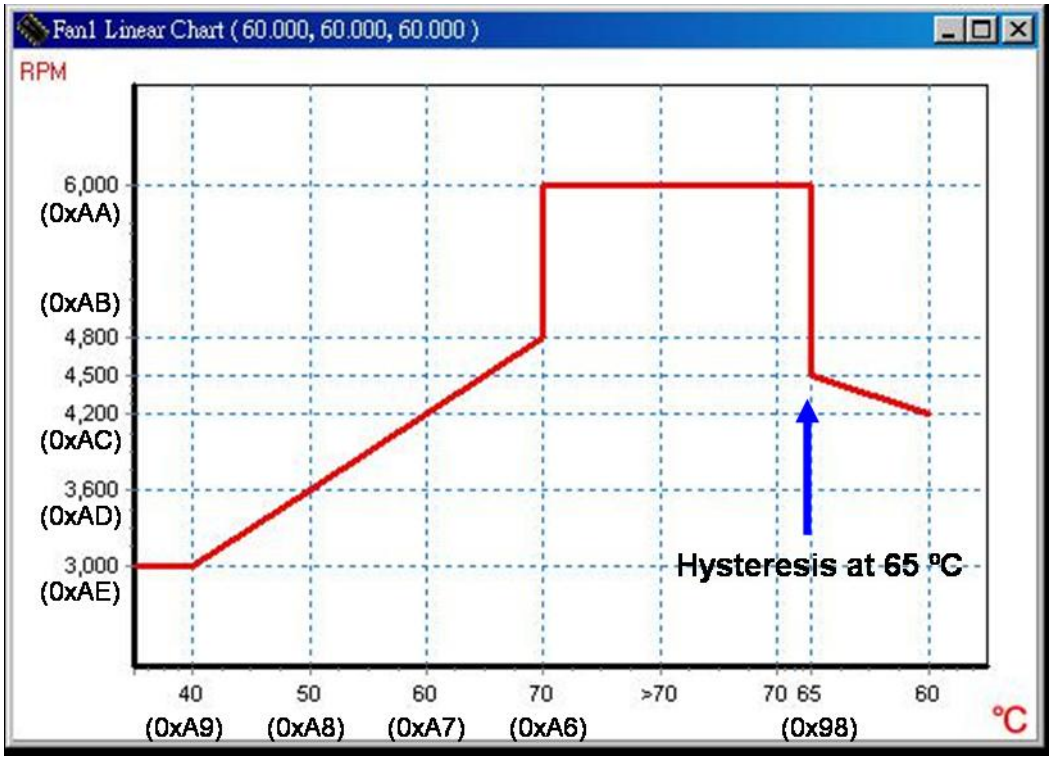
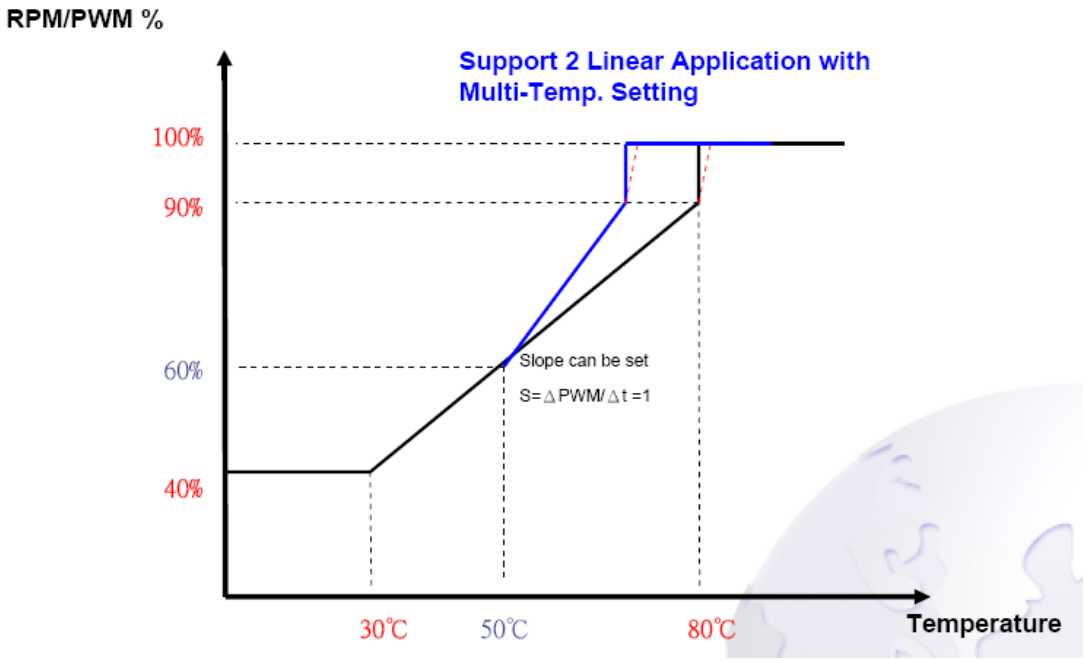


Figure 11 Linear mode fan control illustration-2

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 rpm (50% of full speed).
b. Once the temperature is over 40°C,50°C and 60°C, the fan speed will vary from 3,000 to 4,800 rpm almost linearly with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 rpm.
d. If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed wull reduce from full speed and decrease linearly with the temperature.

Fan Speed Control with Multi-temperature.

F71808A supports Multi-temperature for one fan control. This function works with linear auto mode can extend two linear slopes for one Fan control. As the graph below, this machine can support more silence fan control in low temperature environment and faster fan speed in high temperature segment. More detail setting please refers to the registers.

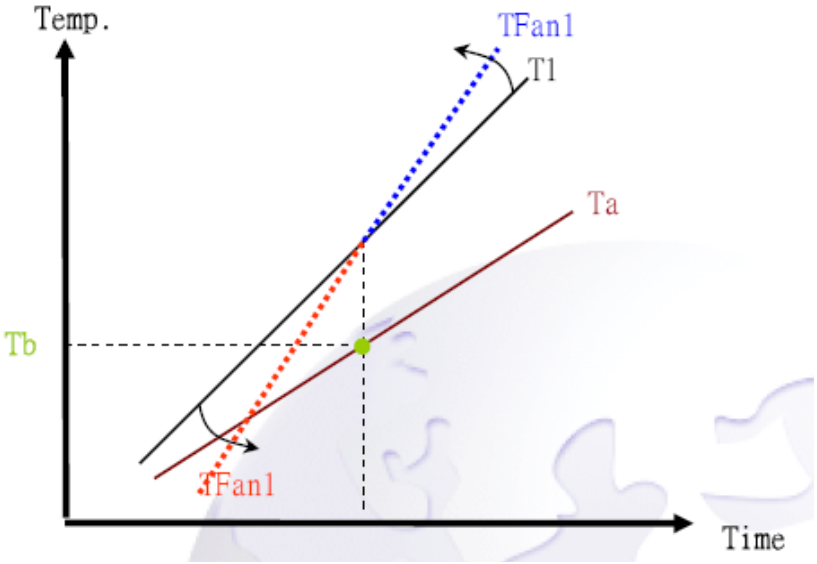


In the figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.

TFan1= T1 + (Ta-Tb)*Ctup

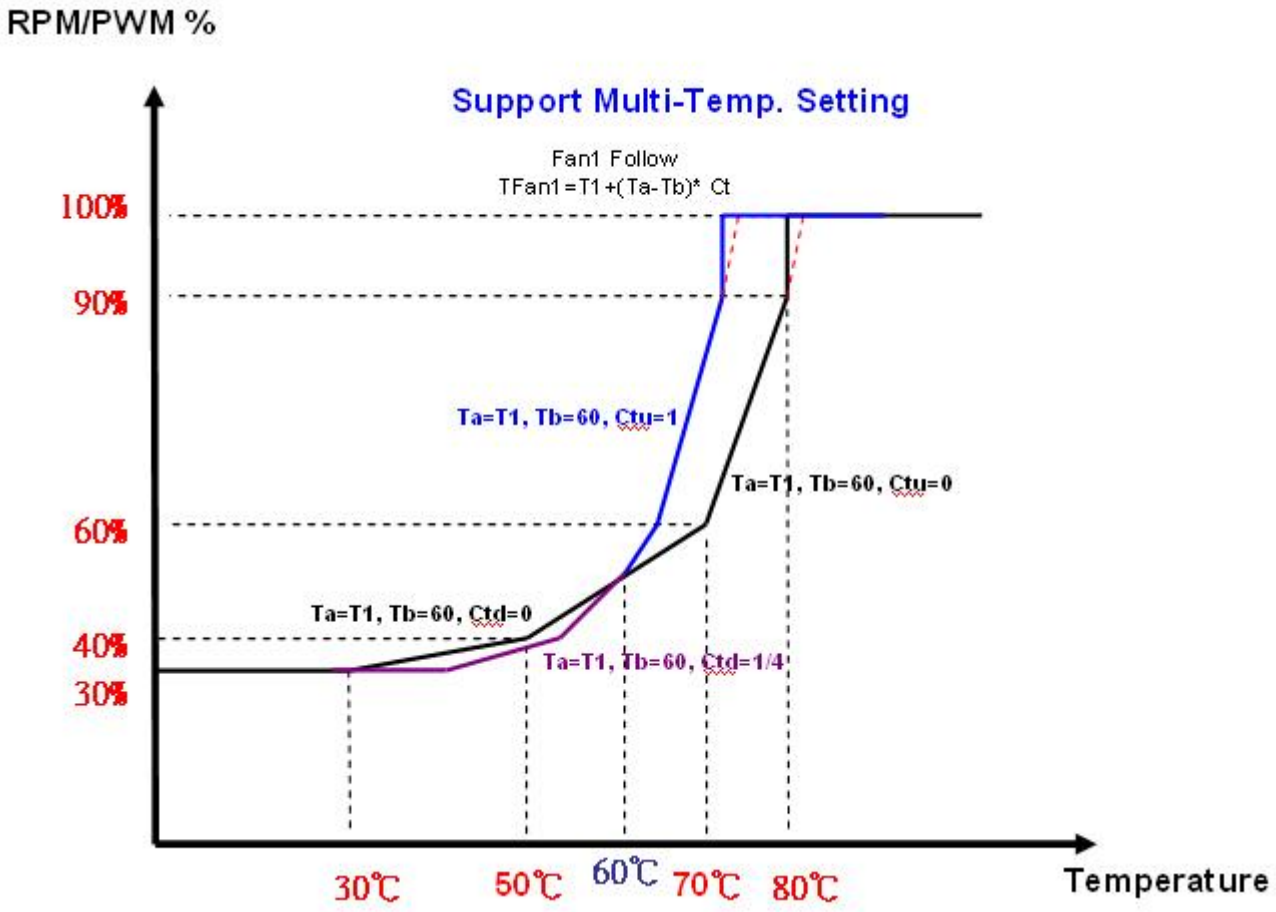
TFan1= T1 + (Ta-Tb)*Ctdn

1. **Ctup**, **Ctdn** Can be Programmed to **1, ½, ¼, 0**
2. **Ta** Can be Selected to the Same Temp. Source (Ex:T1)



In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

EX: Ta = T1, Tb = 60, Ctu = 1, Ctd = 1/4



PWMOUT Duty-cycle operating process

In both “Manual RPM” and “Temperature RPM” modes, the F71808A adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.

(2). When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.

(3). If both (1) and (2) are not true,

(4). When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, the F71808A will keep duty-cycle at 00h for 1.6 seconds. After that, the F71808A starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F71808A will ignore it.

Figure 12

FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time. (Figure 13)

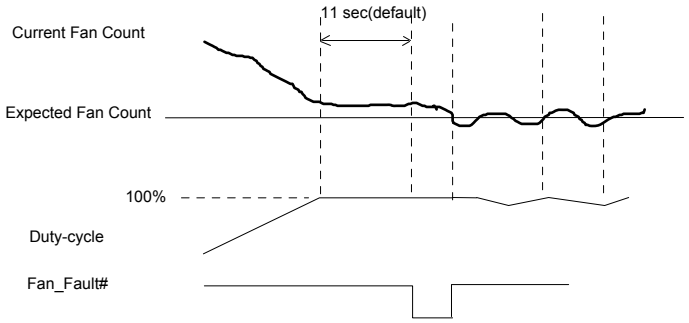


Figure 13 FAN_FAULT# event

(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count still in 0xFFF.

7.4 ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.

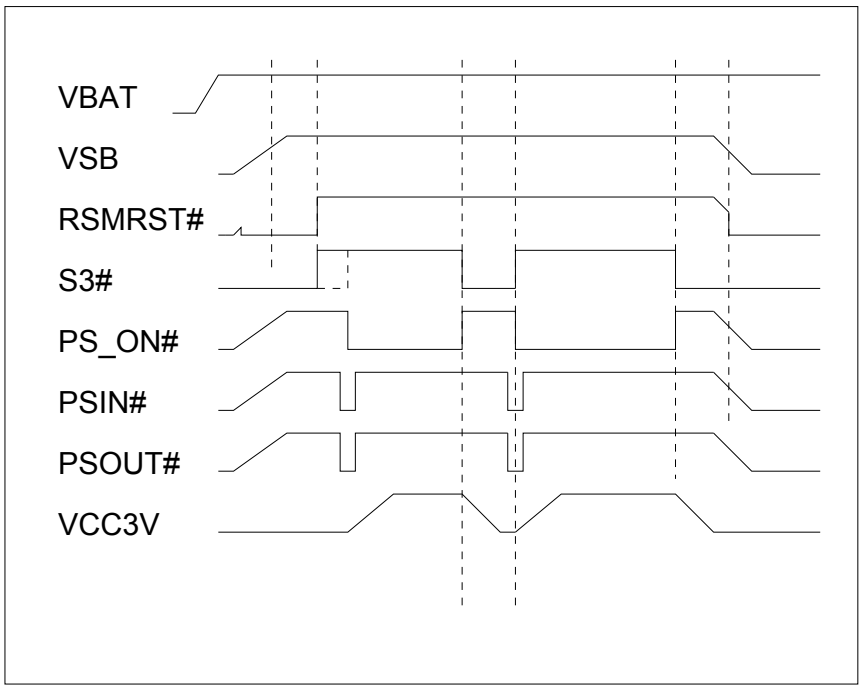


Figure 14 Default timing: Always off

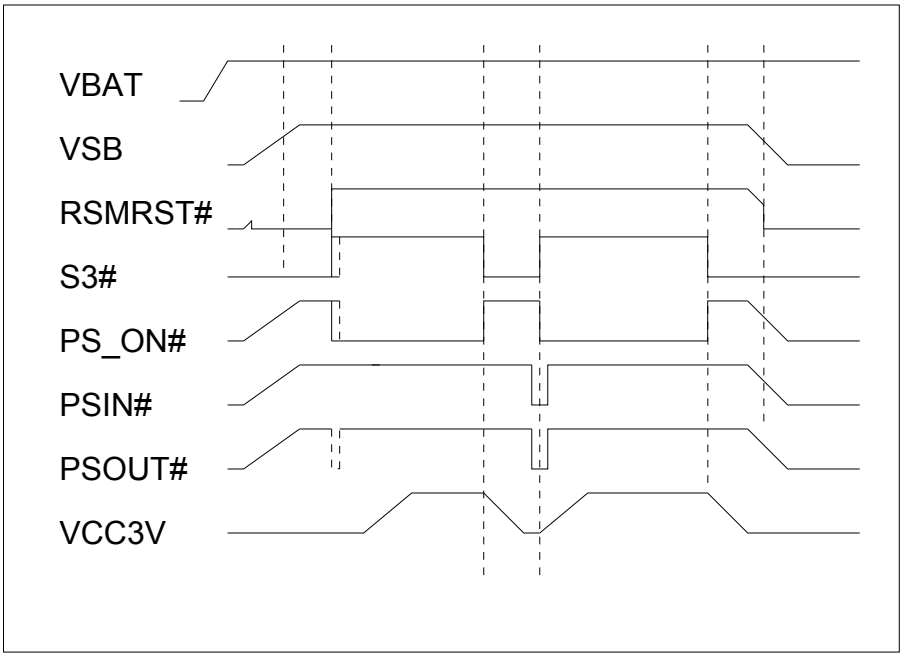


Figure 15 Optional timing: Always on

The F71808A offers 2 timing pins which are designed for AMD platform power sequence control including VCORE and VLDT (default) or other timing application purposes. All the timings on/off are relative to S3#/S5# and can be programmed by the register 0x0AF7. As shown in the below figure, the default timings of VCORE and VLDT are displayed in blue lines. VDDOK_D400 is the PWROK delay timing from VDD3VOK. The default setting is that delay 400ms, there are 100ms, 200ms, and 300ms for option. It can be set in the register 0x0AF5.

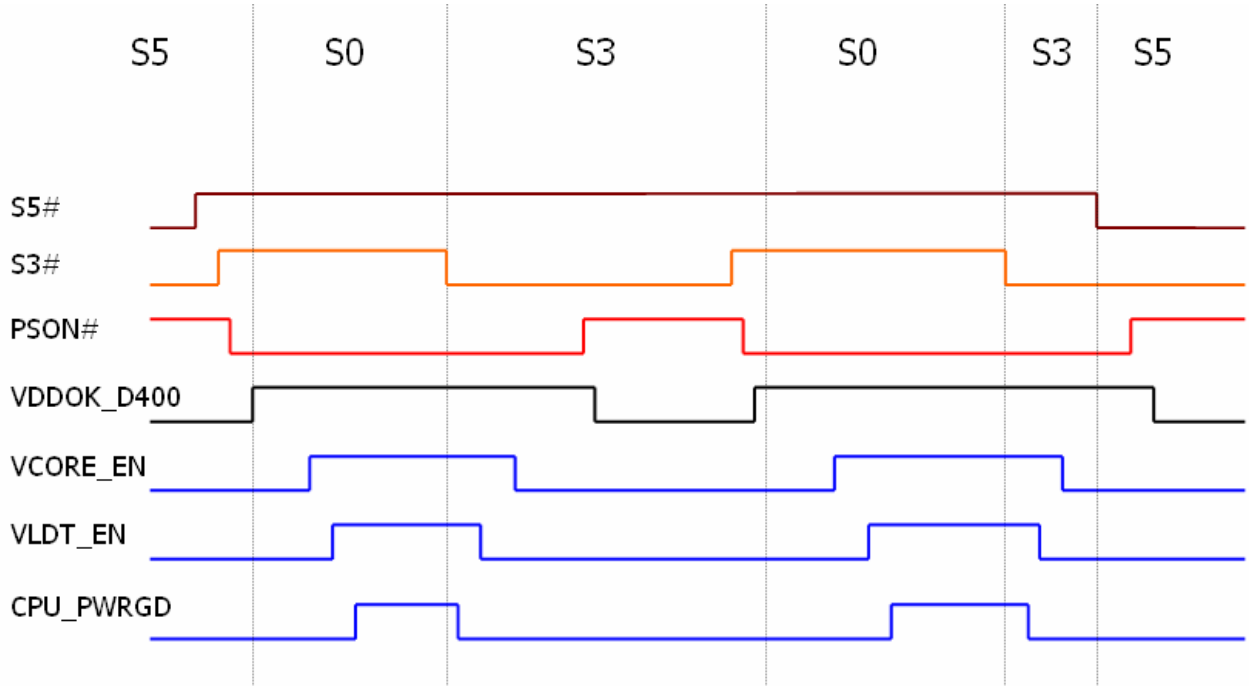


Figure 16 AMD power sequence

S3_Gate Timing

The S3_Gate is used to switch the power source of the 5VDUAL which is combined by the 5VCC and 5VSB rails according to the ACPI state to control the power rail of the DIMM especially. The timing charts of the every ACPI state are mentioned in the following figures.

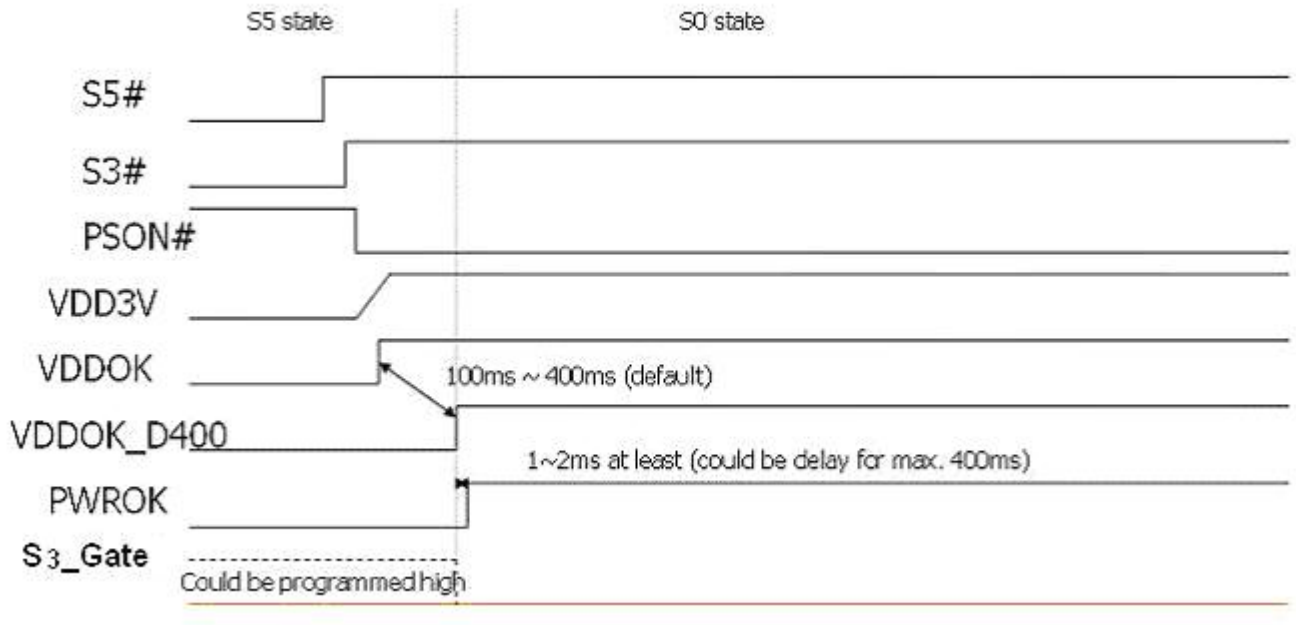


Figure 17 S3_Gate Timing: S5 → S0

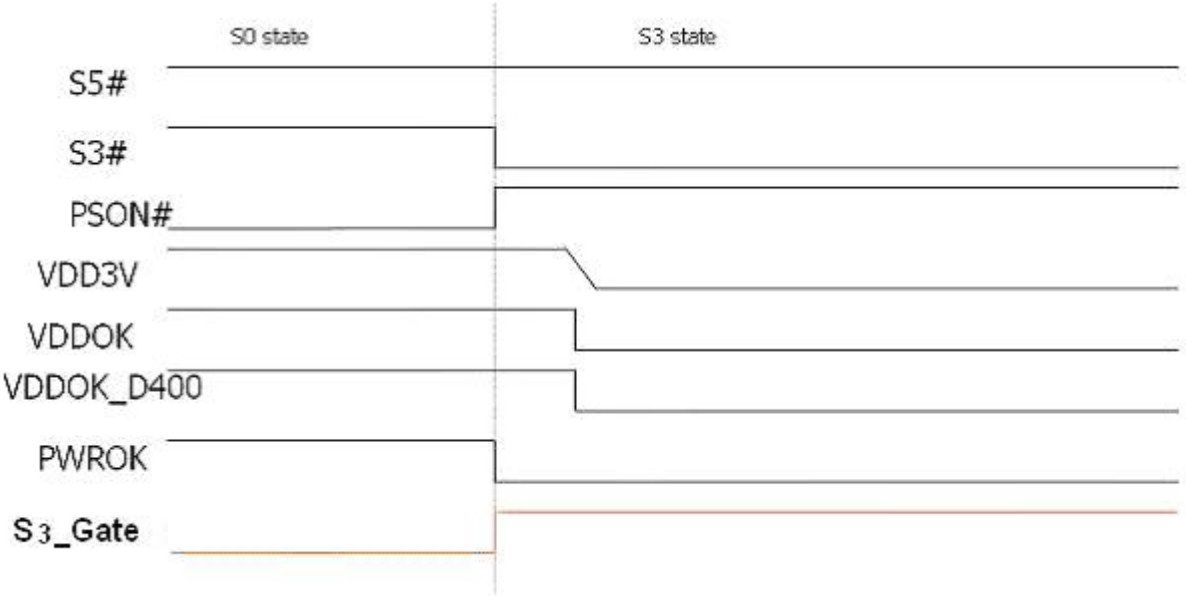


Figure 18 S3_Gate Timing: S0 → S3

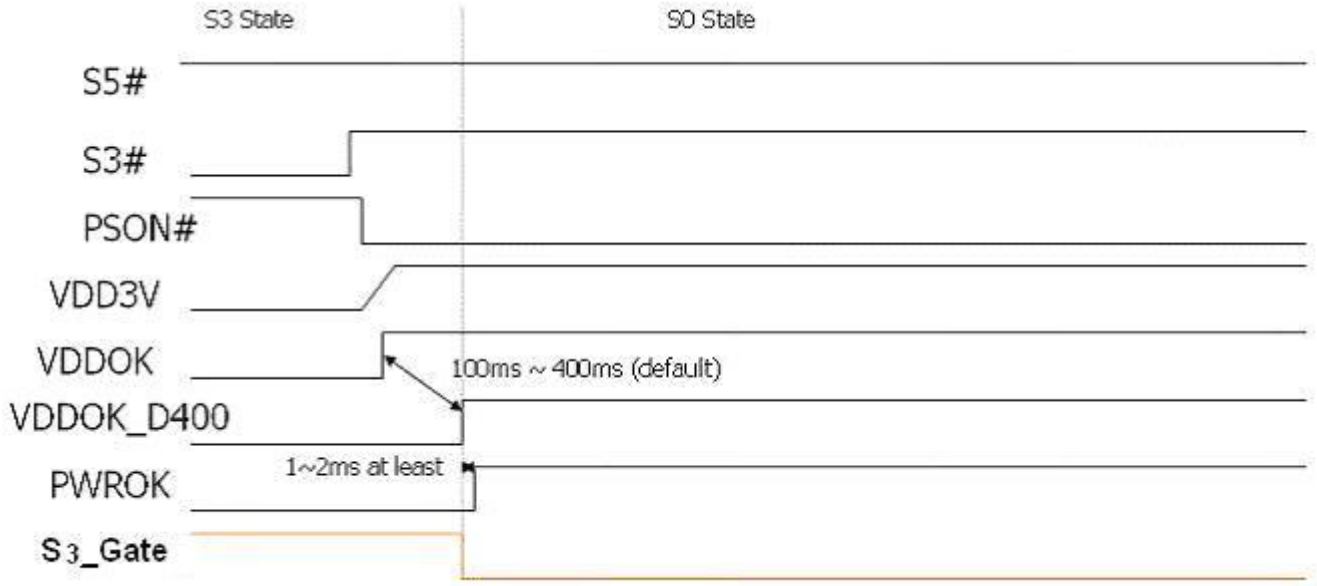


Figure 19 S3_Gate Timing: S3 → S0

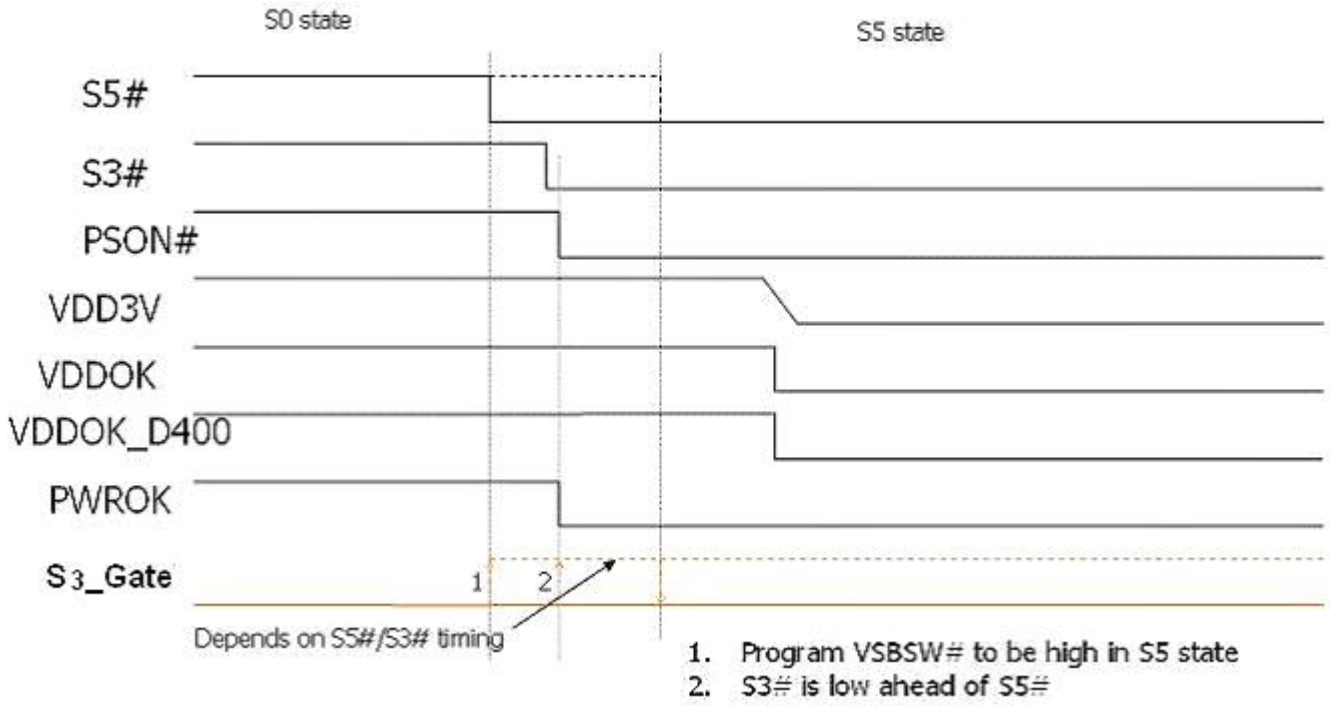
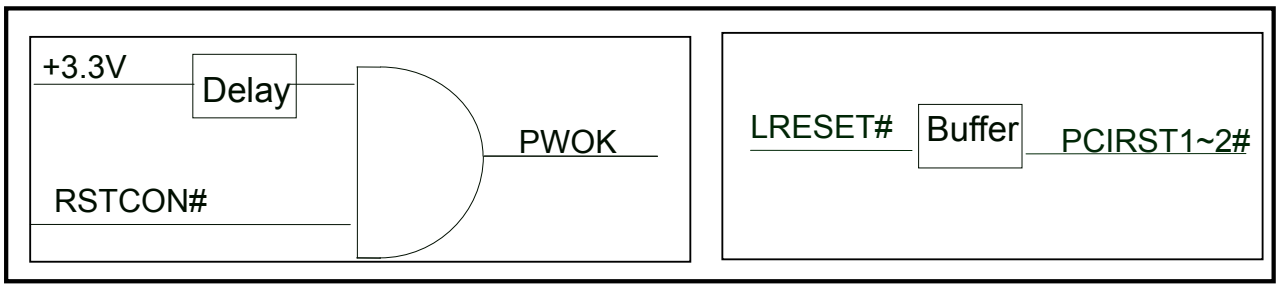


Figure 20 S3_Gate Timing: S0 → S5

PCI Reset and PWOK Signals

The F71808A supports 2 output buffers for 2 reset signals.



So far as the PWOK issue is as the figure above. PWOK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register (100ms ~ 400ms). An additional delay could be added to PWOK (0ms, 100ms, 200ms and 400ms). Default is 0ms. RSTCON# could be programmed to be asserted via PWOK.

7.5 AMD TSI and INTEL PECI 3.0 Function

The F71808A provides Intel PECI/AMD TSI interfaces for new generational CPU temperature sensing. In AMD TSI interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail, please refer the register description.

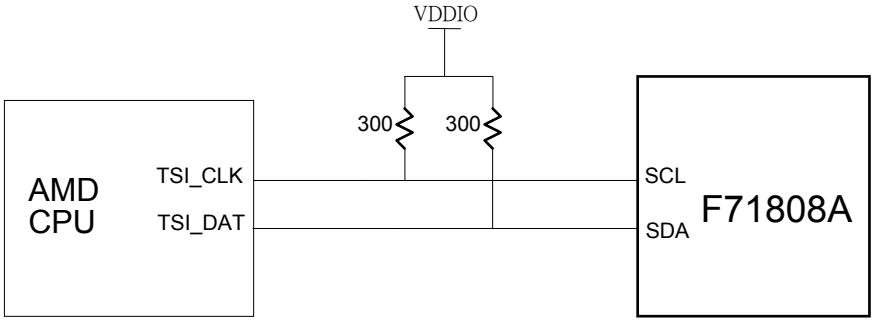


Figure 21 AMD TSI typical application

In Intel PECI interface, the F71808A can connect to CPU directly. The F71808A can read the temperature data from CPU, than the fan control machine of F71808A can implement the Fan to cool down CPU temperature. The application circuit is as below. More detail please refer to the register descriptions.

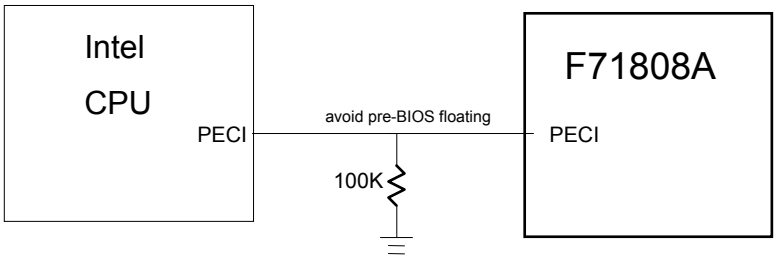


Figure 22 INTEL PECI typical application

F71808A Support	PECI 3.0 Command Name	PECI 1.0 Command Name	Status
V	Ping( )	Ping( )	
V	GetTemp( )	GetTemp( )	
V	GetDIB( )		
V	RdIAMSR( )		
-	WrIAMSR( )		
-	RdPCIConfigLocal( )		Not Available in Mobile/DT
-	WrPCIConfigLocal( )		Not Available in Mobile/DT
-	RdPCIConfig( )		Not Available in Mobile/DT
-	WrPCIConfig( )		Not Available in Mobile/DT
V	RdPkgConfig( )		
V	WrPkgConfig( )		

7.6 Power Saving Controller

The two pins, ERP_CTRL0# and ERP_CTRL1#, which control the standby power rail on/off to fulfil the purpose which decreases the power consumption when the system in the sleep state or the soft-off state. These two pins connected to the external PMOSs and the defaults are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, the two pins can be programmable to set which power rail is turned on. The programmable register is powered by battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3-like state), the F71808A consumes 5VSB power rail only to realize a low power consumption system.

7.7 Scan Code Function

F71808A has 3 GPIO pins (GPIO05, 30, 31) support scan code. These pins can not only be set to volume up/down and mute but also any function keys on keyboard. Because the protocol for these 3 pins is scan code, so we don't need a driver to connect this function to OS. If the button for the GPIO has been pressed continuesly over nearly 1 second, the GPIO will repeatedly sending this function in an interval of 50 ms.

7.8 CIR Function

The F71808A is compatible with Microsoft Windows Vista and Windows 7 IR Receiver or Transceiver Emulation Device which supports RC6 & QP protocol. It Supports 1 IR transceiver functions for blaster application and 1 IR receiver with long range frequency and another with wide band application. In power function, The F71808A supports Vista and Windows 7 wakeup programming function when the PC is in the S3 state. The F71808A decode IR protocol via the same Vista and Windows 7 wakeup programming key. The F71808A is asserted PME or PSOUT to wakeup PC system. Where wake up programming function is reference from Microsoft Vista and windows 7 remote controller specification.

The F71808A supports 1 IR transceiver function for blaster application and two IR receivers for long range frequency and wideband application. The wide-band receiver is necessary to support IR learning, IR-blasting and set-top box control.

The long-range receiver is a receiver which has the following characteristics:

1. Works at a distance of 10 meters.
2. Demodulates the signal inside the receiver part
3. Has a BPF which works with carriers from 32-60 kHz.

The wide-band receiver is a receiver part which has the following characters:

1. Works at a distance of approximately 5 centimeters.
2. Does not demodulate the signal inside the receiver part
3. Works with carriers from 32-60 kHz. (Probably doesn't have a BPF, but still has the same (or wider) range.

About IR information, reference Microsoft Windows Vista / 7 IR receiver or transceiver emulation device spec.

7.9 Intel Cougar Point Timing (CPT)

The F71808A supports Intel Cougar Point Chipset timing for Sandy Bridge. There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWROK.

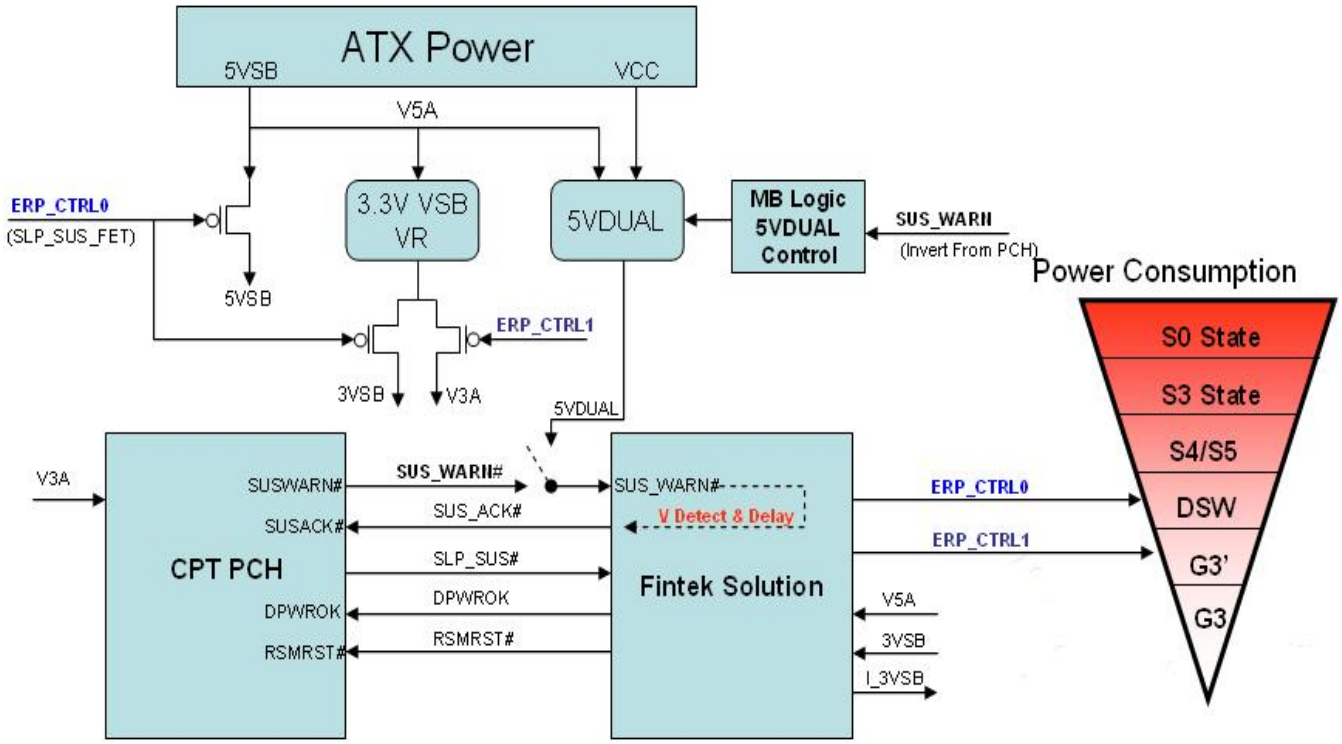
For entering Intel Deep Sleep Well (DSW) state, the PCH will assert SUS_WARN# and turn off 5VDUAL. After the level of 5VDUAL is lower than 1.05V, F71808A will assert SUS_ACK# to inform PCH it is ready for entering DSW. Finally, PCH will ramp down the internal VccSUS and assert SLP_SUS# to F71808A. F71808A will turn off the 5VSB and 3VSB by ERP_CTRL0# and enter the DSW state.

To exit DSW state, PCH will de-assert SLP_SUS#, turn on the SUS rail FETs and ramp up internal 1.05V VccSUS. After the SUS rails voltages are up, RSMRST# will be desserted and the PCH will release SUS_WARN# so that the 5VDUAL will ramp up.

Because the DSW function is controlled by F71808A instead of controlled by PCH directly, there will be more wakeup events such as LAN, KB/Mouse, SIO RI# wake up rather than the 3 wakeup events (RTC, Power Button and GPIO27) for Intel DSW.

In order to achieve lower power consumption, F71808A provides the ERP_CTRL1# to turn off the V3A so that the system can enter the Fintek G3' state.

The block diagram below shows how the connection and control method for F71808A and PCH.



8. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	1	0	0	0	0
21	Chip ID Register	0	0	0	0	0	0	0	1
23	Vendor ID Register	0	0	0	1	1	0	0	1
24	Vendor ID Register	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	-	-	-	-	0	-
26	Clock Select Register	0	-	-	-	-	0	-	-
27	Configuration Port Select Register	0	0	0	0	0	0	0	1
28	Multi-function Select Register 0	0	0	0	0	0	0	0	0
29	Multi-function Select Register 1	1	1	0	0	0	0	0	0
2A	Multi-function Select Register 2	0	0	1	0	0	0	0	0
2B	Multi-function Select Register 3	0	1	1	1	1	1	1	1
2C	Multi-function Select Register 4	0	0	0	0	1	1	0	0

2D	Wakeup Control Register	0	0	1	0	1	0	0	0

Device Configuration Registers

"-" Reserved or Tri-State

UART Device Configuration Registers (LDN 0x01)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	RS485 Enable Register	-	-	0	0	-	-	-	-
Hardware Monitor Device Configuration Registers (LDN 0x04)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0
KBC Device Configuration Registers (LDN 0x05)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
FE	Swap Register	0	-	-	0	0	0	0	1
FF	User Wakeup Code Register	0	0	1	0	1	0	0	1
GPIO Device Configuration Registers (LDN 0x06)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
70	GPIRQ Channel Select Register	-	-	-	-	0	0	0	0
C0	GPIO3 Output Enable Register	-	-	0	0	0	0	0	0
C1	GPIO3 Output Data Register	-	-	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	-	-	0	0	0	0	0	0
C4	Event SMI Enable Register	-	-	-	0	0	0	0	0

C5	Event Detect Select Register	-	-	-	0	0	0	0	0
C6	Event SMI Status Register	-	-	-	0	0	0	0	0
CB	Event 2 Make Code Register	0	0	0	0	0	0	0	0
CC	Event 1 Make Code Register	0	0	0	0	0	0	0	0
CD	Event 0 Make Code Register	0	0	0	0	0	0	0	0
CE	Event Prefix Code Register	1	1	1	0	0	0	0	0
CF	Event KBC Control Register	0	1	-	-	-	-	-	-
D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	0	0	0	0	0	0	0	0
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
D4	GPIO2 PME Enable Register	-	-	0	0	0	0	-	-
D5	GPIO2 Detect Edge Select Register	-	-	0	0	0	0	-	-
D6	GPIO2 PME Status Register	-	-	0	0	0	0	-	-
D7	GPIO2 Outpute Mode Select Register	0	0	0	0	0	0	0	0
D8	GPIO2 Pulse Width Select Register	0	0	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	0	0	0	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	0	0	0	0	0	0	0	0
F0	GPIO Output Enable Register	0	0	0	0	0	0	0	0
F1	GPIO Output Data Register	1	1	1	1	1	1	1	1
F2	GPIO Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO Drive Enable Register	0	0	0	0	0	0	0	0

WDT Device Configuration Registers (LDN 0x07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	WDT Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	WDTRST# Output Enable Register	0	-	-	-	0	0	1	1
F2	Reserved	-	-	-	-	-	-	-	-
F3	Rserved	-	-	-	-	-	-	-	-
F4	Reserved	-	-	-	-	-	-	-	-
F5	WDT Unit Select Register	-	0	0	0	0	0	0	0
F6	WDT Count Register	0	0	0	0	1	0	1	0
F7	Watchdog Timer PME Register	0	0	0	-	-	-	-	-

CIR Configuration Register (LDN 0x08)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	CIR Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	CIR IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	Reserved	-	-	-	-	-	-	-	-
F1	Reserved	-	-	-	-	-	-	-	-
F8	Reserved	0	0	0	0	0	0	0	0
F9	Reserved	0	0	0	0	0	0	0	0
FA	Reserved	1	0	0	0	0	0	0	0
FB	Reserved	0	0	1	1	1	0	1	1
FC	Reserved	0	0	0	0	0	0	0	0
FD	Reserved	0	0	0	0	0	0	0	0
FE	Reserved	0	0	0	0	0	0	0	0

PME, ACPI, Power Saving Device Configuration Registers (LDN 0x0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0
F0	PME Event Enable Register 1	0	0	0	0	-	-	0	-
F1	PME Event Status Register 1	-	-	-	-	-	-	-	-
F2	PME Event Enable Register 2	-	-	-	0	-	-	0	0
F3	PME Event Status Register 2	-	-	-	-	-	-	-	-
F4	Keep Last State Select Register	0	0	0	0	0	1	1	0
F5	VDDOK Delay Select Register	0	0	1	1	1	1	0	0
F6	PCIRST Control Register	0	0	0	1	1	1	1	1
F7	VSBGATE Control Register	-	-	-	-	0	-	0	0
F8	LED VCC Control Register	0	0	0	0	0	0	0	0
F9	LED VSB Control Register	-	0	0	0	0	0	0	0
FA	LED VCC/VSB Additional Control Register	-	0	0	0	-	0	0	0
FD	Reserved	-	-	-	-	-	-	-	-
E0	EuP Enable Register	0	-	-	1	-	-	0	0
E1	EuP Control Register 1	1	1	0	0	0	0	0	0
E2	EuP Control Register 2	-	-	0	0	-	-	0	0
E3	EuP PSIN Debounce Register	0	0	0	1	0	0	1	1
E4	EuP RSMRST Debounce Register	0	0	0	0	1	0	0	1
E5	EuP PSOUT Debounce Register	1	1	0	0	0	1	1	1
E6	EuP PSON Debounce Register	0	0	0	0	1	0	0	1

E7	EuP Deep S5 Delay Register	0	1	1	0	0	0	1	1
E8	EuP Wakeup Event Enable Register 1	-	0	0	-	0	0	0	0
E9	EuP Deep S3 Delay Register	0	0	0	0	1	1	1	1
EC	EuP Wakeup Event Enable Register 2	0	0	0	0	0	0	0	0
ED	EuP Watchdog Control Register	0	0	0	0	-	-	0	0
EE	EuP Watchdog Time Register	0	0	0	0	0	0	0	0

8.1 Global Control Registers

8.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

8.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	01h: Select UART device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 08h: Select CIR device configuration registers. 0ah: Select PME, ACPI & Power Saving device configuration registers.

8.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	10h	Chip ID 1.

8.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	01h	Chip ID2.

8.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1 of Fintek devices.

8.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2 of Fintek devices.

8.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1	SOFTPD_UR	R/W	0	Write “1” to disable UART clock.
0	Reserved	-	-	Reserved.

8.1.8 UART IRQ Sharing Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R/W	0	0: CLKIN is 48MHz 1: CLKIN is 24MHz
6-3	Reserved	-	-	Reserved.
2	TX_DEL_1BIT	R/W	0	0: UART TX transmits data immediately after writing THR. 1: UART TX transmits data one bit time after writing THR.
1-0	Reserved	-	-	Reserved.

8.1.9 Configuration Port Select Register — Index 27h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	PORT_4E_EN	R/W	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT/ Config4E_2E. Pull down to select port 2E/2F.
3-2	Reserved	-	-	Reserved.
1	PWOK_MODE	R/W	-	0: PWOK follows Intel sequence. 1: PWOK follows AMD sequence. This register is power on trapped by GPIO04/PWM/RTS#/STRAP_PWROK. Pull down to select Intel sequence.

0	TIMING_EN	R/W	1	0: Disable timing sequence. 1: Enable timing sequence.

8.1.10 Multi-Function Select Register 0 — Index 28h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO07_ALT_EN	R/W	0	GPIO07_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 60. The function select signal is shown below. FUNC_SEL = { GPIO07_ALT_EN, UR_GP_EN[1:0]} 000, 001, 010: SIN 011: GPIO07 1xx: CIRWB#
6	Reserved	-	-	Reserved
5	GPIO05_ALT_EN	R/W	0	GPIO05_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 58. The function select signal is shown below. FUNC_SEL = { GPIO05_ALT_EN, UR_GP_EN[1:0]} 000: DSR# 001, 010, 011: GPIO05 1xx: BEEP
4	GPIO04_ALT_EN	R/W	0	GPIO04_ALT_EN and UR_GP_EN[0] are used to select the function of Pin 57. The function select signal is shown below. FUNC_SEL = { GPIO04_ALT_EN, UR_GP_EN[0]} 00: RTS# 01: GPIO04 1x: PWM
3	GPIO03_ALT_EN	R/W	0	GPIO03_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 56. The function select signal is shown below. FUNC_SEL = { GPIO03_ALT_EN, UR_GP_EN[1:0]} 000: DTR# 001, 010, 011: GPIO03 1xx: CIRTX

2	GPIO02_ALT_EN	R/W	0	GPIO02_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 55. The function select signal is shown below. FUNC_SEL = { GPIO02_ALT_EN, UR_GP_EN[1:0]} 000: CTS# 001, 010, 011: GPIO02 1xx: CIRLED
1	GPIO01_ALT_EN	R/W	0	GPIO01_CIRWB_EN, GPIO01_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 54. The function select signal is shown below. If GPIO01_CIRWB_EN is set to 1, the pin function is CIRWB#. If GPIO01_CIRWB_EN is set to 0, the pin function is as below. 000: RI# 001, 010, 011: GPIO01 1xx: OVT#
0	GPIO00_ALT_EN	R/W	0	GPIO00_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 53. The function select signal is shown below. FUNC_SEL = { GPIO00_ALT_EN, UR_GP_EN[1:0]} 000: DCD# 001, 010, 011: GPIO00 1xx: SDA

8.1.11 Multi-Function Select Register 1 — Index 29h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-6	UR_GP_EN	R/W	3h	UART/GPIO function select. UR_GP_EN needs to combine with the additional pin function select in index 28h if pin function is more than 3. Please refer to index 28h for more detail. 00 : All Pins for UART 01: SIN/SOUT enable, other pins are GPIOs. 10: SIN/SOUT/RTS# enable, other pins are GPIOs. 11: All pins are GPIOs.
5	GPIO35_EN	R/W	0	FANIN2/GPIO35 function select. 0: The pin function is FANIN2 1: The pin function is GPIO35

4	GPIO34_EN	R/W	0	FANCTL2/GPIO34 function select. 0: The pin function is FANCTL2. 1: The pin function is GPIO34.
3	Reserved	-	-	Reserved
2	WDRST_GP25_EN	R/W	0	GPIO25/LEDVCC/WDRST# function select. If GP25_WDRST_EN is set to 1, the pin function is WDRST#. If GP25_WDRST_EN is set to 0, the pin function is selected by GPIO25_EN. 0: The pin function is LEDVCC. 1: The pin function is GPIO25.
1	GPIO31_EN	R/W	0	VLDT_EN/GPIO31/SDA2 function select. 0: The pin function is VLDT_EN 1: The pin function is GPIO31 This register only has effect when TSI_SDA2_PIN_EN is “0”.
0	GPIO30_EN	R/W	0	VCORE_EN/GPIO30 function select. 0: The pin function is VCORE_EN 1: The pin function is GPIO30

8.1.12 Multi-Function Select Register 2 — Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GP01_CIRWB_EN	R/W	0	GPIO01_CIRWB_EN, GPIO01_ALT_EN and UR_GP_EN[1:0] are used to select the function of Pin 54. The function select signal is shown below. If GPIO01_CIRWB_EN is set to 1, the pin function is CIRWB#. If GPIO01_CIRWB_EN is set to 0, the pin function is as below. FUNC_SEL = {GPIO01_ALT_EN, UR_GP_EN[1:0]} 000: RI# 001, 010, 011: GPIO01 1xx: OVT#

6	GP26_WDRST_EN	R/W	0	SLP_SUS#/WDRST#/RESETCON#/GPIO26 function select. If GP26_WDRST_EN is set to 1, the pin function is WDTRST#. If GP26_WDRST_EN is set to 0, the pin function is as below. Func_sel = {GP26_ALT_EN, GP26_WDRST_EN, GPIO26_EN} 1xx : The pin function is SLP_SUS# 01x: The pin function is WDRST# 000: The pin function is RESETCON#. 001: The pin function is GPIO26.
5	DPWROK_GP23_EN	R/W	1	DPWROK/GPIO23/WDTRST#/FANIN3 function select. The function si controlled by {DPWROK_GP23_EN, FANIN3_GP_EN, GPIO23_EN} 1xx: The pin function is DPWROK. 01x: The pin function is FANIN3. 001: The pin function is GPIO23. 000: The pin function is WDTRST#.
4	PSOUT_GP_EN	R/W	0	PSOUT#/GPIO14 function select. 0: The pin function is PSOUT#. 1: The pin function is GPIO14.
3	FANIN3_GP23_EN	R/W	0	DPWROK/GPIO23/WDTRST#/FANIN3 function select. The function si controlled by {DPWROK_GP23_EN, FANIN3_GP_EN, GPIO23_EN} 1xx: The pin function is DPWROK. 01x: The pin function is FANIN3. 001: The pin function is GPIO23. 000: The pin function is WDTRST#.
2	FANIN3_GP21_EN	R/W	0	GPIO21/OVT#/FANIN3 function select. The function is controlled by {FANIN3_GP21_EN, GPIO21_EN} 1x: The pin function is FANIN3. 01: The pin function is GPIO21. 00: The pin function is OVT#. The priority of FANIN3_GP23_EN is higher than FANIN3_GP21_EN.

1	KB_GP_EN	R/W	0	KCLK/GPIO11/OVT# and KDATA/GPIO10/FANIN3 function select. Pin 14 is controlled by {GP10_ALT_EN(Index 2Ch_bit0), KB_GP_EN} 1x: The pin function is FANIN3. 01: The pin function is GPIO10. 00: The pin function is KDATA. Pin 15 is controlled by {GP11_ALT_EN(Index 2Ch_bit1), KB_GP_EN} 1x: The pin function is OVT#. 01: The pin function is GPIO11. 00: The pin function is KCLK.
0	MO_GP_EN	R/W	1	SUS_ACK#/MDATA/GPIO12 and SUS_WARN#/MCLK/GPIO13/CIRWB# function select. Pin 16 is controlled by {GP12_ALT_EN(Index 2Ch_bit2), MO_GP_EN} 1x: The pin function is SUS_ACK#. 01: The pin function is GPIO12. 00: The pin function is MDATA. Pin 17 is controlled by {GP13_ALT_EN(Index 2Ch_bit3), MO_GP_EN} 11: The pin function is SUS_WARN#. 10: The pin function is CIRWB#. 01: The pin function is GPIO13. 00: The pin fcuntion is MCLK.

8.1.13 Multi-Function Select Register 3 — Index 2Bh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	GPIO27_EN	R/W	0	PSIN#/GPIO27 function select. 0: The pin function is PSIN#. 1: The pin function is GPIO27.

6	GPIO26_EN	R/W	1	SLP_SUS#/WDRST#/RESETCON#/GPIO26 function select. If GP26_WDRST_EN is set to 1, the pin function is WDTRST#. If GP26_WDRST_EN is set to 0, the pin function is as below. Func_sel = {GP26_ALT_EN, GPIO26_EN} 00: The pin function is RESETCON#. 01: The pin function is GPIO26. 1x: The pin function is SLP_SUS#
5	GPIO25_EN	R/W	1	GPIO25/LEDVCC/WDRST# function select. If GP25_WDRST_EN is set to 1, the pin function is WDRST#. If GP25_WDRST_EN is set to 0, the pin function is selected by GPIO25_EN. 0: The pin function is LEDVCC. 1: The pin function is GPIO25.
4	GPIO24_EN	R/W	1	GPIO24/LEDVSB function select. 0: The pin function is LEDVSB. 1: The pin function is GPIO24.
3	GPIO23_EN	R/W	1	DPWROK/GPIO23/WDTRST#/FANIN3 function select. The function si controlled by {DPWROK_GP23_EN, FANIN3_GP_EN, GPIO23_EN} 1xx: The pin function is DPWROK. 01x: The pin function is FANIN3. 001: The pin function is GPIO23. 000: The pin function is WDTRST#.
2	GPIO22_EN	R/W	1	GPIO22/PWM function select. 0: The pin function is PWM. 1: The pin function is GPIO22.
1	GPIO21_EN	R/W	1	GPIO21/OVT#/FANIN3 function select. The function is controlled by {FANIN3_GP21_EN, GPIO21_EN} 1x: The pin function is FANIN3. 01: The pin function is GPIO21. 00: The pin function is OVT#. The priority of FANIN3_GP23_EN is higher than FANIN3_GP21_EN.

0	GPIO20_EN	R/W	1	GPIO20/PME# function select. 0: The pin function is PME#. 1: The pin function is GPIO20.

8.1.14 Multi-Function Select Register 4 — Index 2Ch (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	DSW_ALT_EN	R/W	0	Set this bit "1" to enable VIN3 (pin 45) function as SUS_WARN# and pin 49 function as SUS_ACK#.
6	K8_CHK_S0	R/W	0	0: AMD timing sequence does not check S0/S3/S5 state. 1: AMD timing sequence checks S0/S3/S5 state.
5	Reserved	-	-	Reserved
4	GP26_ALT_EN	R/W	1	SLP_SUS#/WDRST#/RESETCON#/GPIO26 function select. If GP26_WDRST_EN is set to 1, the pin function is WDTRST#. If GP26_WDRST_EN is set to 0, the pin function is as below. Func_sel = {GP26_ALT_EN, GP26_WDRST_EN, GPIO26_EN} 1xx : The pin function is SLP_SUS# 01x: The pin function is WDRST# 000: The pin function is RESETCON#. 001: The pin function is GPIO26.
3	GP13_ALT_EN	R/W	1	SUS_WARN#/MCLK/GPIO13/CIRWB# function select. Pin 17 is controlled by {GP13_ALT_EN, MO_GP_EN (Index 2Ah_bit0)} 11: The pin function is SUS_WARN#. 10: The pin function is CIRWB#. 01: The pin function is GPIO13. 00: The pin fcuntion is MCLK.
2	GP12_ALT_EN	R/W	1	SUS_ACK#/MDATA/GPIO12 and function select. Pin 16 is controlled by {GP12_ALT_EN, MO_GP_EN (Index 2Ah_bit0)} 1x: The pin function is SUS_ACK#. 01: The pin function is GPIO12. 00: The pin function is MDATA.

1	GP11_ALT_EN	R/W	0	KCLK/GPIO11/OVT# function select. Pin 15 is controlled by {GP11_ALT_EN, KB_GP_EN (Index 2Ah_bit1)} 1x: The pin function is OVT#. 01: The pin function is GPIO11. 00: The pin function is KCLK.
0	GP10_ALT_EN	R/W	0	KDATA/GPIO10/FANIN3 function select. Pin 14 is controlled by {GP10_ALT_EN, KB_GP_EN (Index 2Ah_bit1)} 1x: The pin function is FANIN3. 01: The pin function is GPIO10. 00: The pin function is KDATA.

8.1.15 Wakeup Control Register — Index 2Dh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	VSBOK_HYS_DIS	R/W	0	0: Enable VSBOK detect hysteresis. 1: Disable VSBOK detect hysteresis.
5	VSBOK_LVL_SEL	R/W	1	0: VSB3V power good level is 3.05V and not good level is 2.95V. 1: VSB3V power good level is 2.8V and not good level is 2.5V. By VSBOK_HYS_DIS and VSBOK_LVL_SEL, RSMRST# falling edge could be determined: 00: when VSB3V is lower than 2.95V. 01: when VSB3V is lower than 2.5V. 10: when VSB3V is lower than 3.05V. 11: when VSB3V is lower than 2.8V.
4	KEY_SEL_ADD	R/W	0	This bit is added to add more wakeup key function.
3	WAKEUP_EN	R/W	1	0: disable keyboard/mouse wake up. 1: enable keyboard/mouse wake up.

<table>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>00</td><td>This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wakeup Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + USER_WAKEUP_CODE (SPACE)</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + USER_WAKEUP_CODE (SPACE)</td></tr>
<tr><td>1</td><td>11</td><td>USER_WAKEUP_CODE (SPACE)</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>0</td><td>This register select the mouse wake up key.
0: Wake up by click.
1: Wake up by click and movement.</td></tr>
</table>

8.2 UART Registers (LDN 0x01)

8.2.1 UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR_EN	R/W	1	0: disable UART. 1: enable UART.

8.2.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART base address.

8.2.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART base address.

8.2.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELURIRQ	R/W	4h	Select the IRQ channel for UART.

8.2.5 RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	RS485_INV	-	-	Write “1” will invert the RTS# if RS485_EN is set.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. RTS# drive high when transmitting data, otherwise is kept low.
3-0	Reserved	-	-	Reserved.

8.3 Hardware Monitor Register (LDN 0x04)

8.3.1 Hardware Monitor Configuration Registers

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

8.3.2 Device Registers

Before the device registers, the following is a register map order which shows a summary of all registers. Please refer each one register if you want more detail information.

Register CR01 ~ CR03 → Configuration Registers

Register CR0A ~ CR0F → PECI / TSI Control Register

Register CR10 ~ CR3F → Voltage Setting Register

Register CR40~ CR4F → PECI Master Control Register

Register CR60 ~ CR8E → Temperature Setting Register

Register CR90 ~ CRDF → Fan Control Setting Register

→ Fan1 Detail Setting CRA0 ~ CRAF

→ Fan2 Detail Setting CRB0 ~ CRBF

→ Fan3 Detail Setting CRC0 ~ CRCF

8.3.2.1 Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

8.3.2.2 Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	CASE_BEEP_EN	R/W	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.

5-4	OVT_MODE	R/W	0	00: The OVT# will be low active level mode. 01: The OVT# will be low active pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	Reserved	-	-	Reserved
2	CASE_SMI_EN	R/W	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	Reserved	-	-	Reserved

8.3.2.3 Configuration Register — Index 03h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	CASE_STS	R/W	1	Case open status, write 1 to clear if case open event cleared.

8.3.2.4 Configuration Register — Index 08h

Bit	Name	R/W	Default	Description
7-1	SMBUS_ADDR	R/W	7'h26	When AMD TSI or Intel PCH SMBus is enabled, this byte is used as SMBUS_ADDR. SMBUS_ADDR[7:1] is the slave address sent by the embedded master to fetch the temperature.
0	Reserved	-	-	Reserved

8.3.2.5 Configuration Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-6	FUNC_SEL_ADD	R/W	0	Additional function select bits to combine with FUNC_SEL[1:0] for selecting the function of PECI/AMD TSI/Intel IBex.
5-4	Reserved	-	-	Reserved.
3-2	VTT_SEL	R/W	0	PECI (Vtt) voltage select. 00: Vtt is 1.23V 01: Vtt is 1.13V 10: Vtt is 1.00V 11: Vtt is 1.00V

1-0	FUNC_SEL	R/W	0	FUNC_SEL[1:0] combine with FUNC_SEL_ADD[1:0] to select PECI / AMD TSI / Intel IBex functions. The new function select is show below. NEW_FUNC_SEL = {FUNC_SEL_ADD[1:0], FUNC_SEL[1:0]} 0000: AMD TSI/Intel Ibex/ PECI are not enable 0001: AMD TSI (Pin51 is used as SDA) 0010: PECI 0011: Intel IBex (Pin51 is used as SDA) X100: PECI + Intel IBex (Pin50 is used as SDA) X101: AMD TSI (Pin50 is uesd as SDA) X110: PECI + AMD TSI (Pin50 is uesd as SDA) X111: Intel IBex (Pin50 is uesd as SDA) 1000: PECI + Intel IBex (Pin53 is used as SDA) 1001: AMD TSI (Pin53 is uesd as SDA) 1010: PECI + AMD TSI (Pin53 is uesd as SDA) 1011: Intel IBex (Pin53 is uesd as SDA)

8.3.2.6 Configuration Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping() command to find CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 1, i.e. PECI address is 0x31. 0100: CPU is in socket 2, i.e. PECI address is 0x32. 1000: CPU is in socket 3, i.e. PECI address is 0x33. Otherwise are reserved.
3-1	Reserved	-	-	Reserved.
0	DOMAIN1_EN	R/W	0	If the CPU selected is dual core. Set this register 1 to read the temperature of domain1. This bit is also used to send a domain1 PECI3.0 command if PECI is used as a PECI master.

8.3.2.7 Configuration Register — Index 0Ch

Bit	Name	R/W	Default	Description

7-0	TCC_TEMP	R/W	55h	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. When AMD TSI or Intel PCH SMBus is enabled, this byte is used as the offset to be added to the temperature reading of CPU. The range of this register is -128 ~ 127.

8.3.2.8 Configuration Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	TSI_OFFSET	R/W	00h	When PECI and AMD TSI/Intel IBex are enabled at the same time, this byte is used as the offset to be added to the CPU temperature reading of AMD_TSI/Intel IBex. To using this byte as offset of AMD TSI/Intel IBex CPU temperature reading, the TSI_OFFSET_SEL in CR0F must be set to 1. The range of this register is -128 ~ 127.

8.3.2.9 Configuration Register — Index 0Fh

Bit	Name	R/W	Default	Description
7	TSI_LV_SEL	R/W	0	Set this bit to select the SCL/SDA input level. 0: TTL Level 1: Low voltage input level (VIH=0.9v, VIL=0.6v)
6	TSI_OFFSET_SEL	R/W	0	Set this bit to select the offset of AMD TSI/Intel IBex. 0: TCC_TEMP in CR0C 1: TSI_OFFSET in CR0D
5	Reserved	R/W	1	Reserved.
4	TSI03_SEL	R/W	0	If this bit is set to 1, CR7B is able to be written and can also be used to control fan.
3	TSI02_SEL	R/W	0	If this bit is set to 1, CR7C is able to be written and can also be used to control fan.
2	TSI01_SEL	R/W	0	If this bit is set to 1, CR7D is able to be written and can also be used to control fan.

1-0	DIG_RATE_SEL	R/W	0	The accessing rate for AMD TSI/Intel IBex/PECI to access external slave device. 0: Access slave device after 1 diode temperature conversion 1: Access slave device after 2 diode temperature conversion 2: Access slave device after 3 diode temperature conversion 3: Access slave device after 4 diode temperature conversion

Voltage Setting

8.3.2.10 Voltage reading and limit Register — Index 20h- 3Fh

Address	Attribute	Default Value	Description
20h	RO	--	VCC3V reading. The unit of reading is 8mV.
21h	RO	--	V1 (Vcore) reading. The unit of reading is 8mV.
22h	RO	--	V2 reading. The unit of reading is 8mV.
23h	RO	--	V3 reading. The unit of reading is 8mV.
24h	--	--	Reserved
25h	--	--	Reserved
26h	--	--	Reserved
27h	RO	--	VSB3V reading. The unit of reading is 8mV.
28h	RO	--	VBAT reading. The unit of reading is 8mV.
29~2Ch	--	--	Reserved
2Dh	RO	--	FAN1 present fan duty reading
2Eh	RO	--	FAN2 present fan duty reading
2Fh	RO	--	FAN3 present fan duty reading
30~3Fh	--	--	Reserved

PECI 3.0 Command and Register

8.3.2.11 PECI Configuration Register — Index 40h

Bit	Name	R/W	Default	Description
7	RDIAMSR_CMD_EN	R/W	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	0	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	Reserved
3	C3_PTEMP_EN	R/W	0	Set this bit 1 to enable updateing positive value of temperature if the completion code of RdIAMSR() is 0x82.

2	C0_PTEMP_EN	R/W	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

8.3.2.12 PECI Master Control Register — Index 41h

Bit	Name	R/W	Default	Description
7	PECI_CMD_START	W	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)
6-5	Reserved	R	-	Reserved
4	PECI_PENDING	R/W	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	Reserved
2-0	PECI_CMD	R/W	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

8.3.2.13 PECI Master Status Register — Index 42h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	-	Reserved
2	ABORT_FCS	R/WC	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

8.3.2.14 PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA0	R/W	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents "Host ID[7:1] & Retry[0]". Please refer to PECI interface specification for more detail.

8.3.2.15 PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA1	R/W	0	For RdIAMSR() , this byte represents "Processor ID". For RdPkgConfig() and WrPkgConfig() , this byte represents "Index". Please refer to PECI interface specification for more detail.

8.3.2.16 PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA2	R/W	0	For RdIAMSR(), this byte is the least significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of "Parameter". Please refer to PECI interface specification for more detail.

8.3.2.17 PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA3	R/W	0	For RdIAMSR(), this byte is the most significant byte of "MSR Address". For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of "Parameter". Please refer to PECI interface specification for more detail.

8.3.2.18 PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA4	R/W	0	For GetDIB() , this byte represents "Device Info" For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is "Completion Code". For WrPkgConfig(), this byte represents "DATA[7:0]"

8.3.2.19 PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA5	R/W	0	For GetDIB() , this byte represents "Revision Number" For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[7:0]" For WrPkgConfig(), this byte represents "DATA[15:8]"

8.3.2.20 PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA6	R/W	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[15:8]". For WrPkgConfig(), this byte represents "DATA[23:16]"

8.3.2.21 PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Default	Description
7-0	PECI_DATA7	R/W	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[23:16]". For WrPkgConfig(), this byte represents "DATA[31:24]"

8.3.2.22 PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Default	Description

7-0	PECI_DATA8	R/W	0	For RdIAMSR() and RdPkgConfig() , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

8.3.2.23 PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Default	Description
7-0	PECI_DATA9	R/W	0	For RdIAMSR(), this byte represents "DATA[39:32]". For WrPkgConfig(), this byte represents "Completion Code"

8.3.2.24 PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA10	R/W	0	For RdIAMSR(), this byte represents "DATA[47:40]".

8.3.2.25 PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA11	R/W	0	For RdIAMSR(), this byte represents "DATA[55:48]".

8.3.2.26 PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA12	R/W	0	For RdIAMSR(), this byte represents "DATA[63:56]".

Temperature Setting

8.3.2.27 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	Reserved	R	-	Reserved
6	EN_ T2_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	R	-	Reserved
3	Reserved	R	-	Reserved
2	EN_ T2_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R	-	Reserved

8.3.2.28 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	T2_OVT _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
5	T1_OVT _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	T2_EXC _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
1	T1_EXC _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	-	-	Reserved

8.3.2.29 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	-	-	Reserved

8.3.2.30 Temperature Beep Enable Register — Index 63h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved

6	EN_ T2_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	EN_ T2_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	-	-	Reserved

8.3.2.31 T1 Over-OVT and Over-High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-4	T1_OVT_TEMP_SEL	R/W	0	Set this bit to select the temperature source of T1_OVT_LIMIT. 00: Diode T1 Temperature 01: PECI Temperature 10: CPU Temperature of AMD TSI or Intel IBex 11: Max. Temperature of Intel IBex
3-2	Reserved	-	-	Reserved
1-0	T1_HIGH_TEMP_SEL	R/W	0	Set this bit to select the temperature source of T1_HIGH_LIMIT. 00: Diode T1 Temperature 01: PECI Temperature 10: CPU Temperature of AMD TSI or Intel IBex 11: Max. Temperature of Intel IBex

8.3.2.32 OVT Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	EN_T2_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	-	-	Reserved.

8.3.2.33 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	-	-	Reserved

8.3.2.34 TEMP1 Limit Hystersis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	-	-	Reserved

8.3.2.35 TEMP2 and TEMP3 Limit Hystersis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3-0	TEMP2_HYS	R/W	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).

8.3.2.36 DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	PECI_OPEN	RO	0h	When PECI interface is enabled, it indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	RO	0h	When AMD TSI or Intel IBex interface is enabled, it indicates the error of not receiving NACK bit or a timeout occurred.
3	Reserved	-	-	Reserved
2	T2_DIODE_OPEN	RO	0h	Set to 1 when external diode 2 is open or short
1	T1_DIODE_OPEN	RO	0h	Set to 1 when external diode 1 is open or short
0	Reserved	-	-	Reserved

8.3.2.37 Diode T1 Temperature Scale Register -- Index 7Fh

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
3	ADD	R/W	0h	Diode T1 Temperature scale selection. 1: Temp. = Reading Value + Reading Value* $2^{-DIODE\_T1\_SCALE}$ 0: Temp. = Reading Value - Reading Value* $2^{-DIODE\_T1\_SCALE}$
2	Reserved	-	-	Reserved

1-0	SCALE	R/W	0h	When ADD is 1, Diode T1 Temp. is selected by SCALE 00: Temp. = 1 * Reading Value 01: Temp. = 17/16 * Reading Value 10: Temp. = 33/32 * Reading Value 11: Temp. = 65/64 * Reading Value When ADD is 0, Diode T1 Temp. is selected by SCALE 00: Temp. = 1 * Reading Value 01: Temp. = 15/16 * Reading Value 10: Temp. = 31/32 * Reading Value 11: Temp. = 63/64 * Reading Value

8.3.2.38 Temperature — Index 70h- 8Fh

Address	Attribute	Default Value	Description
70h	Reserved	--	Reserved
71h	Reserved	--	Reserved
72h	RO	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	RO	--	Reserved
74h	RO	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h	RO	--	Reserved
76h	RO	--	Reserved
77-79h	RO	--	Reserved
7Ah	RO	--	The data of CPU temperature from digital interface after IIR filter. (Available if Intel IBX or AMD TSI interface is enabled)
7Bh	RO	--	The raw data of PCH temperature from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	RO	--	The raw data of MCH read from digital interface. (Only available if Intel IBX interface is enabled)
7Dh	RO	--	The raw data of maximum temperature from digital interface. (Only available if Intel IBX interface is enabled)
7Eh	RO	--	The data of CPU temperature from digital interface after IIR filter. (Only available if PECI interface is enabled)
80h	--	--	Reserved
81h	--	--	Reserved
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1°C.

86-8Bh	--	--	Reserved
8C~8Dh	--	--	Reserved

Fan Control Setting

8.3.2.39 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	EN_FAN3_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt.. Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

8.3.2.40 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	FAN3_STS	R/W	-	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	-	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	-	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

8.3.2.41 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	FAN3_EXC	RO	-	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	RO	-	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

0	FAN1_EXC	RO	-	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

8.3.2.42 FAN Full Speed Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	FULL_WITH_T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4-0	Reserved	-	-	Reserved.

8.3.2.43 Fan Type Select Register -- Index 94h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	PWM_TYPE	R/W	2'b 10	00: PWM pin output PWM mode (push pull) 01: PWM pin output voltage from DAC 10: PWM pin output PWM mode (open drain) 11: Reserved.
3-2	FANCTL2_TYPE	R/W	2'b 1S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTL2 0: FANCTL2 is pull up by external resistor. 1: FANCLT2 is pull down by internal 100K resistor.
1-0	FANCTL1_TYPE (CPUFAN)	R/W	2'b 10	00: Output PWM mode (push pull) to control fans. 10: Output PWM mode (open drain) to control Intel 4-wire fans.

S: Register default values are decided by trapping.

8.3.2.44 Fan1 Base Temperature for Temperature Adjustment Register -- Index 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Default	Description

7-0	FAN1_BASE _TEMP	R/W	0	This register is used to set the base temperature for FANCTL1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL (CR9F[7]) must be set to “1”.

8.3.2.45 FAN1 Temperature Adjust Rate Register -- Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6-4	TFAN1_ADJ_UP _RATE		3’h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.
3	Reserved	-	-	Reserved
2-0	TFAN1_ADJ_DN _RATE	R/W	3’h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.

8.3.2.46 Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.

3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that defined in 0xB6-0xBE. 10: Manual mode fan control, user can write expect **RPM** count to 0xB2-0xB3, and F71808AU will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F71808AU will output this value duty or voltage to control fan speed.
1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expect **RPM** count to 0xA2-0xA3, and F71808AU will auto control duty cycle (PWM fan type) or voltage(linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F71808AU will output this value duty or voltage to control fan speed.

8.3.2.47 Fan Temperature Adjust Select Register -- Index 96h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2-0	TFAN1_ADJ_SEL	R/W	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 01x: T2 (CR74h) 100: IBX/TSI CPU temperature (CR7Ah) 101: IBX PCH temperature (CR7Bh) 110: IBX MCH temperature (CR7Ch) 111: IBX maximum temperature (CR7Dh) To access this register FAN_PROG_SEL must set to “1”.

8.3.2.48 Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

8.3.2.49 Auto Fan Up Speed update Rate Select Register -- Index 9Bh (FAN_PROG_SEL = 0)

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-2	FAN2_ UP_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1(CPU) _UP_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

8.3.2.50 Auto Fan Down Speed update Rate Select Register -- Index 9Bh (FAN_RATE_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	Direct_Update	R/W	0	0: Fan duty update rate is defined in bit[5:0] 1: Fan duty is updated to the desired
5-4	Reserved	-	-	Reserved.
3-2	FAN2_DOWN_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DOWN_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

8.3.2.51 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE Register — Index 9Ch

Bit	Name	R/W	Default	Description

7-4	FAN2_STOP_DUTY	R/W	5h	When fan start, the FANCTL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FANCTL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP_DUTY	R/W	5h	When fan start, the FANCTL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FANCTL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

8.3.2.52 FAN POWER-ON DEFAULT DUTY-CYCLE/VOLTAGE Register — Index 9Eh

Bit	Name	R/W	Default	Description
7-0	PWRON_DEF_DUTY	R/W	8'h66	Fan duty value immediately loaded after VDD is powered on.

8.3.2.53 Fan Fault Time Register - Index 9Fh

Bit	Name	R/W	Default	Description
7	FAN_PROG_SEL	R/W	0	Set this bit to "1" will enable access registers of other bank.
6	FAN_MNT_SEL	R/W	0	Set this bit to monitor a slower fan.
5-0	Reserved	-	-	Reserved

8.3.2.54 Fan1 Index A0h- AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. **Duty mode(CR96 bit0=1):** This byte is reserved byte.
A3h	R/W	8'h01	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit0=1):** The Value programming in this byte is duty value. In auto fan mode

			(CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

8.3.2.55 VT1 BOUNDARY 1 TEMPERATURE Register – Index A6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP1	R/W	3Ch ($60^{o}C$)	The 1st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **1** register (index AAh). When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **2** register (index ABh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.56 VT1 BOUNDARY 2 TEMPERATURE Register – Index A7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP1	R/W	32h ($50^{o}C$)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **2** register (index ABh). When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **3** register (index ACh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.57 VT1 BOUNDARY 3 TEMPERATURE Register – Index A8

Bit	Name	R/W	Default	Description

7-0	BOUND3TMP1	R/W	28h (40^{o}C)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **3** register (index ACh). When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **4** register (index ADh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.58 VT1 BOUNDARY 4 TEMPERATURE Register – Index A9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP1	R/W	1Eh (30^{o}C)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **4** register (index ADh). When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **5** register (index AEh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.59 FAN1 SEGMENT 1 SPEED COUNT Register – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100% full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.60 FAN1 SEGMENT 2 SPEED COUNT Register – Index ABh

Bit	Name	R/W	Default	Description

7-0	SEC2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.61 FAN1 SEGMENT 3 SPEED COUNT Register – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.62 FAN1 SEGMENT 4 SPEED COUNT Register – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED1	R/W	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.63 FAN1 SEGMENT 5 SPEED COUNT Register – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC5PEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.64 FAN1 Temperature Mapping Select Register – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_TEMP_SEL_DIG	R/W	0	This bit companying with FAN1_TEMP_SEL select the temperature source for controlling FAN1.

6	Reserved	-	0	Reserved
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP_HIGH_EN	R/W	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_UP_RATE register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP_LOW_EN	R/W	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_DN_RATE register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	1	This registers companying with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 100: fan1 follows IBX/TSI CPU temperature (CR7Ah) 101: fan1 follows IBX PCH temperature (CR7Bh). 110: fan1 follows IBX MCH temperature (CR7Ch). 111: fan1 follows IBX maximum temperature (CR7Dh). Otherwise: reserved.

8.3.2.65 Fan2 Index B0h- BFh

Address	Attribute	Default Value	Description

B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. **Duty mode(CR96 bit2=1):** This byte is reserved byte.
B3h	R/W	8'h01	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit2=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

8.3.2.66 VT2 BOUNDARY 1 TEMPERATURE Register – Index B6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP2	R/W	3Ch ($60^{o}C$)	The 1st BOUNDARY temperature for VT2 in temperature mode. When VT2temperature is **exceed** this boundary, FAN2 expect value will load from segment **1** register (index BAh). When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BBh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.67 VT2 BOUNDARY 2 TEMPERATURE Register – Index B7

Bit	Name	R/W	Default	Description

7-0	BOUND2TMP2	R/W	32h ($50^{o}C$)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **2** register (index BBh). When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **3** register (index BCh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.68 VT2 BOUNDARY 3 TEMPERATURE Register – Index B8

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP2	R/W	28h ($40^{o}C$)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **3** register (index BCh). When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **4** register (index BDh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.69 VT2 BOUNDARY 4 TEMPERATURE Register – Index B9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP2	R/W	1Eh ($30^{o}C$)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **4** register (index BDh). When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **5** register (index BEh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

8.3.2.70 FAN2 SEGMENT 1 SPEED COUNT Register – Index BAh

Bit	Name	R/W	Default	Description

7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100% full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.71 FAN2 SEGMENT 2 SPEED COUNT Register – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.72 FAN2 SEGMENT 3 SPEED COUNT Register – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	B2h (70%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.73 FAN2 SEGMENT 4 SPEED COUNT Register – Index BDh

Bit	Name	R/W	Default	Description

7-0	SEC4SPEED2	R/W	99h (60%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.74 FAN2 SEGMENT 5 SPEED COUNT Register – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC5PEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

8.3.2.75 FAN2 Temperature Mapping Select Register – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_TEMP_SEL_DIG	R/W	0	This bit companying with FAN2_TEMP_SEL select the temperature source for controlling FAN2.
6	Reserved	-	-	Reserved
5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_HIGH_EN	R/W	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_UP_RATE register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.

2	FAN2_JUMP_LOW_EN	R/W	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_DN_RATE register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.
1-0	FAN2_TEMP_SEL	R/W	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 100: fan1 follows IBX/TSI CPU temperature (CR7Ah) 101: fan1 follows IBX PCH temperature (CR7Bh). 110: fan1 follows IBX MCH temperature (CR7Ch). 111: fan1 follows IBX maximum temperature (CR7Dh). Otherwise: reserved.

8.3.2.76 Fan3 Index C0h- CFh

Address	Attribute	Default Value	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hFF	FAN3 count reading (LSB).
C2h	Reserved	-	Reserved
C3h	R/W	8'h7F	The Value programming in this byte is duty value for PWM pin.
C4h~CEh	Reserved	-	Reserved

8.3.2.77 PWM Configuration Register – Index CFh

Bit	Name	R/W	Default	Description

7-6	PWM_FREQ_SEL	R/W	0	PWM pin output frequency selection 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220Hz
5-4	Reserved	-	-	Set to select FAN3 filter. (Reserved for Fintek only)
3-1	Reserved	-	-	Reserved
0	PWM_EXT_EN	R/W	0	0: PWM pin output duty is set by programming index C3h 1: PWM pin output duty is controlled by Pin 53 (+) and P 54 (-). There are total 16 steps for external control.

8.3.2.78 TSI Temperature 0 Register– Index E0h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP0	R	-	This is the AMD TSI reading if AMD TSI enable. And will be highest temperature among CPU, MCH and PCH if Intel temperature interface enable. The range is 0~255'C.

8.3.2.79 TSI Temperature 1 Register– Index E1h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP1	R	-	This is the high byte of Intel temperature interface PCH reading. The range is 0~255'C.

8.3.2.80 TSI Temperature 2 Low Byte Register– Index E2h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_LO	R	-	This is the low byte of Intel temperature interface CPU reading. The reading is the fraction part of CPU temperature. Bit 0 indicates the error status. 0: No error. 1: Error code.

8.3.2.81 TSI Temperature 2 High Byte Register– Index E3h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_HI	R	-	This is the high byte of Intel temperature interface CPU reading. The reading is the decimal part of CPU temperature.

8.3.2.82 TSI Temperature 3 Register– Index E4h

Bit	Name	R/W	Default	Description

7-0	TSI_TEMP3	R	-	This is the high byte of Intel temperature interface MCH reading. The range is 0~255'C.

8.3.2.83 SMB Master Block Count Byte – Index ECh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-0	BLOCK_CNT	R/W	0	1. Use the register to specify the byte count of block write protocol. (Support up to 5 bytes of block write protocol). 2. SMB master will save the "Block Read Count" here when receiving a block-read protocol.

8.3.2.84 AMD TSI/Intel IBex Command Byte Register – Index EDh

Bit	Name	R/W	Default	Description
7-0	TSI_CMD	R/W	1h	TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

8.3.2.85 SMB Master Status and Control Register – Index EEh

Bit	Name	R/W	Default	Description
7	TSI_PENDING	R/W	0	Set 1 to pending auto TSI accessing. (In AMD model, auto accessing will issue a send-byte followed a receive-byte; In Intel model, auto accessing will issue a block read). To use the TSI_SCL/TSI_SDA as a SMBus master, set this bit to "1" first.
6	Reserved	-	-	Reserved
5	PROC_KILL	R/W	0	Kill the current SMBus transfer and return the state machine to idle. It will set an fail status if the current transfer is not completed.
4	FAIL_STS	R	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBus transfer.
3	SMB_ABT_ERR	R	0	This is the arbitration lost status if a SMBus command is issued. Auto cleared by next SMBus command.
2	SMB_TO_ERR	R	0	This is the timeout status if a SMBus command is issued. Auto cleared by next SMBus command.
1	SMB_NAC_ERR	R	0	This is the NACK error status if a SMBus command is issued. Auto cleared by next SMBus command.
0	SMB_READY	R	1	0: a SMBus transfer is in process. 1: Ready for next SMBus command.

8.3.2.86 SMB Master Control Register – Index EFh

Bit	Name	R/W	Default	Description
7	SMB_START	W	0	Write "1" to trigger a SMBus Master transfer with the protocol specified by SMB_PROTOCOL.
6-4	Reserved	-	-	Reserved.

3-0	SMB_PROTOCOL	R/W	0	Select what protocol if SMBus transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: process call. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: quick command (read). Otherwise: reserved.

8.4 KBC Registers (LDN 0x05)

8.4.1 KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

8.4.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4;

8.4.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

8.4.4 KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	1h	Select the IRQ channel for keyboard interrupt.

8.4.5 Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description

7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	Ch	Select the IRQ channel for PS/2 mouse interrupt.

8.4.6 Auto Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	0	0: disable auto detect keyboard/mouse swap. 1: enable auto detect keyboard/mouse swap.
6-5	Reserved	-	-	Reserved.
4	KB_MO_SWAP	R/W	0	0: Keyboard/mouse not swap. 1: Keyboard/mouse swap. This bit is set/clear by hardware if AUTO_DET_EN is set to “1”. Users could also program this bit manually.
3	PSEUDO_8408_EN	R/W	0	Set “1” to enable auto response to KBC command. It will return 0xFA, 0xAA for 0xFF command and 0xFA for other commands. This bit is used for GPIO scan code function without PS/2 keyboard.
2-0	Reserved	-	-	Reserved.

8.4.7 User Wakeup Code Register — Index FFh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7-0	USER_WAKEUP_CODE	R/W	29h	This is user define wakeup code. Default is space.

8.5 GPIO Registers (LDN 0x06)

8.5.1 GPIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELGPIRQ	R/W	0h	Select the IRQ channel for GPIO interrupt.

8.5.2 GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
4	GPIO35_OE	R/W	0	0: GPIO35 is in input mode. 1: GPIO35 is in output mode.

4	GPIO34_OE	R/W	0	0: GPIO34 is in input mode. 1: GPIO34 is in output mode.
3	GPIO33_OE	R/W	0	0: GPIO33 is in input mode. 1: GPIO33 is in output mode.
2	GPIO32_OE	R/W	0	0: GPIO32 is in input mode. 1: GPIO32 is in output mode.
1	GPIO31_OE	R/W	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode.
0	GPIO30_OE	R/W	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode.

8.5.3 GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO35_VAL	R/W	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

8.5.4 GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO35_IN	R	-	The pin status of FANIN2/GPIO35
4	GPIO34_IN	R	-	The pin status of FANCTL2/GPIO34.
3	GPIO33_IN	R	-	The pin status of SCL/GPIO33.
2	GPIO32_IN	R	-	The pin status of PECI/SDAT/GPIO32.
1	GPIO31_IN	R	-	The pin status of VLDT_EN/GPIO31
0	GPIO30_IN	R	-	The pin status of VCORE_EN/GPIO30

8.5.5 GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	GPIO35_DRV_EN	R/W	0	0: GPIO35 is open drain in output mode. 1: GPIO35 is push pull in output mode.

4	GPIO34_DRV_EN	R/W	0	0: GPIO34 is open drain in output mode. 1: GPIO34 is push pull in output mode.
3	GPIO33_DRV_EN	R/W	0	0: GPIO33 is open drain in output mode. 1: GPIO33 is push pull in output mode.
2	GPIO32_DRV_EN	R/W	0	0: GPIO32 is open drain in output mode. 1: GPIO32 is push pull in output mode.
1	GPIO31_DRV_EN	R/W	0	0: GPIO31 is open drain in output mode. 1: GPIO31 is push pull in output mode.
0	GPIO30_DRV_EN	R/W	0	0: GPIO30 is open drain in output mode. 1: GPIO30 is push pull in output mode.

8.5.6 Event PME Enable Register — Index C4h (* Reset by LRESET#)

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO01_PME_EN	R/W	0*	When GPIO01_PME_STS is 1 and GPIO01_PME_EN is set to 1, a GPIO PME event will be generated.
3	GPIO00_PME_EN	R/W	0*	When GPIO00_PME_STS is 1 and GPIO00_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO05_PME_EN	R/W	0*	When GPIO05_PME_STS is 1 and GPIO05_PME_EN is set to 1, a GPIO PME event will be generated.
1	GPIO31_PME_EN	R/W	0	When GPIO31_PME_STS is 1 and GPIO30_PME_EN is set to 1, a GPIO PME event will be generated.
0	GPIO30_PME_EN	R/W	0	When GPIO30_PME_STS is 1 and GPIO30_PME_EN is set to 1, a GPIO PME event will be generated.

8.5.7 GPIO3 Input Detection Select Register — Index C5h (*reset by LRESET#)

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO01_DET_SEL	R/W	0	When GPIO01 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
3	GPIO00_DET_SEL	R/W	0	When GPIO00 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

2	GPIO05_DET_SEL	R/W	0*	When GPIO05 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
1	GPIO31_DET_SEL	R/W	0*	When GPIO31 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
0	GPIO30_DET_SEL	R/W	0*	When GPIO30 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

8.5.8 GPIO3 Event Status Register — Index C6h (*reset by LRESET#)

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO01_PME_STS	R/WC	0	When GPIO01 is in input mode and a GPIO01 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
3	GPIO00_PME_STS	R/WC	0	When GPIO00 is in input mode and a GPIO00 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
2	GPIO05_PME_STS	R/WC	0*	When GPIO05 is in input mode and a GPIO05 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1	GPIO31_PME_STS	R/WC	0*	When GPIO31 is in input mode and a GPIO31 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
0	GPIO30_PME_STS	R/WC	0*	When GPIO30 is in input mode and a GPIO30 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.

8.5.9 GPIO05 KB Emulation Key Code Register — Index CBh

Bit	Name	R/W	Default	Description

0	GP05_KB_CODE	R/W	0	The make code of GP05 keyboard emulation key. The break code is GP05_KB_CODE + 0x80.

8.5.10 GPIO31 KB Emulation Key Code Register — Index CCh

Bit	Name	R/W	Default	Description
0	GP31_KB_CODE	R/W	0	The make code of GP31 keyboard emulation key. The break code is GP31_KB_CODE + 0x80.

8.5.11 GPIO30 KB Emulation Key Code Register — Index CDh

Bit	Name	R/W	Default	Description
0	GP30_KB_CODE	R/W	0	The make code of GP30 keyboard emulation key. The break code is GP30_KB_CODE + 0x80.

8.5.12 KB Emulation Key Prefix Code Register — Index CEh

Bit	Name	R/W	Default	Description
0	PRE_KB_CODE	R/W	0xe0	The prefix code when PRE_CODE_EN is set. Two byte will send when key is pressed or released. For example, when GP30 is pressed, 0xe0 will be sent first and then GP30_KB_CODE is sent.

8.5.13 Event KBC Control Register — Index CFh

Bit	Name	R/W	Default	Description
7	GP_KBC_EN	R/W	0	Set this bit to enable KeyBoard key emulation function.
6	PRE_CODE_EN	R/W	1	0: Emulation code is one byte decided by make code. 1: Emulation code is two bytes with pre-fix defined in PRE_CODE.
5	GP05_BRK_STS	R/WC	0	The KeyBoard Key emulation status of break code by GPIO05. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. GP05_BRK_STS will be cleared after host reading IO port 0x0060.
4	GP05_MAKE_STS	R/WC	0	The KeyBoard Key emulation status of make code by GPIO05. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. GP05_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time is 0.5 ~ 1sec with 50ms repeat time.
3	GP31_BRK_STS	R/WC	0	The KeyBoard Key emulation status of break code by GPIO31. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. GP31_BRK_STS will be cleared after host reading IO port 0x0060.

2	GP31_MAKE_STS	R/WC	0	The KeyBoard Key emulation status of make code by GPIO31. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. GP31_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time is 0.5 ~ 1sec with 50ms repeat time.
1	GP30_BRK_STS	R/WC	0	The KeyBoard Key emulation status of break code by GPIO30. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. GP30_BRK_STS will be cleared after host reading IO port 0x0060.
0	GP30_MAKE_STS	R/WC	0	The KeyBoard Key emulation status of make code by GPIO30. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. GP30_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time is 0.5 ~ 1sec with 50ms repeat time.

8.5.14 GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

8.5.15 GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	0	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs 1 when in output mode.
6	GPIO26_VAL	R/W	0	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs 1 when in output mode.
5	GPIO25_VAL	R/W	0	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.

4	GPIO24_VAL	R/W	0	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	0	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	0	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	0	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	0	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

8.5.16 GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of PSIN#/GPIO27.
6	GPIO26_IN	R	-	The pin status of RESETCON#/WDRST#/GPIO26.
5	GPIO25_IN	R	-	The pin status of GPIO25/LEDVCC.
4	GPIO24_IN	R	-	The pin status of GPIO24/LEDVSB.
3	GPIO23_IN	R	-	The pin status of 5VA_PWOK# / GPIO23 / WDTRST# / FANIN3.
2	GPIO22_IN	R	-	The pin status of GPIO22/PWM/ERP_CTRL1#.
1	GPIO21_IN	R	-	The pin status of GPIO21/FANIN3/OVT#.
0	GPIO20_IN	R	-	The pin status of GPIO20/PME#.

8.5.17 GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Default	Description
7	GPIO27_DRV_EN	R/W	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	0	GPIO23 is open drain in output mode.
2	GPIO22_DRV_EN	R/W	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

8.5.18 GPIO2 PME Enable Register — Index D4h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.

5	GPIO25_PME_EN	R/W	0	When GPIO25_PME_STS is 1 and GPIO25_PME_EN is set to 1, a GPIO PME event will be generated.
4	GPIO24_PME_EN	R/W	0	When GPIO24_PME_STS is 1 and GPIO24_PME_EN is set to 1, a GPIO PME event will be generated.
3	GPIO23_PME_EN	R/W	0	When GPIO23_PME_STS is 1 and GPIO23_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO22_PME_EN	R/W	0	When GPIO22_PME_STS is 1 and GPIO22_PME_EN is set to 1, a GPIO PME event will be generated.
1-0	Reserved	-	-	Reserved.

8.5.19 GPIO2 Input Detection Select Register — Index D5h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO25_DET_SEL	R/W	0	When GPIO25 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
4	GPIO24_DET_SEL	R/W	0	When GPIO24 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
3	GPIO23_DET_SEL	R/W	0	When GPIO23 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
2	GPIO22_DET_SEL	R/W	0	When GPIO22 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
1-0	Reserved	-	-	Reserved.

8.5.20 GPIO2 Event Status Register — Index D6h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO25_PME_STS	R/WC	0	When GPIO25 is in input mode and a GPIO25 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
4	GPIO24_PME_STS	R/WC	0	When GPIO24 is in input mode and a GPIO24 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.

3	GPIO23_PME_STS	R/WC	0	When GPIO23 is in input mode and a GPIO23 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
2	GPIO22_PME_STS	R/WC	0	When GPIO22 is in input mode and a GPIO22 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1-0	Reserved	-	-	Reserved.

8.5.21 GPIO2 Output Mode Status Register — Index D7h

Bit	Name	R/W	Default	Description
7-6	GPIO25_MODE	R/W	0	GPIO25_MODE is used to select the output mode of GPIO25: 00: High Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode
5-4	GPIO24_MODE	R/W	0	GPIO24_MODE is used to select the output mode of GPIO24: 00: Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode
3-2	GPIO23_MODE	R/W	0	GPIO23_MODE is used to select the output mode of GPIO23: 00: Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode
1-0	GPIO22_MODE	R/W	0	GPIO22_MODE is used to select the output mode of GPIO22: 00: Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode

8.5.22 GPIO2 Pulse Width of Pulse Mode Status Register — Index D8h

Bit	Name	R/W	Default	Description
7-6	GPIO25_PW_SEL	R/W	0	GPIO25_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms
5-4	GPIO24_PW_SEL	R/W	0	GPIO24_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms

3-2	GPIO23_PW_SEL	R/W	0	GPIO23_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms
1-0	GPIO22_PW_SEL	R/W	0	GPIO22_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms

8.5.23 GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

8.5.24 GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

8.5.25 GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.

4	GPIO14_IN	R	-	The pin status of PSOUT#/GPIO14.
3	GPIO13_IN	R	-	The pin status of SUS_WARN#/MCLK/GPIO13/CIRWB#.
2	GPIO12_IN	R	-	The pin status of SUS_ACK#/MDAT/GPIO12.
1	GPIO11_IN	R	-	The pin status of KCLK/GPIO11.
0	GPIO10_IN	R	-	The pin status of KDAT/GPIO10.

8.5.26 GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_DRV_EN	R/W	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

8.5.27 GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	GPIO07_OE	R/W	0	0: GPIO07 is in input mode. 1: GPIO07 is in output mode.
6	GPIO06_OE	R/W	0	0: GPIO06 is in input mode. 1: GPIO06 is in output mode.
5	GPIO05_OE	R/W	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.
2	GPIO02_OE	R/W	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode.
1	GPIO01_OE	R/W	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode.
0	GPIO00_OE	R/W	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode.

8.5.28 GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	GPIO07_VAL	R/W	1	0: GPIO07 outputs 0 when in output mode. 1: GPIO07 outputs 1 when in output mode.

6	GPIO06_VAL	R/W	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs 1 when in output mode.
5	GPIO05_VAL	R/W	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

8.5.29 GPIO Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	GPIO07_IN	R	-	The pin status of GPIO07/CIRWB#/GPIO07.
6	GPIO06_IN	R	-	The pin status of GPIO06/ SOUT/2E_4E.
5	GPIO05_IN	R	-	The pin status of GPIO05/BEEP/DSR#.
4	GPIO04_IN	R	-	The pin status of GPIO04/PWM/RTS#.
3	GPIO03_IN	R	-	The pin status of GPIO03/CIR_TX/DTR#.
2	GPIO02_IN	R	-	The pin status of GPIO02/CIR_LED/CTS#.
1	GPIO01_IN	R	-	The pin status of GPIO01/OVT#/RI#.
0	GPIO00_IN	R	-	The pin status of GPIO00/SDA/DCD#.

8.5.30 GPIO Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	GPIO07_DRV_EN	R/W	0	0: GPIO07 is open drain in output mode. 1: GPIO07 is push pull in output mode.
6	GPIO06_DRV_EN	R/W	0	0: GPIO06 is open drain in output mode. 1: GPIO06 is push pull in output mode.
5	GPIO05_DRV_EN	R/W	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode.
4	GPIO04_DRV_EN	R/W	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode.
3	GPIO03_DRV_EN	R/W	0	0: GPIO03 is open drain in output mode. 1: GPIO03 is push pull in output mode.
2	GPIO02_DRV_EN	R/W	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode.
1	GPIO01_DRV_EN	R/W	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode.
0	GPIO00_DRV_EN	R/W	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode.

8.6 WDT Registers (LDN 0x07)

Configuration Registers

8.6.1 WDT Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	WDT_EN	R/W	0	0: disable watch dog timer 1: enable watch dog timer

8.6.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of WDT base address.

8.6.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of WDT base address.

Device Registers

8.6.4 Configuration Register — Index F0h (offset + 00h)

Bit	Name	R/W	Default	Description
7	WDOUT_EN	R/W	0	If this bit is set to 1 and watchdog timeout event occurs, WDTRST# output is enabled.
6-4	Reserved	-	-	Reserved
3-0	Reserved	-	-	Reserved

8.6.5 Register — Index F2h~F4h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

8.6.6 Watchdog Timer Configuration Register 1— Index 05h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.

3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1:0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

8.6.7 Watchdog Timer Configuration Register 2 — Index 06h

Bit	Name	R/W	Default	Description
7:0	WD_TIME	R/W	Ah	Time of watchdog timer

8.6.8 WDT PME Register — Index 07h

Bit	Name	R/W	Default	Description
7	WDT_PME	R	0	WDT PME real time status.
6	WDT_PME_EN	R/W	0	0: Disable WDT PME. 1: Enable WDT PME.
5	WDT_PME_ST	R/W	0	0: No WDT PME occurred. 1: WDT PME occurred. The WDT PME is occurred one unit before WDT timeout.
4-0	Reserved	-	-	Reserved

8.7 CIR Registers (LDN 0x08)

Configuration Registers

8.7.1 CIR Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	CIR_EN	R/W	0	0: disable CIR 1: enable CIR

8.7.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of CIR base address.

8.7.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of CIR base address.

8.7.4 CIRIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELCIRIRQ	R/W	0h	Select the IRQ channel for CIR interrupt.

Device Register

8.7.5 CIR Status Register — Index 00h

Bit	Name	R/W	Default	Description
7	CIR_IRQ_EN	R/W	0	CIR IRQ function enable
6-4	Reserved	R	0	Reserved
3	TX_FINISH	R/W	0	CIR transmittion finish status. Write 1 clear.
2	TX_UNDERRUN	R/W	0	CIR transmitttion underrun status. Write 1 clear.
1	RX_TIMEOUT	R/W	0	CIR receiver timeout status. Write 1 clear.
0	RX_RECEIVE	R/W	0	CIR receiver receives data status. Write 1 clear.

8.7.6 CIR RX Data Register — Index 01h

Bit	Name	R/W	Default	Description
7-0	RX_DATA	R	-	CIR received data is read from here.

8.7.7 CIR TX Control Register — Index 02h

Bit	Name	R/W	Default	Description
7	TX_START	R/W	0	Set 1 to start CIR TX transmittion and will be auto cleared if transmittion is finished.
6	TX_END	R/W	0	Set 1 to indicate that all TX data has been written to CIR TX FIFO.
5-0	Reserved	-	-	Reserved

8.7.8 CIR TX Data Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	TX_DATA	R/W	-	The transmittion data should be written to TX_DATA.

8.7.9 CIR Control Register — Index 04h

Bit	Name	R/W	Default	Description
7-0	CIR_CMD	R/W	0	Host writes command to CIR.

8.8 PME, ACPI, Power Saving Registers (LDN 0x0A)

Configuration Register

8.8.1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

8.8.2 EuP Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	EuP_EN	R/W	0	0 : disable EuP function 1: enable EuP function
6-5	Reserved	-	0	Reserved.
4	VSB_CTRL_1_EN	R/W	1	VSB_CTRL_1 enable. 0: disable VSB_CTRL_1 function. 1: Function of pin 20 is VSB_CTRL_1
3-2	Reserved	-	-	Reserved
1	EVENT_PME_EN	R/W	0	EVENT_IN# PME event enable. 0: disable EVENT_IN# PME event. 1: enable EVENT_IN# PME event
0	EVENT_PSOUT_EN	R/W	0	EVENT_IN# PSOUT event enable. 0: disable EVENT_IN# PSOUT event. 1: enable EVENT_IN# PSOUT event

8.8.3 EuP control register — Index E1h

Bit	Name	R/W	Default	Description
7-6	Boot_Mode	R/W	11	Write these two bits to select Boot Mode for Always Off/ Always On/ Keep Last State. 00:Default Always Off 11:Support Always On and Keep Last State 10:Reserved 01:Reserved
5	S3 _CTRL_1_DIS	R/W	0	If clear to “0” CTRL_1 will output Low when enter deep S3 state. Else If set to “1” CTRL_1 will output High when enter deep S3 state.
4	S3 _CTRL_0_DIS	R/W	0	If clear to “0” CTRL_0 will output Low when enter deep S3 state. Else If set to “1” CTRL_0 will output High when enter deep S3 state.
3	S5 _CTRL_1_DIS	R/W	1	If clear to “0” CTRL_1 will output Low when S5 state. Else If set to “1” CTRL_1 will output High when S5 state.
2	S5 _CTRL_0_DIS	R/W	1	If clear to “0” CTRL_0 will output Low when S5 state. Else If set to “1” CTRL_0 will output High when S5 state.
1	AC_ CTRL_1_DIS	R/W	0	If clear to “0” CTRL_1 will output Low when after AC lost. Else If set to “1” CTRL_1 will output High when after AC lost.

0	AC_ CTRL_0_DIS	R/W	0	If clear to “0” CTRL_0 will output Low when after AC lost. Else If set to “1” CTRL_0 will output High when after AC lost.

8.8.4 EuP control register — Index E2h

Bit	Name	R/W	Default	Description
7	AC_LOST	R/WC	-	Set 1 if AC lost, and write 1 to clear.
6	Reserved	R/W	0	Reserved
5	VSB_CTRL_EN[1]	R/W	1’b0	0: disable eup_ctrl2 assert rsmrst low 1: enable eup_ctrl2 assert rsmrst low
4	VSB_CTRL_EN[0]	R/W	1’b0	0: disable eup_ctrl1 assert rsmrst low 1: enable eup_ctrl1 assert rsmrst low
3	S5_DET_S5#	R/W	1	Device into S5 state will check S5# signal and VCC_IN pin status, but when user clear this bit to 0. Device into S5 state will not check S5# become low.
2	S5_DET_VCC	R/W	1	Device into S5 state will check S5# signal and VCC_IN pin status, but when user clear this bit to 0. Device into S5 state will not check VCC_IN become low.
1	RSMRST_DET_5V_N	R/W	0	Device detects VSB5V power ok (4.4V) and VSB3V_IN become high, and after 60ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check VSB5V power ok.
0	Reserved	-	-	Reserved.

8.8.5 EuP PSIN deb-register — Index E3h

Bit	Name	R/W	Default	Description
.7-0	PS_DEB_TIME	R/W	0x13	PS_IN pin input de-bounce time default is 20mSec

8.8.6 EuP RSMRST deb-register — Index E4h

Bit	Name	R/W	Default	Description
7-0	RSMRST_DEB_TIME	R/W	0x09	RSMRST internal de-bounce time default is 10mSec

8.8.7 EuP PSOUT deb-register — Index E5h

Bit	Name	R/W	Default	Description
7-0	PS_OUT_PULSE_W	R/W	0xC7	PS_OUT_OUT output Pulse width default is 200mSec low pulse

8.8.8 EuP PSON deb-register — Index E6h

Bit	Name	R/W	Default	Description
7-0	PS_ON_DEB_TIME	R/W	0x09	PSON_IN pin input de-bounce time default is 10mSec

8.8.9 EuP S5 deb-register — Index E7h

Bit	Name	R/W	Default	Description

7-0	S5_DEL_TIME	R/W	0x63	Delay time for S5 to deep S5 state. The unit of this byte is 64ms. Default is 6.4Sec

8.8.10 EuP Wakeup Event Enable Register — Index E8h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	CIR_WAKEUP_EN	R/W	0	Enable CIR PME event to wakeup.
5	RI_WAKEUP_EN	R/W	0	Enable RI# PME event to wakeup.
4	Reserved	-	-	Reserved.
3	GP_WAKEUP_EN	R/W	0	Enable GPIO PME event to wakeup.
2	TMOUT_WAKEUP_EN	R/W	0	Enable EuP Watchdog Timer timeout event to wakeup. See index EDh and EEh.
1	MO_WAKEUP_EN	R/W	0	Enable Mouse PME event to wakeup.
0	KB_WAKEUP_EN	R/W	0	Enable Keyboard PME event to wakeup.

8.8.11 EuP S3 Delay register — Index E9h

Bit	Name	R/W	Default	Description
7-0	S3_DEL_TIME	R/W	0x0F	Delay time for S3 to deep S3 state. The unit of this byte is 64ms. Default is 1.024Sec

8.8.12 EuP Wakeup Event Enable Register 2— Index ECh

Bit	Name	R/W	Default	Description
7	PIN31_WAEKUP_EN	R/W	0	Enable falling edge of pin 31 to trigger a wakeup event.
6	PIN27_WAEKUP_EN	R/W	0	Enable falling edge of pin 27 to trigger a wakeup event.
5	PIN23_WAEKUP_EN	R/W	0	Enable falling edge of pin 23 to trigger a wakeup event.
4	PIN22_WAEKUP_EN	R/W	0	Enable falling edge of pin 22 to trigger a wakeup event.
3	PIN21_WAEKUP_EN	R/W	0	Enable falling edge of pin 21 to trigger a wakeup event.
2	PIN20_WAEKUP_EN	R/W	0	Enable falling edge of pin 20 to trigger a wakeup event.
1	PIN19_WAEKUP_EN	R/W	0	Enable falling edge of pin 19 to trigger a wakeup event.
0	PIN18_WAEKUP_EN	R/W	0	Enable falling edge of pin 18 to trigger a wakeup event.

8.8.13 EuP Watchdog Control Register —Index EDh

Bit	Name	R/W	Default	Description
7-6	EUP_MODE	R/W	00	EuP mode select. 00: Fintek G3' mode. ERP_CTRL# is controlled with Fintek mechanism. 01: Intel DSW + Fintek G3'. 10: reserved. 11: Intel DSW.
5	DPWROK_CTRL1_EN	R/W	0	DPWROK will follow ERP_CTRL1# if this bit is set.
4	WD_TMOUT	R/WC	0	EuP watchdog timer timeout status. Write 1 to clear.
3-2	Revered	-	-	Reserved.
1	WD_UNIT	R/W	0	0: unit of WD_TIME is 1 sec. 1: unit of WD_TIME is 1 minute.
0	WD_EN	R/W	0	Enable EuP watchdog timer.

8.8.14 EuP Watchdog Time Register —Index EEh

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	EuP watchdog timer count time register. Start to count down when WD_EN is set. When reaching 0, WD_EN will auto clear and WD_TMOUT is set. A wakeup event will assert if enabled.

8.8.15 PME Event Enable Register 1— Index F0h

Bit	Name	R/W	Default	Description
7	WDT_PME_EN	R/W	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
6	MO_PME_EN	R/W	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
5	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3-2	Reserved	-	-	Reserved
1	UR_PME_EN	R/W	0	UART PME event enable. 0: disable UART PME event. 1: enable UART PME event.
0	Reserved	-	-	Reserved

8.8.16 PME Event Enable Register 2 — Index F1h

Bit	Name	R/W	Default	Description
7	WDT_PME_ST	R/WC	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	MO_PME_ST	R/WC	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/WC	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/WC	-	Hardware monitor PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
3-2	Reserved	-	-	Reserved

1	UR_PME_ST	R/W	-	UART PME event status. 0: UART has no PME event. 1: UART has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	Reserved	-	-	Reserved

8.8.17 PME Event Status Register — Index F2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	CIR_PME_EN	R/W	0	CIR PME event enable. 0: disable CIR PME event. 1: enable CIR PME event.
3-2	Reserved	-	-	Reserved
1	RI_PME_EN	R/W	0	RI# PME event enable. 0: disable RI# PME event. 1: enable RI# PME event.
0	GP_PME_EN	R/W	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.

8.8.18 PME Event Status Register — Index F3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	CIR_PME_ST	R/W	-	CIR PME event status. 0: CIR has no PME event. 1: CIR has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	EUP_PME_ST	R/W	-	EUP PME event status. 0: EUP has no PME event. 1: EUP has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	Reserved	-	-	Reserved
1	RI_PME_ST	R/W	-	RI# PME event status. 0: RI# has no PME event. 1: RI# has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	GP_PME_ST	R/W	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.

8.8.19 Keep Last State Select Register — Index F4h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	EN_CIRWAKEUP	R/W	0	Set one to enable CIR wakeup event asserted via PWSOUT#.

5	EN_GPWAKEUP	R/W	0	Set one to enable GPIO wakeup event asserted via PWSOUT#.
4	EN_KBWAKEUP	R/W	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : Keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

8.8.20 VDDOK Delay Register — Index F5h

Bit	Name	R/W	Default	Description
7-6	PWROK_DELAY	R/W	0	The additional PWROK delay. 00: no delay 01: 100ms. 10: 200ms 11: 400ms.
5	RSTCON_EN	R/W	1	0: RESETCON# will assert via PWROK. 1: RESETCON# will assert via RESETOUT1# and RESETOUT2#.
4-3	VDD_DELAY	R/W	11	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms
2-0	Reserved	-	-	Reserved.

8.8.21 PCIRST Control Register — Index F6h

Bit	Name	R/W	Default	Description
7	S3_SEL	R/W	0	Select the KBC S3 state. 0: Enter S3 state when internal VDD3VOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	PSON_DEL_EN	R/W	0	0: PSON# is the inverted of S3# signal. 1: PSON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
5-2	Reserved	-	-	Reserved.
1	RESETOUT2_GATE	R/W	1	Write “0” to this bit will force RESETOUT2# to sink low.
0	RESETOUT1_GATE	R/W	1	Write “0” to this bit will force RESETOUT1# to sink low.

8.8.22 Power Sequence Control Register — Index F7h

Bit	Name	R/W	Default	Description
7-4	Reserved	R/W	0	Dummy register.

3	WDT_PWROK_EN	R/W	0	0: Disable WDT assert to PWROK pin. 1: Enable WDT assert to PWROK pin.
2	PWROK_250MS	W	0	Write “1” to generate a 250ms low pulse from PWROK pin.
1	S3_Gate_TRI	R/W	0	0: 3VSBSW# sinks low in S5 state. 1: 3VSBSW# is driving high in S5 state.
0	Reserved	-	-	Reserved.

8.8.23 LED VCC Mode Select Register — Index F8h

Bit	Name	R/W	Default	Description
7	LED_VCC_INV_DIS	R/W	0	Invert LED_VCC clock output.
6	LED_VCC_DS3	R/W	0	Enable LED_VCC deep S3 mode. LED_VCC will output 0.25Hz clock with 75% duty when enter deep S3 state.
5-4	LED_VCC_S5_MODE	R/W	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VCC_S3_MODE	R/W	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VCC_S0_MODE	R/W	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

8.8.24 LED VSB Mode Select Register — Index F9h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	LED_VSB_DS3	R/W	0	Enable LED_VSB deep S3 mode. LED_VSB will output 0.25Hz clock with 75% duty when enter deep S3 state.
5-4	LED_VSB_S5_MODE	R/W	0	Select LED_VSB mode in S5 state. The mode is controlled by {LED_VSB_S5_ADD, LED_VSB_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VSB_S3_MODE	R/W	0	Select LED_VSB mode in S3 state. The mode is controlled by {LED_VSB_S3_ADD, LED_VSB_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VSB_S0_MODE	R/W	0	Select LED_VSB mode in S0 state. The mode is controlled by {LED_VSB_S0_ADD, LED_VSB_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

8.8.25 LED Mode Select Add Register — Index Fah

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved

6	LED_VSB_S5_ADD	R/W	0	Select LED_VSB mode in S5 state. The mode is controlled by {LED_VSB_S5_ADD, LED_VSB_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
5	LED_VSB_S3_ADD	R/W	0	Select LED_VSB mode in S3 state. The mode is controlled by {LED_VSB_S3_ADD, LED_VSB_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
4	LED_VSB_S0_ADD	R/W	0	Select LED_VSB mode in S0 state. The mode is controlled by {LED_VSB_S0_ADD, LED_VSB_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3	Reserved	-	-	Reserved
2	LED_VCC_S3_MODE	R/W	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

1	LED_VCC_S3_MODE	R/W	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
0	LED_VCC_S0_MODE	R/W	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

8.8.26 Intel DSW Delay Select Register — Index FCh

Bit	Name	R/W	Default	Description
7-4	Reserved	R/W	-	Reserved
3-0	DSW_DELAY	R/W	7h	This is the delay time for SUS_ACK# and SUS_WARN#. Time unit is 0.5s.

8.8.27 RI De-bounce Select Register — Index FEh

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved
1-0	RI_DB_SEL	R/W	0	Select RI de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V) (Note)

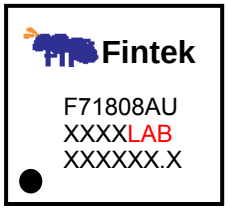
PARAMETER	CONDITONS	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 145 °C, VCC = 3.0V to 3.6V 0 °C <T_D < 60°C 100 °C <T_D < 145°C		± 1 ± 1	± 3 ± 3	°C
Supply Voltage range		3.0	3.3	3.6	V
Average operating supply current			8		mA
Standby supply current			5		uA
Resolution			1		°C
Power on reset threshold			2.2	2.4	V
Diode source current	High Level		95		uA
	Low Level		10		uA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{12ts5v}-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OD_{16t5v}-TTL level bi-directional pin, Open-drain output with16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V

Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/O_{12t}- TTL level bi-directional pin, Output pin with 12mA source-sink capability.						
Input Low Threshold Voltage	Vt-			0.6	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	0.9			V	VDD = 3.3 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{ts} - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN_{t5v} - TTL level input pin with 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN_{ts5v} - TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
OD_{12}-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{12\text{-}5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
OD_{24}-Open-drain output with 24 mA sink capability.						
Output Low Current	IOL		-24		mA	VOL = 0.4V
$OD_{16\text{-}u10\text{-}5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
O_8- Output pin with 8 mA source-sink capability.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
$O_{8\text{-}u47\text{-}5v}$- Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						

10.Ordering Information

Part Number	Package Type	Production Flow
F71808AU	64-TQFP Green Package	Commercial, 0°C to +70°C



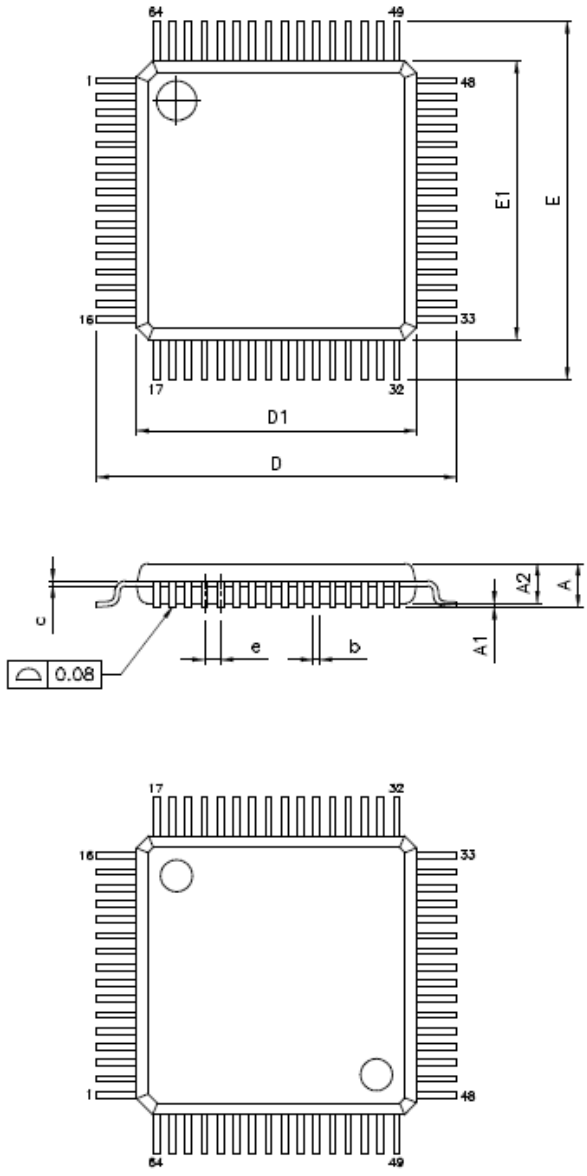
Version Identification:

Ex: For LAB version

The version shows on RED area. Ex: LAB

11.Package Dimensions

64 TQFP



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

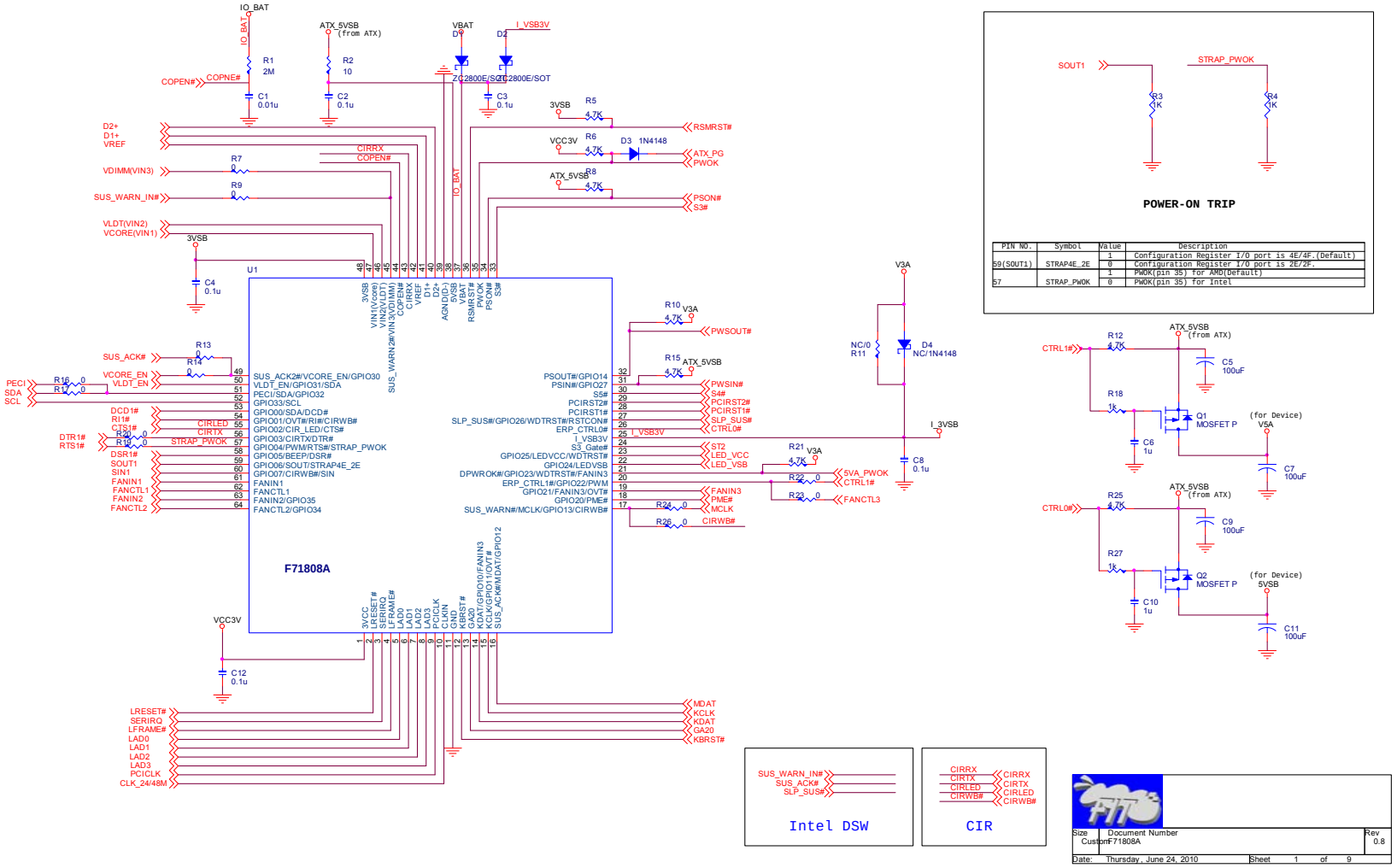
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

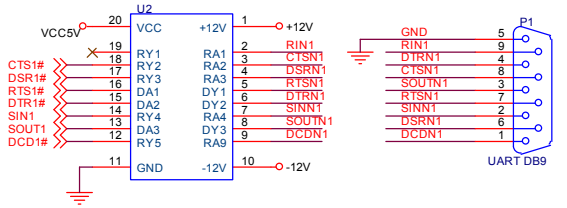
Feature Integration Technology Inc.

Headquarters
3F-7, No 36, Tai Yuan St.,
Chupei City, Hsinchu, Taiwan 302, R.O.C.
TEL : 886-3-5600168
FAX : 886-3-5600166
www: http://www.fintek.com.tw

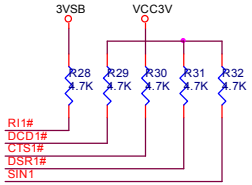
Taipei Office
Bldg. K4, 7F, No.700, Chung Cheng Rd.,
Chungho City, Taipei, Taiwan 235, R.O.C.
TEL : 866-2-8227-8027
FAX : 866-2-8227-8037

12. Application Circuits

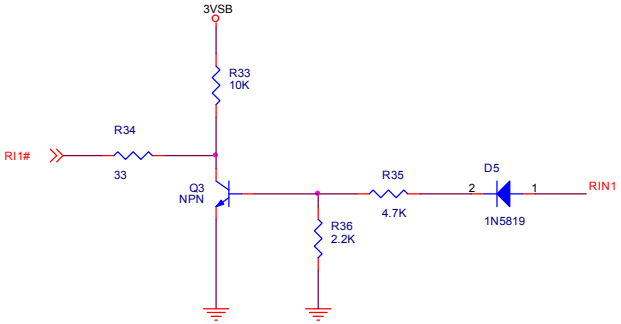




UART 1 PORT INTERFACE

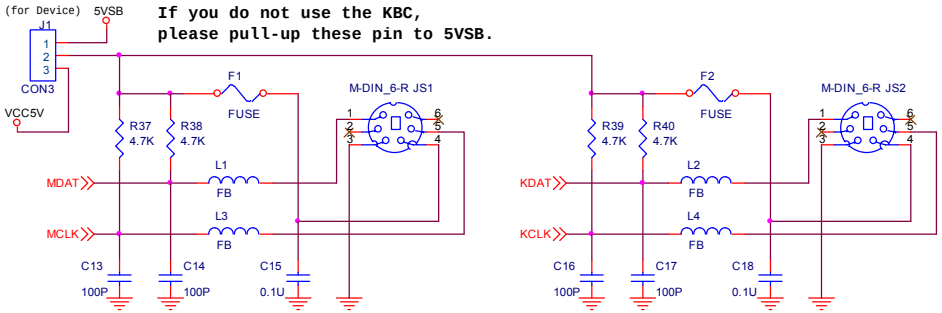


If you do not use the UART port 1, please pull-up these pin to VCC3V.



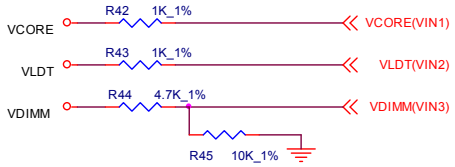
RING-IN Wake-up is supported by F71808.

If you do not use the KBC, please pull-up these pin to 5VSB.



PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

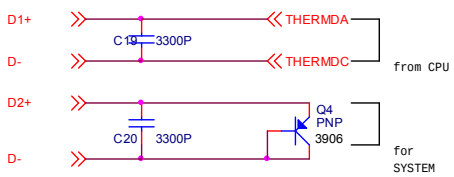
Size	Document Number	Rev
Custom	UART PS/2 KBC	0.8
Date: Thursday, June 24, 2010	Sheet 2 of 9	



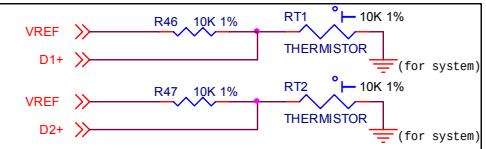
VDIMM Input Level Must > 1V

***VIN1 VIN2 VIN3 internal pull-down 320K ohm @AMD mode**

VOLTAGE SENSING.

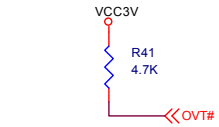


DIODE SENSING CIRCUIT

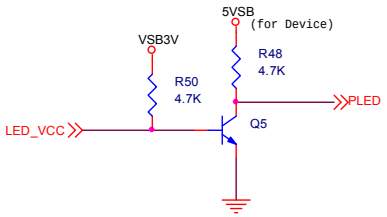


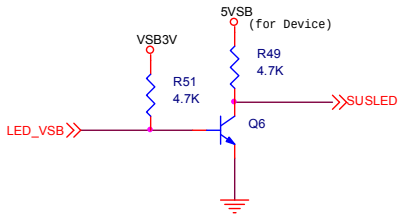
THERMISTOR SENSING CIRCUIT

Temperature Sensing

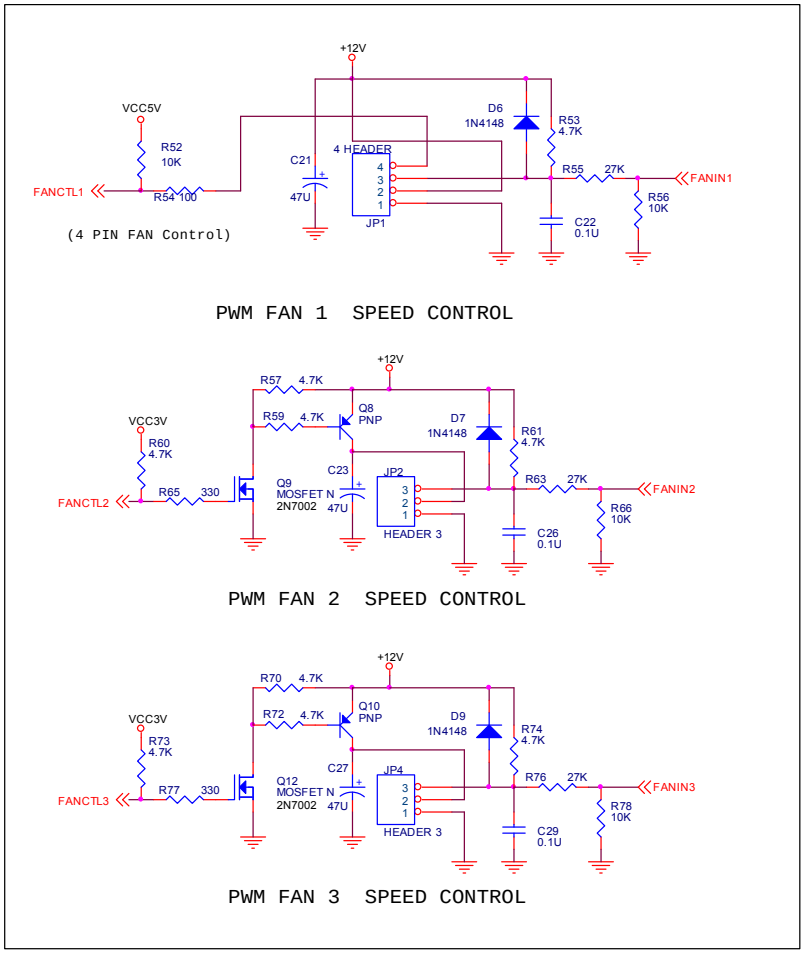


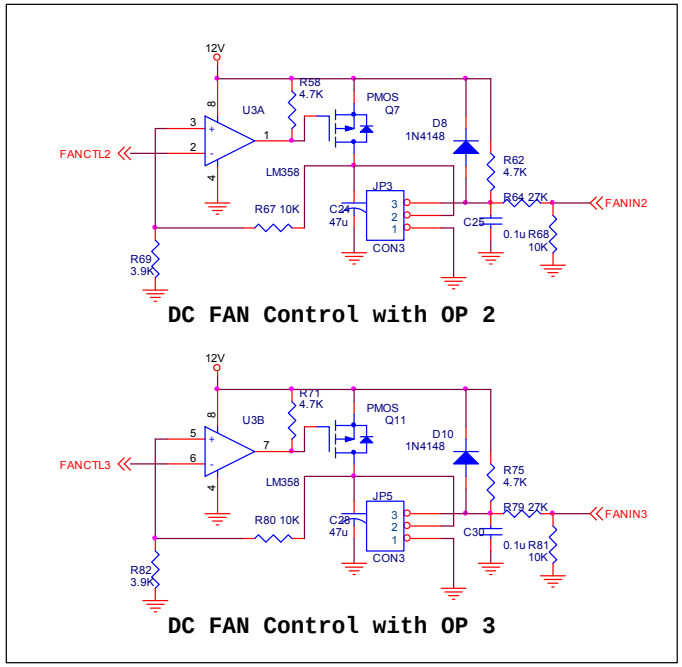
OVT Pull-up





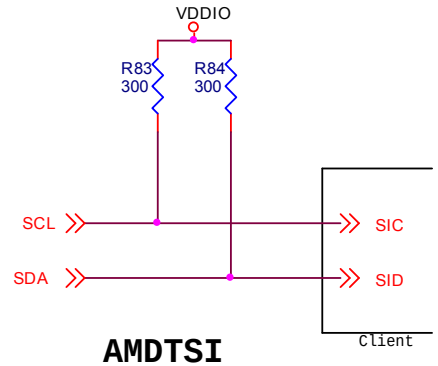
Size	Document Number	Rev
Custom	H/W MONITOR	0.8
Date: Thursday, June 24, 2010	Sheet 3 of 9	



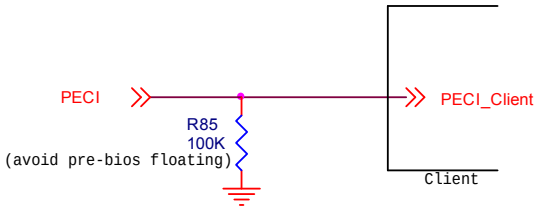


FAN CONTROL FOR PWM OR DC

Size	Document Number	Rev
Custom	FAN CONTROL	0.8
Date: Thursday, June 24, 2010	Sheet 4 of 9	



AMDTSI



INTEL PECI

Power Sequence Pull-up

Size	Document Number	Rev
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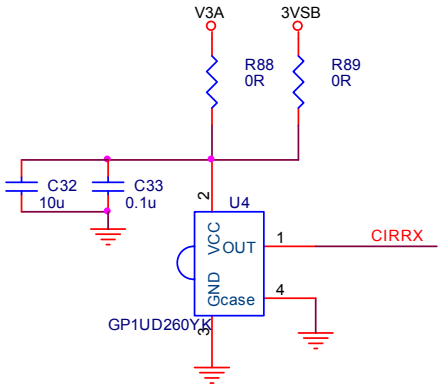
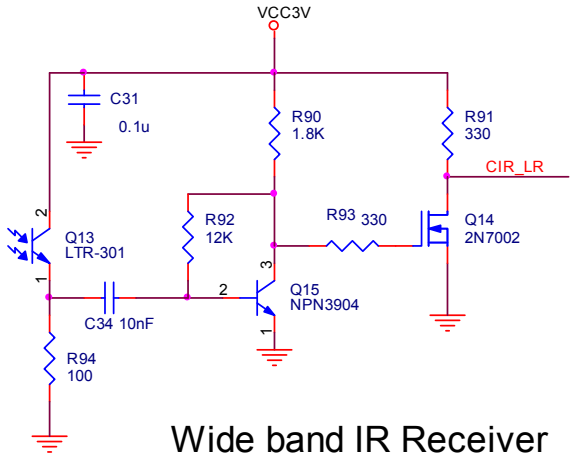
Date: Thursday, June 24, 2010	Sheet 5 of 9	

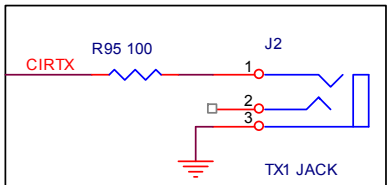


Long Rang IR Receiver

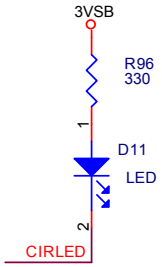
choose power and capacitance by IR receiver



Wide band IR Receiver



TX PORT



IR LED

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A	CIR	0.8
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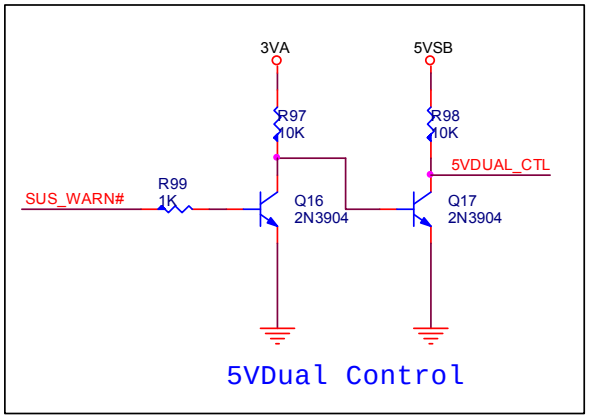
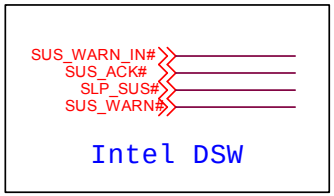
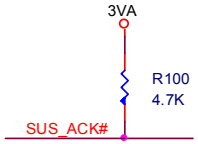
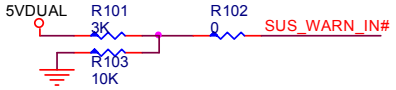
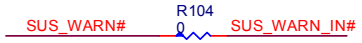








SUS_WARN DETECT MODE1



SUS_WARN DETECT MODE2

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A	Intel DSW	0.8
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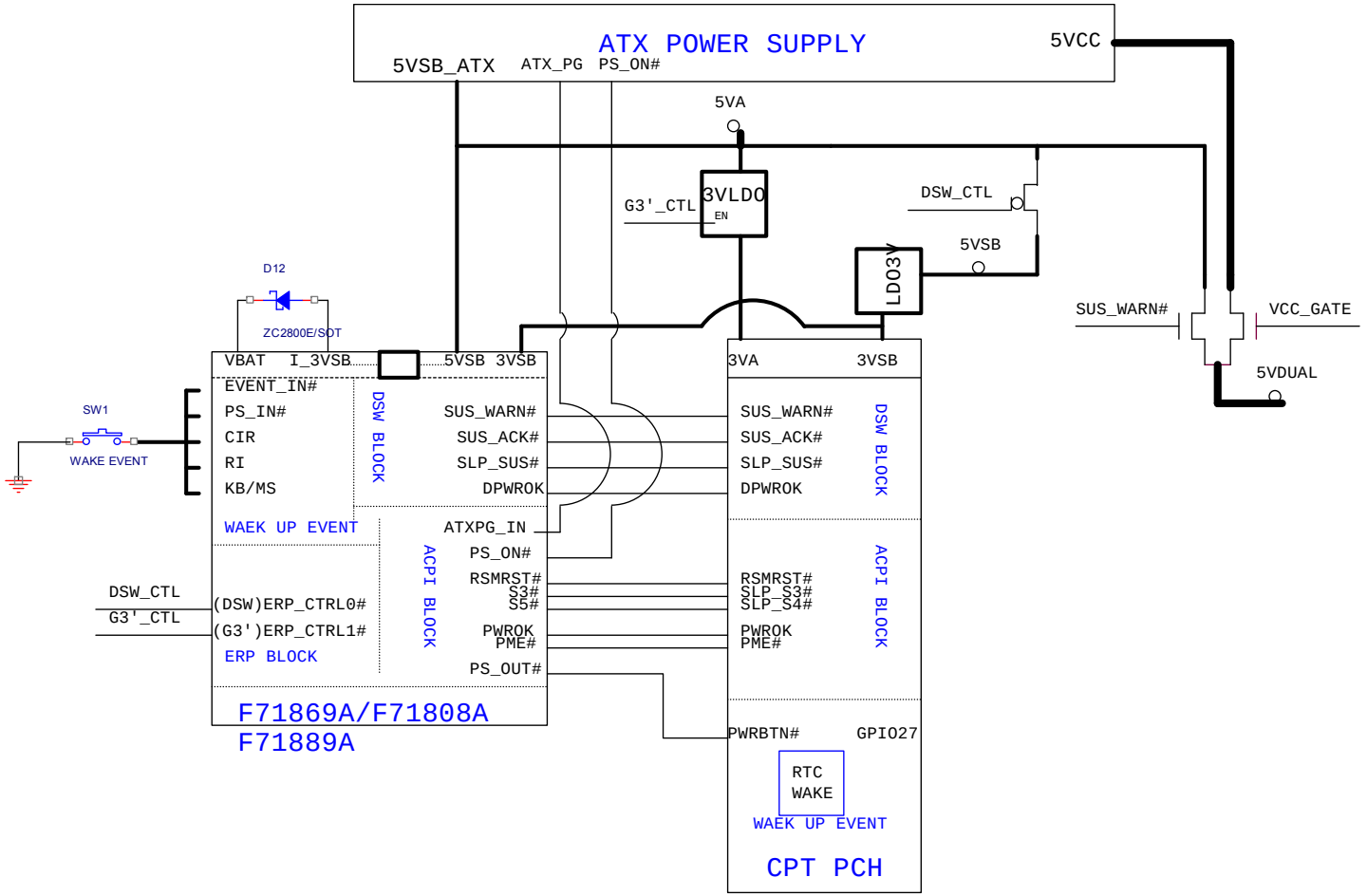

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B	DSW Diagram	0.8
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Version	Content
0.5	2010.5.14 Add DSW multi-fucntion on Pin19, 45, 49
0.6	2010.6.18 Add multi-fucntion on Pin23 pin57(STRAP_PWOK) circuit pin30(S5#) connects S4#(chipset)
0.7	2010.6.22 Remove SUS_ACK# multi-fucntion on Pin19
0.8	2010.6.24 Notice R11 and D4 default is NC.

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A	Revision History	0.8
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