



UTT150N03

Preliminary

Power MOSFET

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

DESCRIPTION

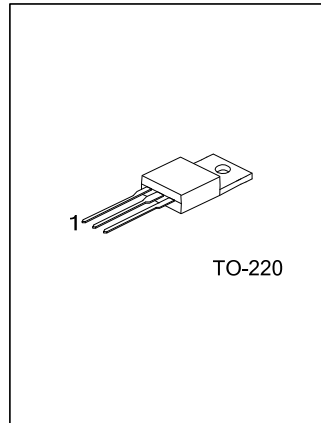
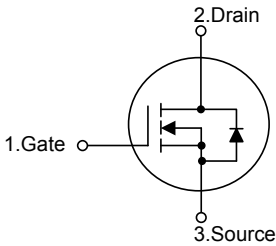
The UTC UTT150N03 is a N-channel power MOSFET, using UTC's advanced trench technology to provide customers with a minimum on-state resistance, low gate charge and superior switching performance.

The UTC UTT150N03 is generally applied in DC to DC convertor, synchronous or conventional switching PWM controllers.

FEATURES

- \* 150A, 30V,  $R_{DS(ON)}=4.1m\Omega @ V_{GS}=10V, I_D = 75A$
- $R_{DS(ON)}=4.6m\Omega @ V_{GS}=4.5V, I_D = 75A$
- \* High Switching Speed
- \* High Power and Current Handling Capability
- \* RoHS Compliant

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UTT150N03L-TA3-T	UTT150N03G-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UTT150N03L-TA3-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) TA3: TO-220
	(3)Lead Free	(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	30	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	150	A
	Pulsed	$I_{DM}$	266	A
Single Pulsed Avalanche Energy (Note 2)		$E_{AS}$	300	mJ
Power Dissipation	Power Dissipation	$P_D$	160	W
	Derate above $25^{\circ}\text{C}$		1.07	$\text{W}/^{\circ}\text{C}$
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature		$T_{STG}$	-55~+150	$^{\circ}\text{C}$

註解 [U1]: 设计人员根据曲线图得到的 (pulse width=300us)

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	0.94	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			1	μA
Gate- Source Leakage Current	Forward	I <sub>GSS</sub>			+100	nA
	Reverse				-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1		3	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =75A		3.4	4.1	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =75A		4.0	4.6	
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1.0MHz		5200		pF
Output Capacitance	C <sub>OSS</sub>			970		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			570		pF
<b>SWITCHING PARAMETERS</b>						
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0.5V, f=1MHz		2.1		Ω
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> =0~10V, V <sub>DD</sub> =15V, I <sub>D</sub> =75A, I <sub>G</sub> =1mA		106	132	nC
	Q <sub>G(5)</sub>	V <sub>GS</sub> =0~5V, V <sub>DD</sub> =15V, I <sub>D</sub> =75A, I <sub>G</sub> =1mA		56	69	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> =0~1V, V <sub>DD</sub> =15V, I <sub>D</sub> =75A, I <sub>G</sub> =1mA		5.0	6.5	nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =75A, I <sub>G</sub> =1mA		15		nC
Gate Charge Threshold to Plateau	Q <sub>GS2</sub>			10		nC
Gate to Drain Charge	Q <sub>GD</sub>			23		nC
Turn-ON Time	t <sub>ON</sub>				168	ns
Turn-ON Delay Time	t <sub>D(ON)</sub>			11		ns
Rise Time	t <sub>R</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =75A, V <sub>GS</sub> =4.5V, R <sub>GS</sub> =3.3Ω		105		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>		70		ns	
Fall-Time	t <sub>F</sub>		46		ns	
Turn-OFF Time	t <sub>OFF</sub>			173	ns	
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =150A			1.25	V
		I <sub>S</sub> =15A			1.0	V
Body Diode Reverse Recovery Time	t <sub>RR</sub>	I <sub>SD</sub> =150A, dI <sub>SD</sub> /dt=100A/μs			37	ns
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>				21	nC

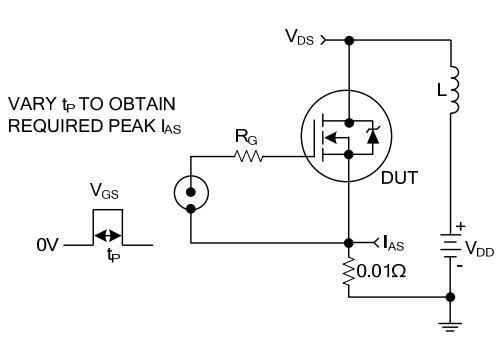
Notes: 1. Package current limitation is 80A.

2. Starting T<sub>J</sub> = 25°C, L = 0.15mH, I<sub>AS</sub> = 64A, V<sub>DD</sub> = 27V, V<sub>GS</sub>=10V

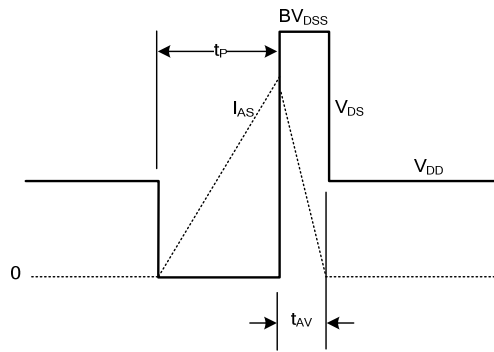
3. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%



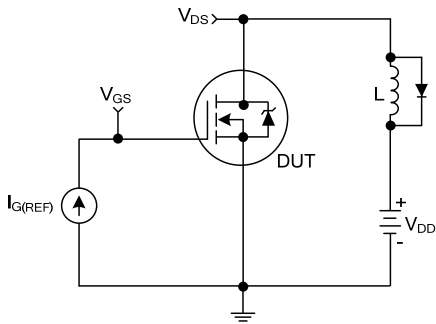
■ TEST CIRCUITS AND WAVEFORMS



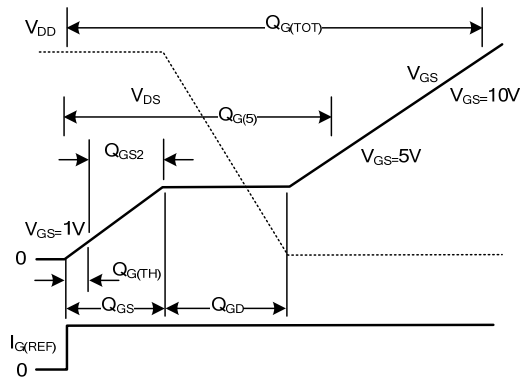
Unclamped Energy Test Circuit



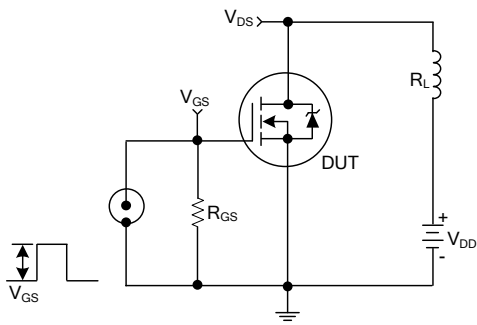
Unclamped Energy Waveforms



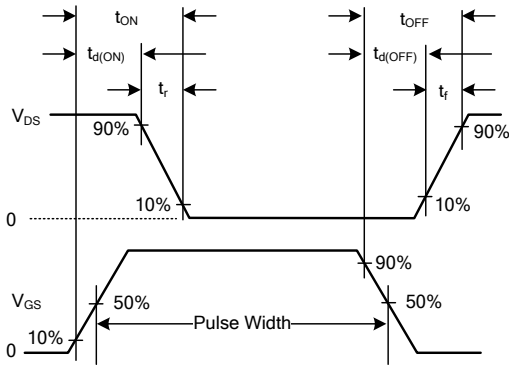
Gate Charge Test Circuit



Gate Charge Waveforms



Switching Time Test Circuit



Switching Time Waveforms



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