

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74VHC125F,TC74VHC125FT,TC74VHC125FK TC74VHC126F,TC74VHC126FT,TC74VHC126FK

TC74VHC125F/FT/FK Quad Bus Buffer  
TC74VHC126F/FT/FK Quad Bus Buffer

The TC74VHC125/126 are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Shottky TTL while maintaining the CMOS low power dissipation.

The TC74VHC125 requires the 3-state control input  $\bar{G}$  to be set high to place the output into the high impedance state, whereas the TC74VHC126 requires the control input G to be set low to place the output into high impedance.

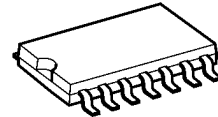
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up.

This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

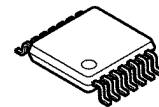
- High speed:  $t_{pd} = 3.8 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC (opr)} = 2 \text{ to } 5.5 \text{ V}$
- Low noise:  $V_{OLP} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74ALS125/126

TC74VHC125F, TC74VHC126F



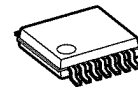
SOP14-P-300-1.27A

TC74VHC125FT, TC74VHC126FT



TSSOP14-P-0044-0.65A

TC74VHC125FK, TC74VHC126FK

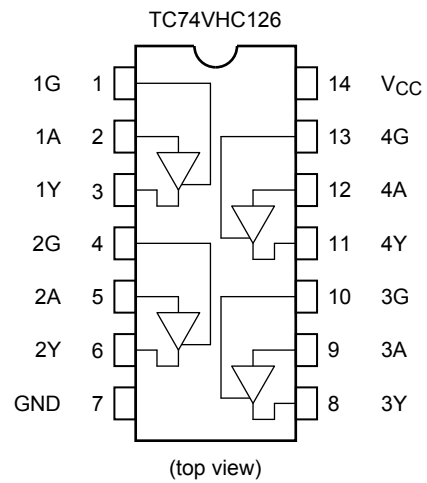
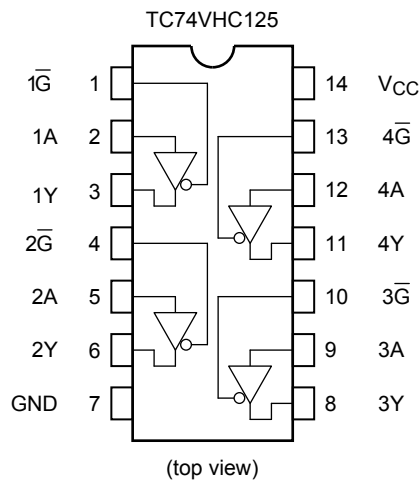


VSSOP14-P-0030-0.50

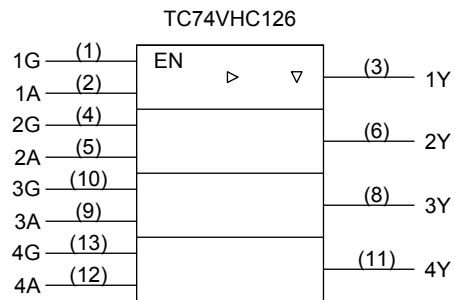
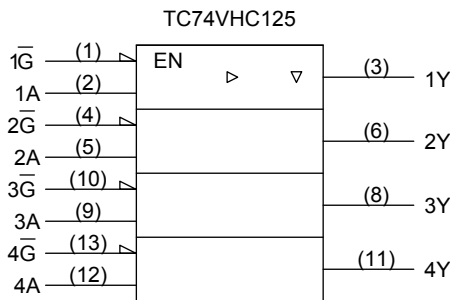
### Weight

SOP14-P-300-1.27A : 0.18 g (typ.)  
TSSOP14-P-0044-0.65A : 0.06 g (typ.)  
VSSOP14-P-0030-0.50 : 0.02 g (typ.)

## Pin Assignment



## IEC Logic Symbol



## Truth Table

**TC74VHC125**

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care

Z: High impedance

**TC74VHC126**

Inputs		Output
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't care

Z: High impedance

## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dv	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—	2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V	
Low-level input voltage	V <sub>IL</sub>	—	2.0 3.0 to 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA	

## AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	5.6	8.0	1.0	9.5	ns
				50	—	8.1	11.5	1.0	13.0	
	5.0 ± 0.5		15	—	3.8	5.5	1.0	6.5		
			50	—	5.3	7.5	1.0	8.5		
Output enable time	t <sub>pZL</sub>	R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	15	—	5.4	8.0	1.0	9.5	ns
				50	—	7.9	11.5	1.0	13.0	
	5.0 ± 0.5		15	—	3.6	5.1	1.0	6.0		
			50	—	5.1	7.1	1.0	8.0		
Output disable time	t <sub>pLZ</sub>	R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	50	—	9.5	13.2	1.0	15.0	ns
			5.0 ± 0.5	50	—	6.1	8.8	1.0	10.0	
Output to output skew	t <sub>osLH</sub>	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
	t <sub>osHL</sub>		5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C <sub>IN</sub>	—		—	4	10	—	10	pF	
Output capacitance	C <sub>OUT</sub>	—		—	6	—	—	—	pF	
Power dissipation capacitance (Note 2)	C <sub>PD</sub>	TC74VHC125		—	14	—	—	—	pF	
		TC74VHC126		—	15	—	—	—		

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

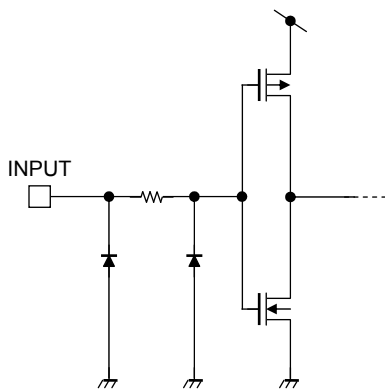
Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

## Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.3	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.3	-0.8	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

**Input Equivalent Circuit**

## Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

**Package Dimensions**

TSSOP14-P-0044-0.65A

Unit: mm



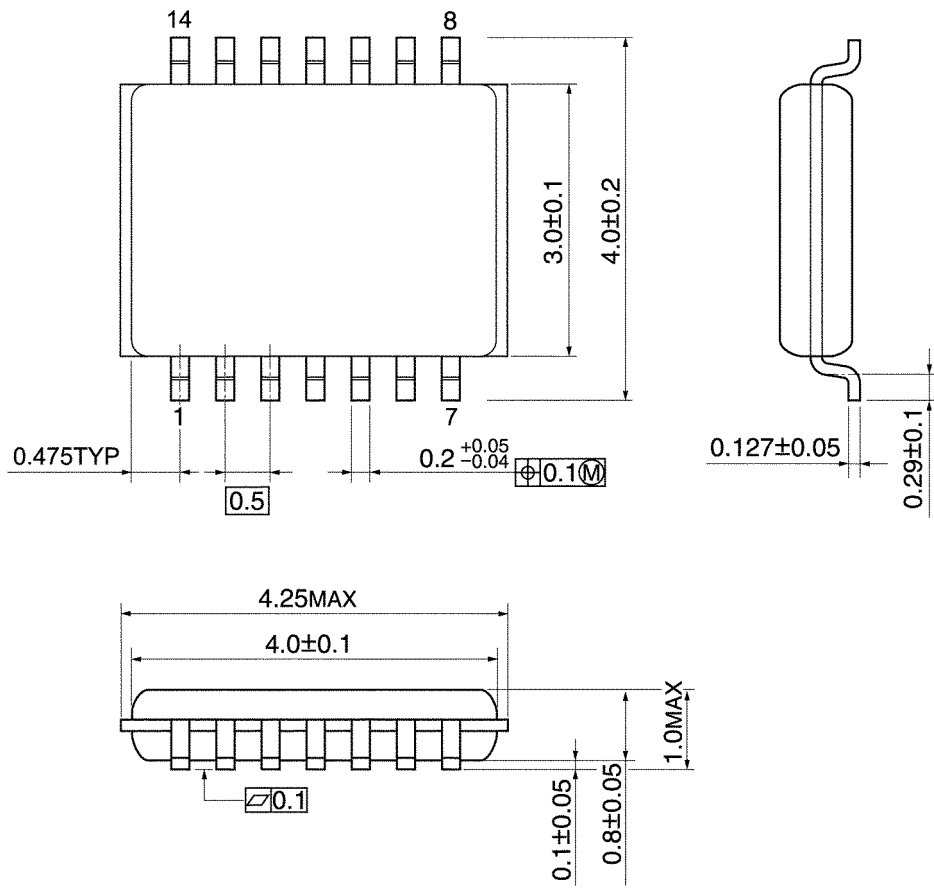
Weight: 0.06 g (typ.)



**Package Dimensions**

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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