5/13/2004

# *Errata: CS8416 Rev. D*

Rev. D Silicon (Reference CS8416 Datasheet revision DS578PP4)

- Parts with a manufacturing date code of 0415 or after will not output a proper clock on RMCK when the RMCK output frequency is set to be 128*Fs. Parts with a manufacturing date code before 0415 will output a proper clock on RMCK when the RMCK output frequency is set to be 128*Fs. All parts will output a proper clock on RMCK when the RMCK output frequency is set to be 256*Fs.

  This problem will be corrected and operate properly in rev E.

- When OMCK System Clock Mode is enabled (SWCLK=1b) and the differential XLR or single ended RCA cable has been plugged and unplugged from the receiver input multiple times, the clock output on the RMCK pin may not properly switch over from the recovered master clock to the OMCK clock when the receiver PLL is unlocked. OLRCK and OSCLK are always divided from the clock output on the RMCK pin.

  If the receiver inputs are always left connected, only unplugged during power down, or connected using an optical connector, OMCK System Clock Mode will function correctly.

  If the application requires the receiver inputs to be rapidly plugged and unplugged multiple times and OMCK System Clock Mode is required, there is a software mode workaround. The user can monitor the UNLOCK bit in the Receiver Error register (0Ch) either by polling or by using the interrupt function. When UNLOCK=1b, the user should set the FSWCLK bit in the Control0 register (00h) to 1b. When UNLOCK=0b, the user should set the FSWCLK bit in the Control0 register (00h) to 0b. There is no workaround for hardware mode.

  This problem will be corrected and operate properly in rev E.

## Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to www.cirrus.com