TOSHIBA Original CMOS 8-Bit Microcontroller

TLCS-870 Series

TMP87PM29UG
TMP87PM29NG

Not Recommended for New Design

TOSHIBA CORPORATION
Semiconductor Company

Revision History

Date	Revision	
2003/3/20	1	First Release
2008/3/06	2	Contents Revised
2008/9/30	3	Contents Revised

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Caution in Setting the UART Noise Rejection Time

When UART is used, settings of RXDNC are limited depending on the transfer clock specified by BRG. The combination "O" is available but please do not select the combination "–".

The transfer clock generated by timer/counter interrupt is calculated by the following equation :

Transfer clock [Hz] = Timer/counter source clock [Hz] ÷ TTREG set value

BRG setting	Transfer clock [Hz]	RXDNC setting			
		00 (No noise rejection)	01 (Reject pulses shorter than 31/fc[s] as noise)	10 (Reject pulses shorter than 63/fc[s] as noise)	11 (Reject pulses shorter than 127/fc[s] as noise)
000	fc/13	O	O	O	–
110 (When the transfer clock generated by timer/counter interrupt is the same as the right side column)	fc/8	O	–	–	–
	fc/16	O	O	–	–
	fc/32	O	O	O	–
The setting except the above		O	O	O	O

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Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

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1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP87PM29N	P-SDIP64-750-1.78	TMP87PM29NG	SDIP64-P-750-1.78	—
TMP87PM29U	P-LQFP64-1010-0.50D	TMP87PM29UG	LQFP64-P-1010-0.50D	—

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

The publication date of this datasheet is printed at the lower right corner of this notification.

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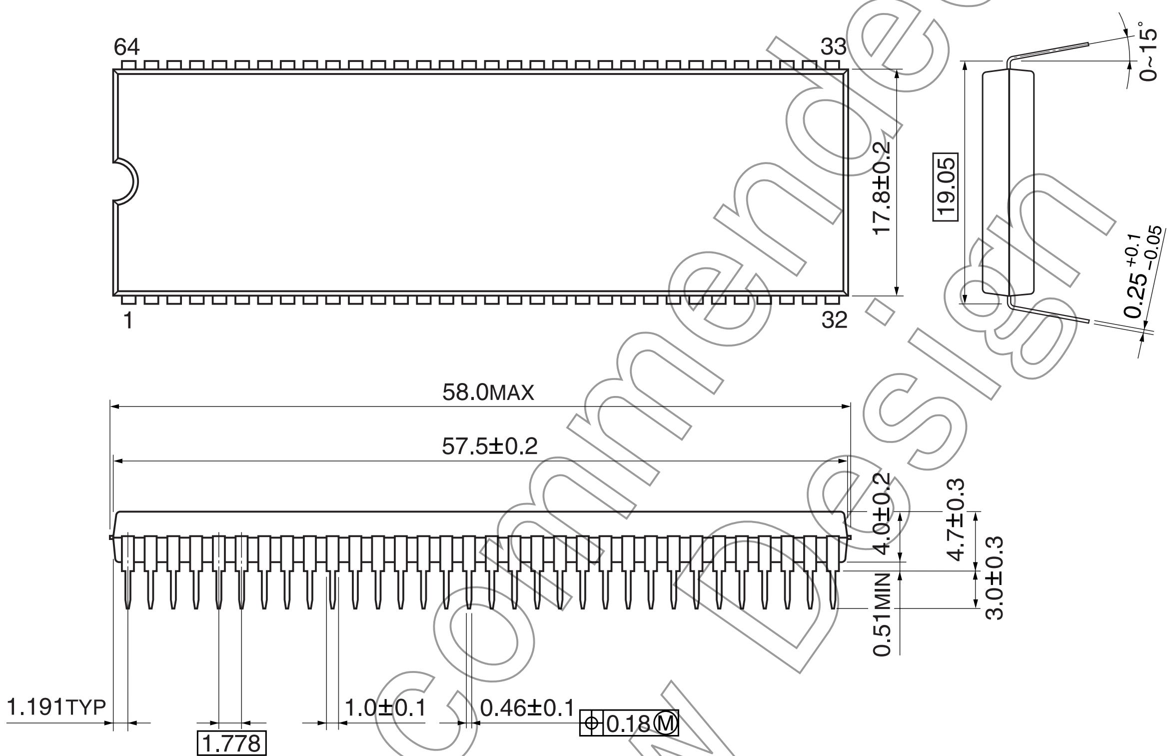
(Annex)

Package Dimensions

SDIP64-P-750-1.78

Unit: mm



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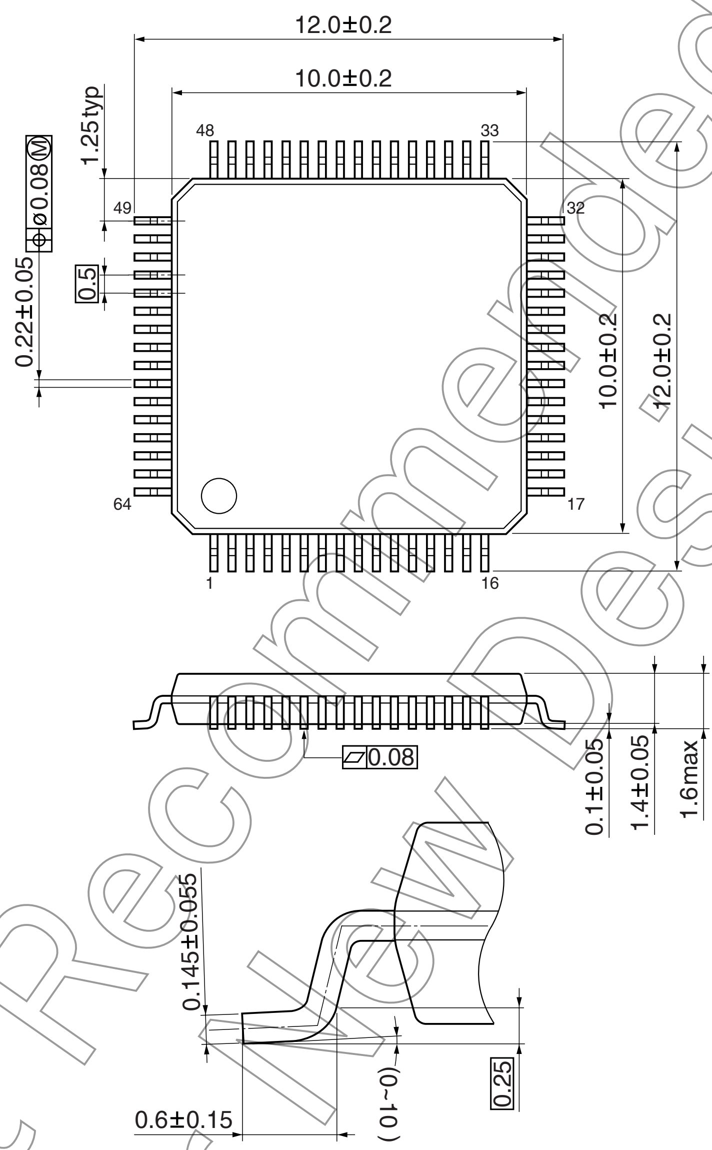
LQFP64-P-1010-0.50D

Unit: mm



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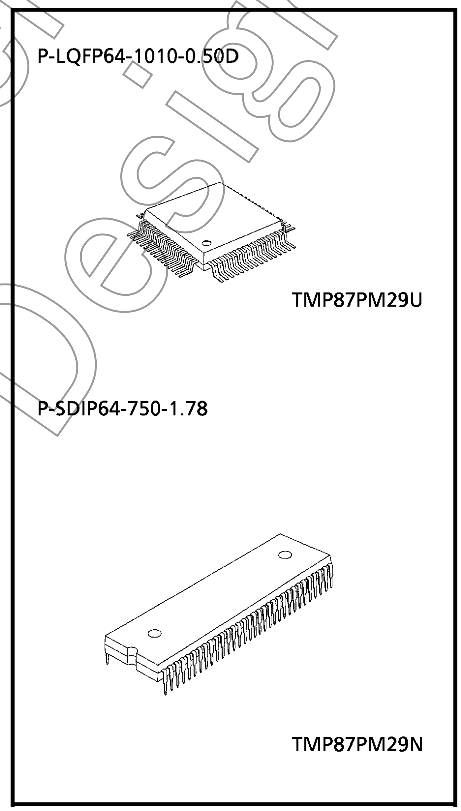
CMOS 8-Bit Microcontroller

TMP87PM29U, TMP87PM29N

The TMP87PM29 is an One-Time PROM microcontroller with low-power 256K bits (32 Kbytes) electrically programmable read only memory for TMP87CH29/CK29/CM29 system evaluation. The TMP87PM29 is pin-compatible with TMP87CH29/CK29/CM29. The operations possible with the TMP87CH29/CK29/CM29 can be performed by writing programs to PROM. The TMP87PM29 can write and verify in the same way as the TC57256AD using an adaptor socket BM11117A/BM11143 and an EPROM programmer.

Part No.	OTP	RAM	Package	Adapter Socket
TMP87PM29U	32 K × 8-bit	1K × 8-bit	P-LQFP64-1010-0.50D	BM11117A
TMP87PM29N			P-SDIP64-750-1.78	BM11143



000707EBP1

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  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
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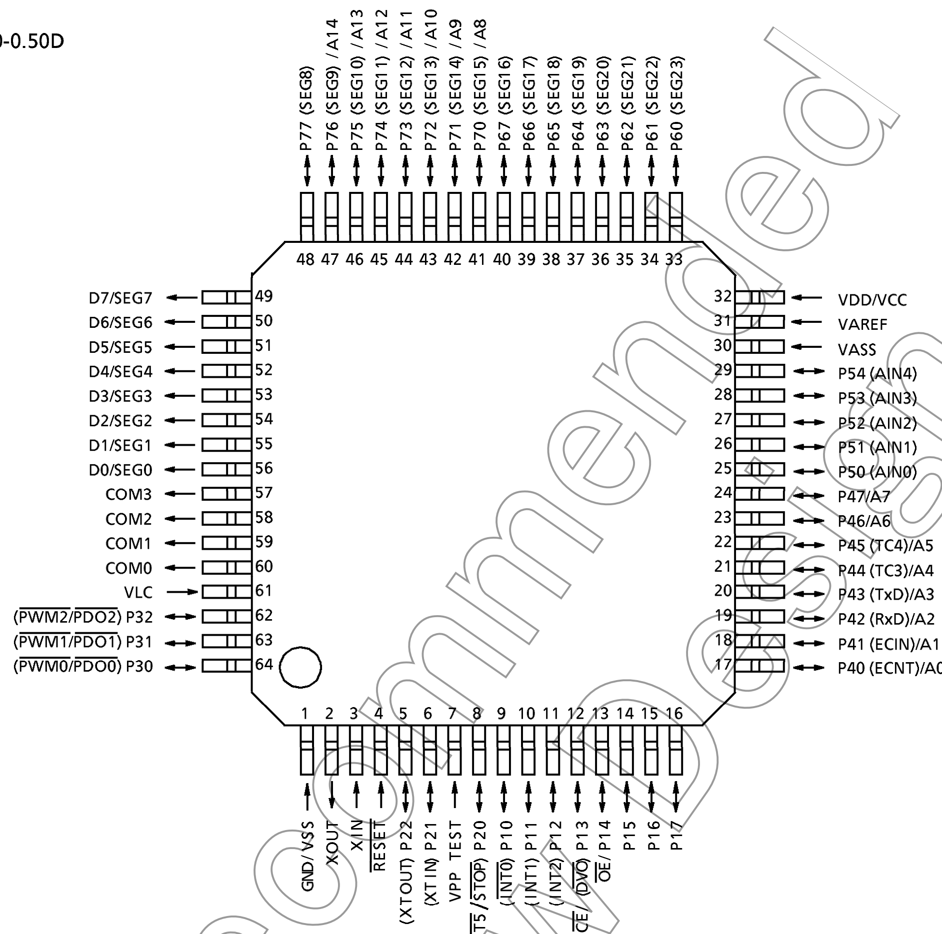
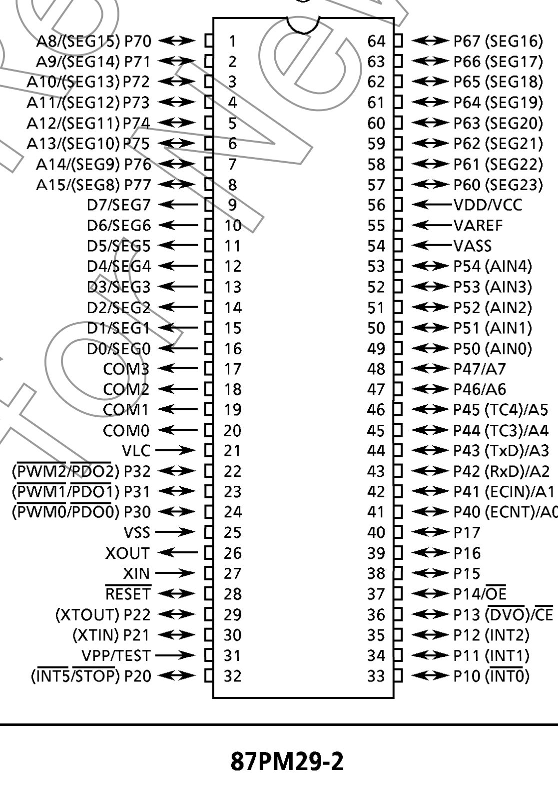
Pin Assignments (Top View)

P-LQFP64-1010-0.50D



P-SDIP64-750-1.78



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Pin Function

The TMP87PM29 has two modes: MCU and PROM.

(1) MCU mode

In this mode, the 87PM29 is pin-compatible with the TMP87CH29/CK29/CM29 (fix the TEST/VPP pin at low level).

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A14 to A8	Input	PROM address inputs	P76 to P70
A7 to A0			P47 to P40
D7 to D0	I/O	PROM data input/outputs	SEG7 to SEG0
$\overline{CE}$	Input	Chip enable signal input (active low)	P13
$\overline{OE}$		Output enable signal input (active low)	P14
VPP	Power supply	+ 12.5 V/5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
GND		0 V	VSS
P32 to P30	I/O	Pull-up with resisteance for input processing.	
P54 to P50			
P67 to P60			
P11		PROM mode setting pins. Fix at high level.	
P21			
P77			
P12, P10		PROM mode setting pins. Fix at low level.	
P17 to P15			
P22, P20			
$\overline{RESET}$			
XIN	Input	Connect an 8 MHz oscillator to stabilize the internal state.	
XOUT	Output		
COM3 to COM0	Output	Open.	
VLC	LCD power supply		
VASS	Power supply	0 V (GND)	
VAREF			

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Operational Description

The following explains the TMP87PM29 hardware configuration and operation. The configuration and functions of the TMP87PM29 are the same as those of the TMP87CH29/CK29/CM29, except in that a one-time PROM is used instead of an on-chip mask ROM.

The TMP87PM29 is placed in the single-clock mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on by executing [SET (SYSCR2). XTEN] instruction at the beginning of the program.

1. Operation Mode

The TMP87PM29 has two modes: MCU and PROM.

1.1 MCU Mode

The MCU mode is activated by fixing the TEST/VPP pin at low level.

In the MCU mode, operation is the same as with the TMP87CH29/CK29/CM29 (the TEST/VPP pin cannot be used open because it has no built-in pull-down resistance).

1.1.1 Program Memory

The TMP87PM29 has a 32K × 8-bit (addresses 8000_H to $FFFF_H$ in the MCU mode, addresses 0000_H to $7FFF_H$ in the PROM mode) of program memory (OTP).

To use the TMP87PM29 as the system evaluation for the TMP87CH29/K29/M29U/N, the program should be written to the program memory area as shown in Figure 1-1.

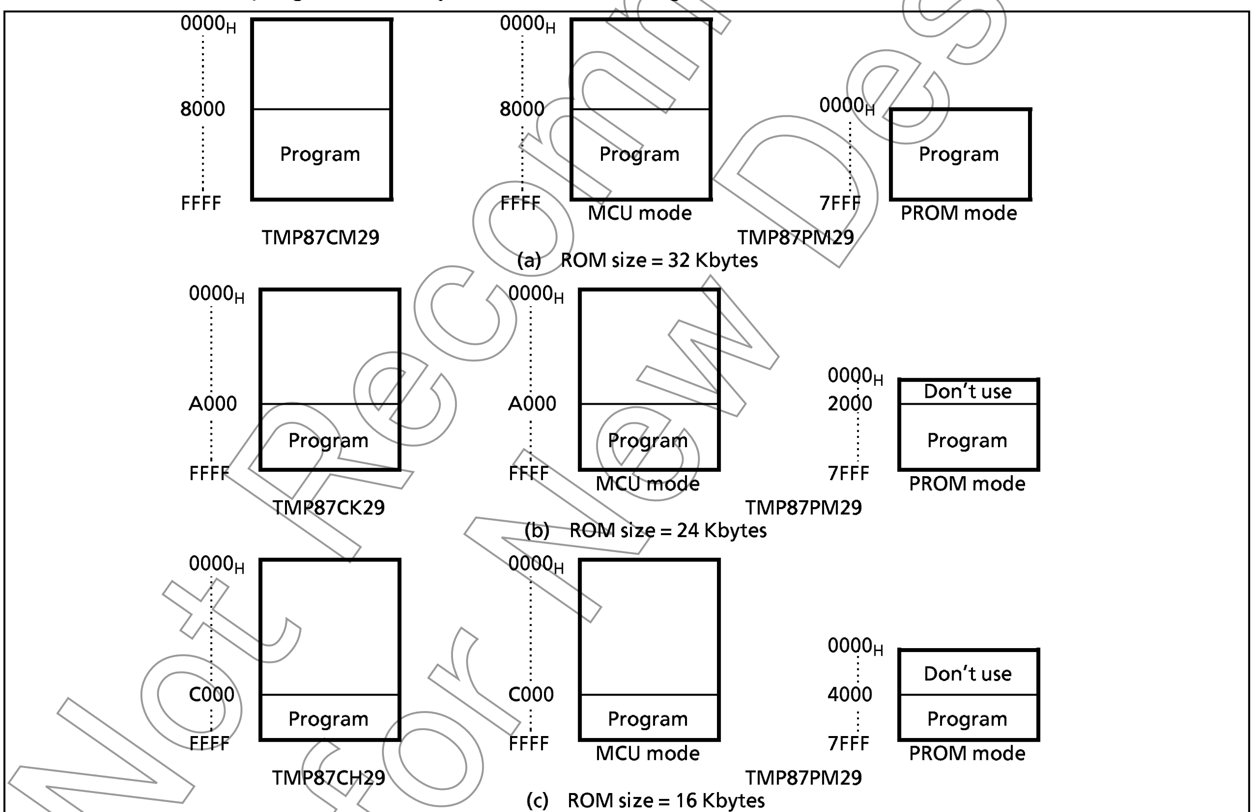


Figure 1-1. Program Memory Area

Note: Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area

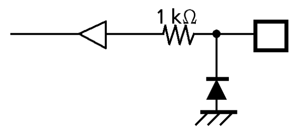
1.1.2 Data Memory

The TMP87PM29 has an on-chip 1K × 8-bit data memory (static RAM).

1.1.3 Input/Output Circuitry

(1) Control pins

The control pins of the TMP87PM29 are the same as those of the TMP87CH29/CK29/CM29 except in that the TEST pin has no built-in pull-down resistance.



Note: TEST pin has no built-in pull-down resistance

Figure 1-2. TEST Pin

(2) I/O ports

The I/O circuitries of the TMP87PM29 I/O ports are the same as circuitries of the TMP87CH29/CK29/CM29.

1.2 PROM Mode

The PROM mode is activated by setting the pins TEST, $\overline{RESET}$ and the ports P17 to P10, P22 to P20 and P77 as shown in Figure 1-3. The PROM mode is used to write and verify programs with a general-purpose PROM programmer.

Note: Please set the high-speed programming mode according to each manual of PROM programmer.

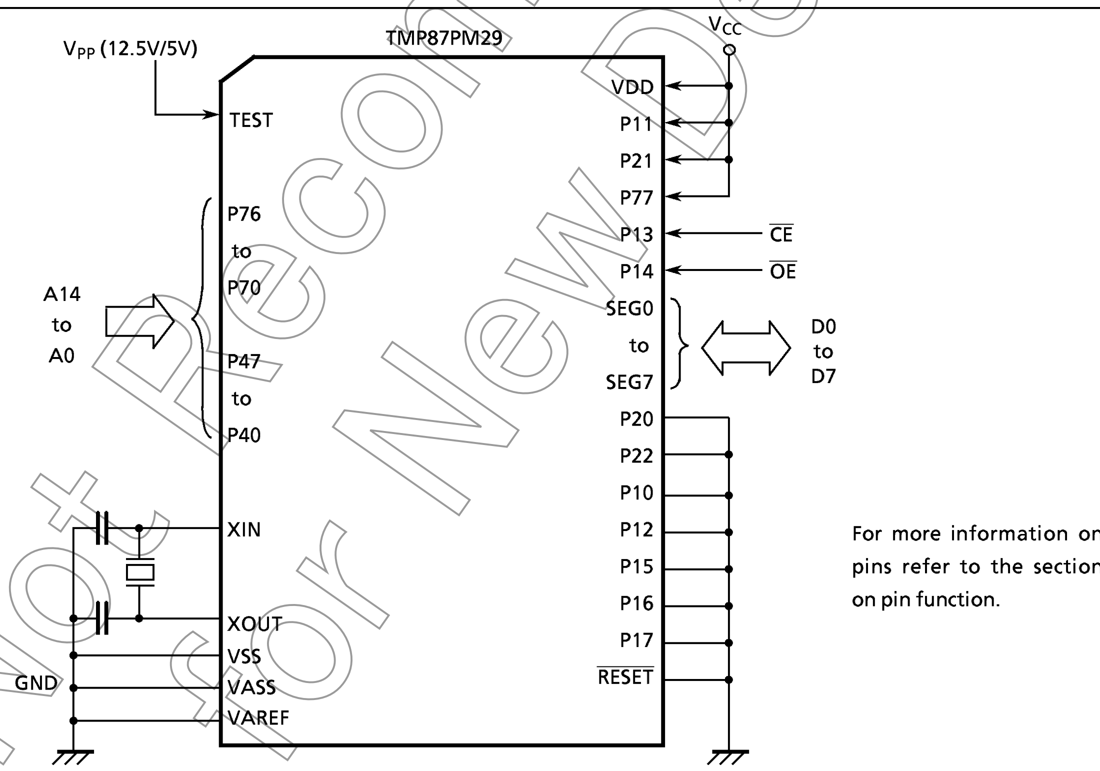


Figure 1-3. Setting for PROM Mode

PROM programmer connection adaptor socket: BM11117A for TMP87PM29U
BM11143 for TMP87PM29N

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1.2.1 Programming Flowchart (High-speed Programming Mode - Ⅰ)

The high-speed programming mode is achieved by applying the program voltage (+12.5V) to the VPP pin when Vcc = 6V. After the address and input data are stable, the data is programmed by applying a single 1ms program pulse to the $\overline{CE}$ input. The programmed data verified. If incorrect, another 1ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. Programming for one address is ended by applying additional program pulse with width 3 times that needed for initial programming (number of programmed times × 1 ms). After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V and verify all addresses.

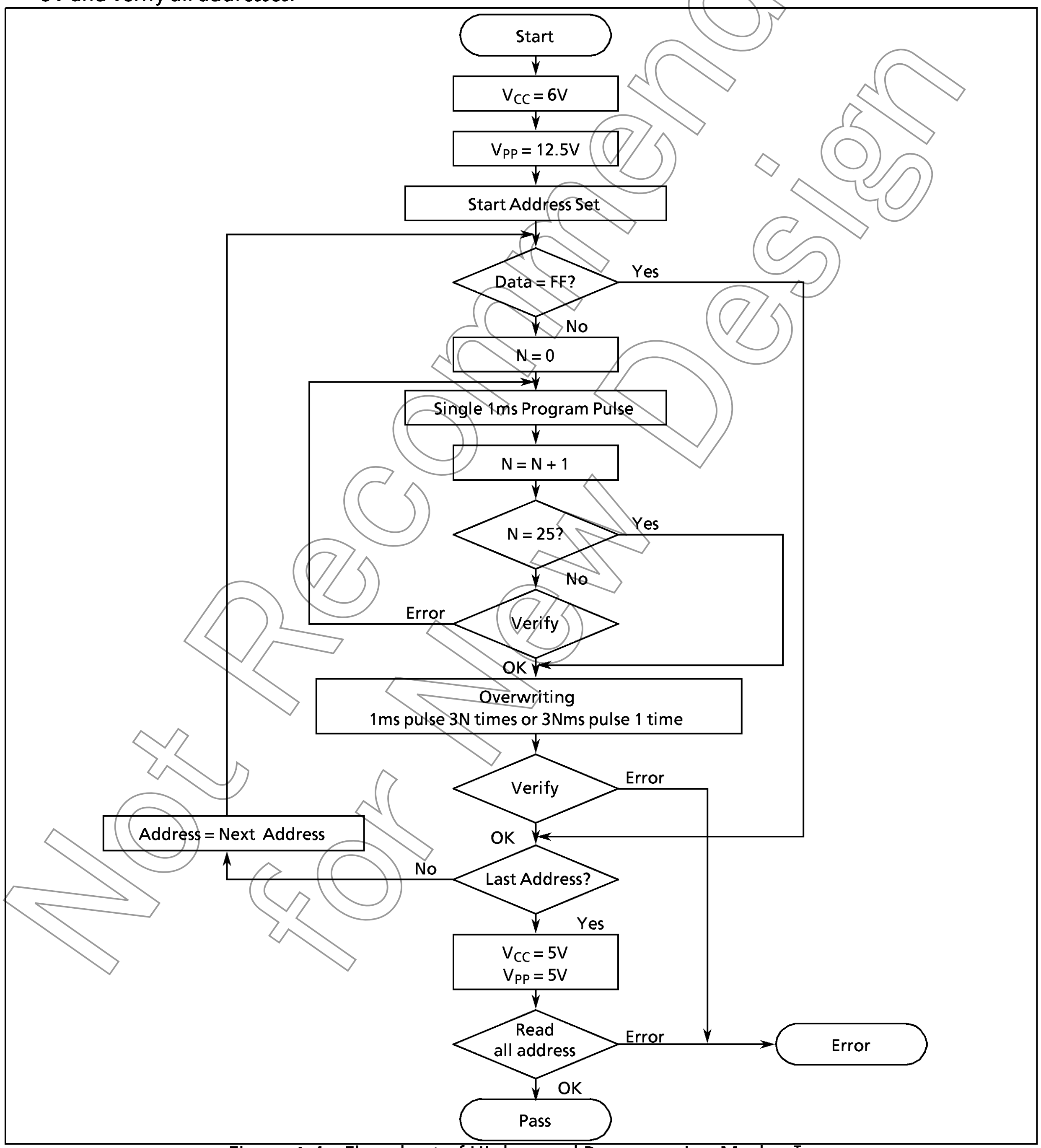

Figure 1-4. Flowchart of High-speed Programming Mode - Ⅰ

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1.2.2 Programming Flowchart (High-speed Programming Mode - II)

The high-speed programming mode is achieved by applying the program voltage (+ 12.75V) to the VPP pin when Vcc = 6.25V. After the address and input data are stable, the data is programmed by applying a single 0.1 ms program pulse to the $\overline{CE}$ input. The programmed data verified. If incorrect, another 0.1 ms program pulse is applied and then the programmed data is verified. This process should be repeated (up to 25 times) until the program operates correctly. After that, change the address and input data, and program as before. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

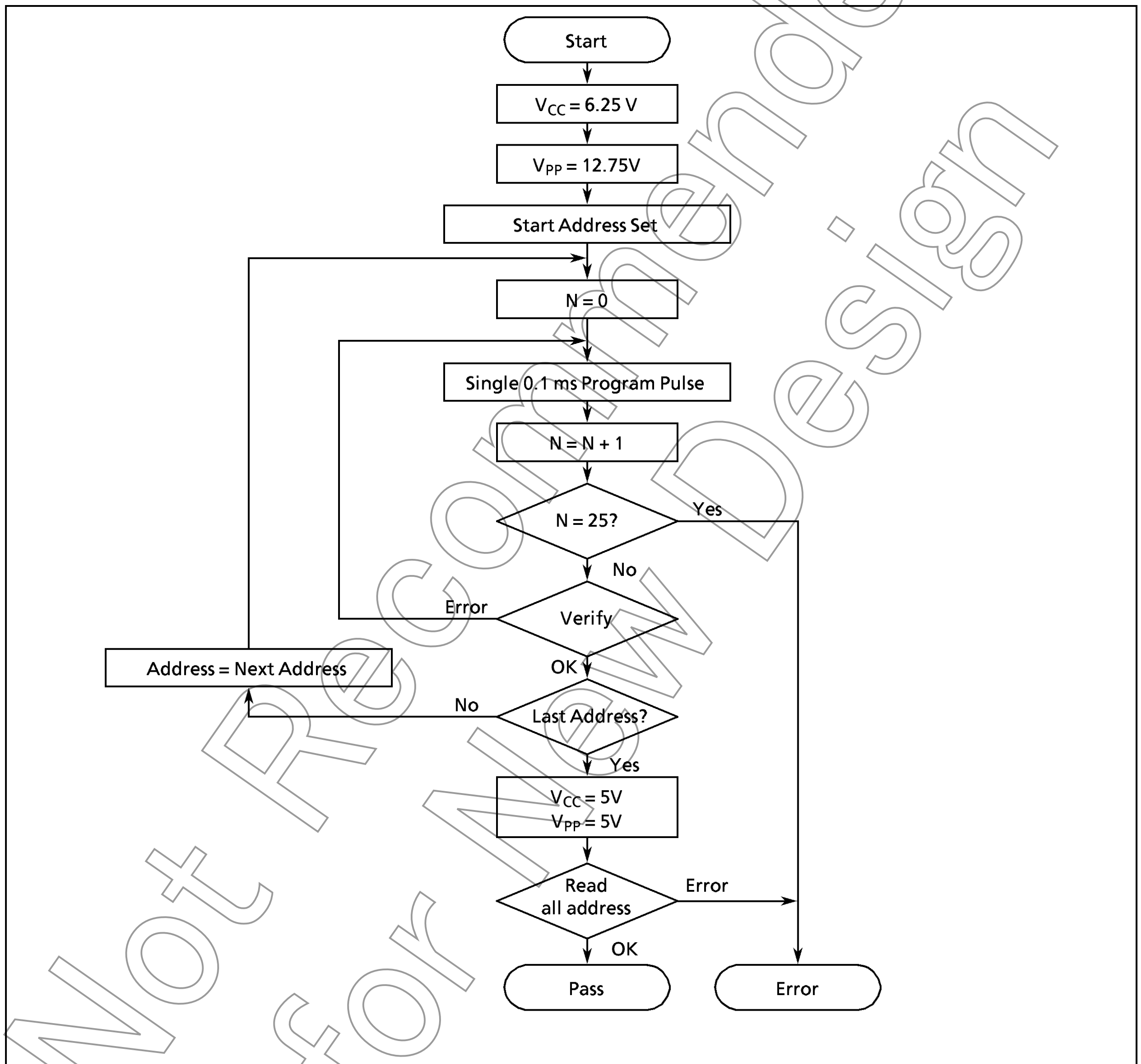

Figure 1-5. Flowchart of High-speed Programming Mode - II

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1.2.3 Writing Method with a General-purpose PROM Program

(1) Adapter
BM11117A: TMP87PM29U
BM11143: TMP87PM29N

(2) Adapter setting
Switch (SW1) is set to side N.

(3) PROM programmer specifying
i) PROM type is specified to TC57256AD.
Writing voltage: 12.5V (high-speed program Ⅰ mode)
12.75V (high-speed program Ⅱ mode)

ii) Data transfer (copy) (note 1)
In the TMP87PM29, EPROM is within addresses 0000 to $7FFF_H$. Data is required to be transferred (copied) to the addresses where it is possible to write. The program area in MCU mode and PROM mode is referred to "Program memory area" in figure 1-1.

Ex. : In the block transfer (copy) mode, executed as below.
ROM capacity of 16 kB: transfer address C000 to $FFFF_H$ to address 4000 to $7FFF_H$

iii) Writing address is specified. (note 1)
Start address: 4000_H
End address: $7FFF_H$

(4) Writing
Writing/Verifying is required to be executed in accordance with PROM programmer operating procedure.

Note 1: The specifying method is referred to the PROM programmer description. Either write the data FF_H to the unused area or set the PROM programmer to access only the program storage area.
Note 2: When MCU is set to an adapter or an adapter is set to PROM programmer, a position of pin 1 must be adjusted. If the setting is reserved, MCU the adapter and PROM program is damaged.
Note 3: The TMP87PM29 does not support, the electric signature mode (hereinafter referred to as "signature"). If the signature is used in PROM program, a device is damaged due to applying 12 V ± 0.5 V to the address pin 9 (A9). The signature must not be used.

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Electrical Characteristics

(2) TMP87PM29

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Program Voltage	V_{PP}	TEST/VPP pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P21, P22, $\overline{\text{RESET}}$, Tri-state port, and Push-pull port	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	P20, port P3 and segment port	– 0.3 to 5.5	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1,P2,P4,P5,P6,P7	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	ΣI_{OUT1}	Ports P1,P2,P4,P5,P6,P7	120	mA
	ΣI_{OUT2}	Port P3	60	
Power Dissipation [Topr = 70°C]	PD	TMP87PM29N	600	mW
		TMP87PM29U	350	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: The supply voltage range of the conditions shows the value in NORMAL 1, 2 modes and IDLE 1, 2 modes.

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DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			—	0.9	—	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V/0 V		—	—	± 2	μA
	I_{IN2}	Sink open drain port and tri-state port						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Low Current	I_{IL}	Push-pull port	V_{DD} = 5.5 V, V_{IN} = 0.4 V		—	—	– 2	mA
Input Resistance	R_{IN}	$\overline{RESET}$			100	220	450	kΩ
Output Leakage Current	I_{LO}	Sink open drain port and tri-state port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		—	—	2	μA
Output High Voltage	V_{OH1}	Push-pull port	V_{DD} = 4.5 V, I_{OH} = – 200 μA		2.4	—	—	V
	V_{OH2}	Tri- state port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA		4.1	—	—	
Output Low Voltage	V_{OL}	Except XOUT and port P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		—	—	0.4	V
Output Low Current	I_{OL}	Only P30, P31, P32	V_{DD} = 4.5 V, V_{OL} = 1.0 V		—	20	—	mA
Supply Current in NORMAL 1 , 2 mode	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V/0.2 V		—	10	16	mA
Supply Current in IDLE 1, 2 mode					—	4.5	6	mA
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V/0.2 V LCD driver is not enable		—	30	60	μA
Supply Current in SLEEP mode					—	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V		—	0.5	10	μA
Segment Output Low Resistance	R_{OS1}	SEG23 to SEG0 pins	V_{DD} = 5 V V_{DD} – V_{LC} = 3 V	RESL = 0 (Note 11)	—	20	—	kΩ
				RSEL = 1		7		
Common Output Low Resistance	R_{OC1}	COM3 to COM0 pins		RESL = 0		20		
				RSEL = 1		7		
Segment Output High Resistance	R_{OS2}	SEG23 to SEG0 pins		RESL = 0		200		
				RSEL = 1		70		
Common Output High Resistance	R_{OC2}	COM3 to COM0 pins		RESL = 0		200		
				RSEL = 1		70		
Segment /Common Output Voltage	$V_{O\ 2/3}$	SEG23 to SEG0 and COM3 to COM0 pins			3.8	4.0	4.2	V
	$V_{O\ 1/2}$				3.3	3.5	3.7	
	$V_{O\ 1/3}$				2.8	3.0	3.2	

Note 1: Typical value show those at T_{opr} = 25°C , V_{DD} = 5 V.
Note 2: Input Current ; The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} ; Except for I_{REF}
Note 4: Output resistors R_{OS}, R_{OC} indicate "on" when switching levels.
Note 5: $V_{O2/3}$ indicates an output current at the 2/3 level when operating in the 1/4 or 1/3 duty mode.
Note 6: $V_{O1/2}$ indicates an output current at the 1/2 level when operating in the 1/2 duty or static mode.
Note 7: $V_{O1/3}$ indicates an output current at the 1/3 level when operating in the 1/4 or 1/3 duty mode.
Note 8: When you use a liquid crystal display (LCD), it is necessary to give careful consideration to the value of the output resistor $R_{OS\ 1/2}$, $R_{OC\ 1/2}$.
Note 9: R_{OS1}, R_{OC1}: On time of the lower output resistor is 2^7/fc, 1/(2·fs) [s].
Note 10: R_{OS2}, R_{OC2}: On time of the higher output resistor is 1/(n·f_F). (1/n duty, f_F: frame frequency)
Note 11: RSEL ; Bit 6 in LCDCR

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AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7 V, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
			–	–	± 2	

Note: Quantizing error is not contained in those errors.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL 1, 2 mode	0.5	–	10	μs
		In IDLE 1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

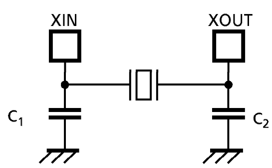
(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
TC1 Input (ECIN Input)	t_{TC1}	Frequency medsurement mode V_{DD} = 4.5 to 5.5 V	Single edge count	–	–	8	MHz
			Both edge count	–	–	4	
		Frequency medsurement mode V_{DD} = 2.7 to 5.5 V	Single edge count	–	–	4.2	
			Both edge count	–	–	3	

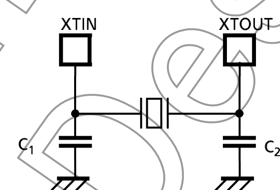
Not Recommended for New Design

Recommended Oscillating Condition (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = − 30 to 70°C)

Parameter	Oscillator	Frequency	Recommended Oscillator		Recommended Condition C_1	Recommended Condition C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30pF	30pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20pF	20pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15pF	15pF



(1) High-frequency



(2) Low-frequency

Note 1: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.
For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html

Not Recommended for New Design

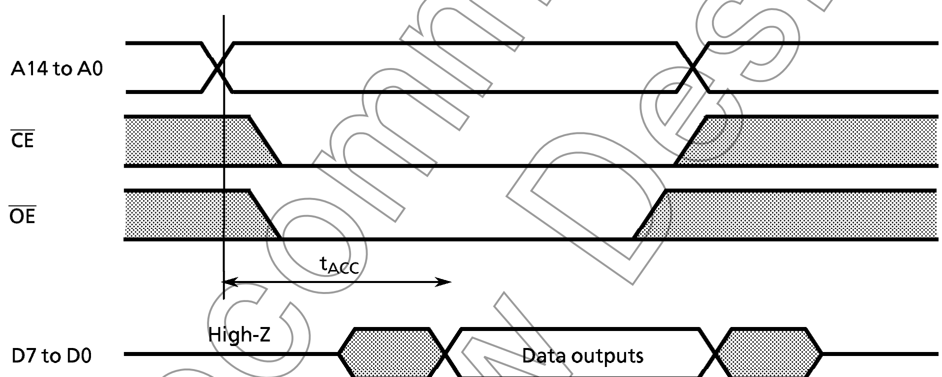
D.C./A.C. Characteristics (PROM mode)

(V_{SS} = 0 V)

(1) Read Operation (Topr = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Program Power Supply Voltage	V_{PP}		$V_{CC} - 0.6$	V_{CC}	$V_{CC} + 0.6$	V
Address Access Time	t_{ACC}	$V_{CC} = 5.0 \pm 0.25$ V	–	1.5 tcyc + 300	–	ns

Note: tcyc = 500 ns at 8 MHz

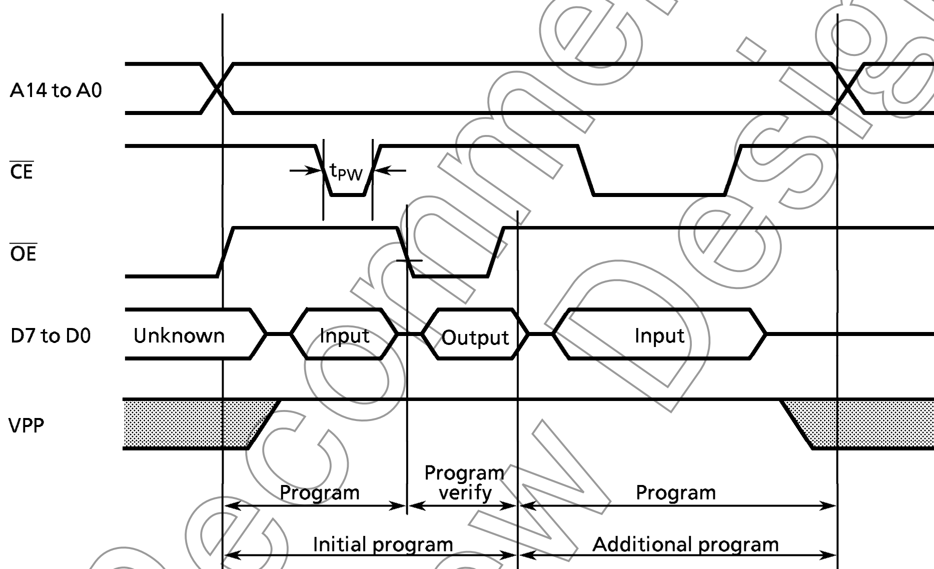


Timing Waveforms of Read Operation

Not Recommended for New Design

(2) High-Speed Programming I Operation (Topr = 25 ± 5°C)

PArameter	Symbol	Condition	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		5.75	6.0	6.25	V
Program Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.0 V, ± 0.25 V V_{PP} = 12.5 ± 0.5 V	0.95	1.0	1.05	ms



Timing Waveforms of Programming Operation

Note 1: Vpp (12.5 V) supply is applied at the same time as Vcc supply or later. It is turned off at the same or earlier.

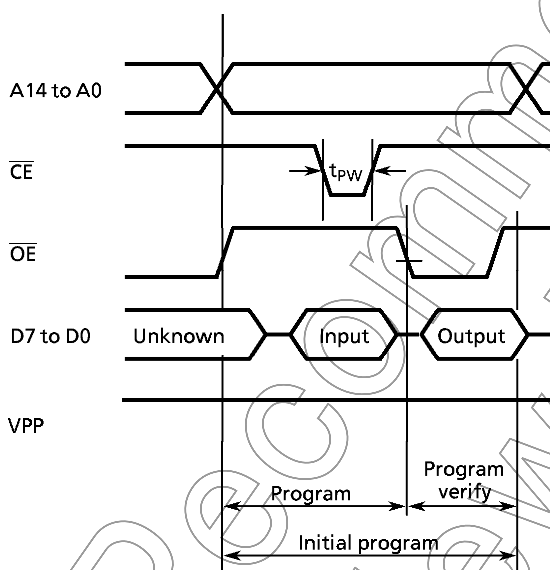
Note 2: When a device is put on or off at VPP = 12.5 V ± 0.5 V, the device may be damaged. Do not put it on or off in programming.

Note3: Use the recommended adapter and mode. When using under other than these conditions, it may be not programmed.

Not Recommended for New Design

(3) High-Speed Programming II Operation (Topr = 25 ± 5°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.12$	V
Power Supply Voltage	V_{CC}		6.00	6.25	6.50	V
Program Power Supply Voltage	V_{PP}		12.50	12.75	13.0	V
Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V	0.095	0.1	0.105	ms



Note 1: Vpp (12.75 V) supply is applied at the same time as Vcc supply or later. It is turned off at the same or earlier.

Note 2: When a device is put on or off at VPP = 12.75 V ± 0.25 V, the device may be damaged. Do not put it on or off in programming.

Note 3: Use the recommended adapter and mode. When using under other than these conditions, it may be not programmed.

Not Recommended for New Design

Not Recommended for New Design