FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11235-1E

MEMORY

CMOS

2 M × 32 BITS HYPER PAGE MODE DRAM MODULE

MB8502E032AA-60/-70

2M × 32 BITS Hyper Page Mode DRAM Module, 5 V, 2-Bank

■ DESCRIPTION

The Fujitsu MB8502E032AA is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of four MB8118165A devices. The MB8502E032AA is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB8502E032AA are the same as the MB8118165A which features hyper page mode operation providing extended valid time for data output and higher speed random access of up to 1,024-bit of data within the same row than the fast page mode. For ease of memory expansion, the MB8502E032AA is offered in a 72-pad Single In-line Memory Module package (SIMM).

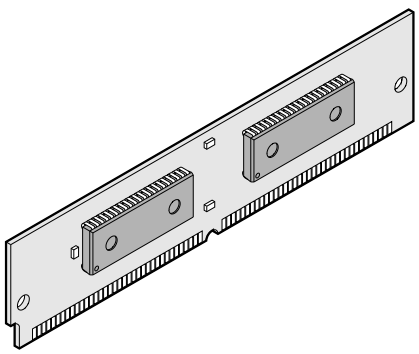
■ PRODUCT LINE & FEATURES

Parameter		MB8502E032AA-60	MB8502E032AA-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		30 ns max.	35 ns max.
$\overline{CAS}$ Access Time		15 ns max.	17 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	1782 mW max.	1672 mW max.
	Hyper Page Mode	1122 mW max.	1012 mW max.
	Standby Mode	44 mW max.	44 mW max.
	Self Refresh Mode	22 mW max.	22 mW max.

- Organization : 2,097,152 words × 32 bits
- Memory : MB8118165A, 4 pcs
- 5.0 V ± 10% Supply Voltage
- 1,024 Refresh Cycles / 16.4 ms
- Self Refresh Capability
- Hyper page mode operation (EDO)
- Package and Ordering Information:
  72-pin SIMM, order as
  MB8502E032AA-××SG
  (SG = Gold Pad)

■ PACKAGE

Plastic SIMM Package

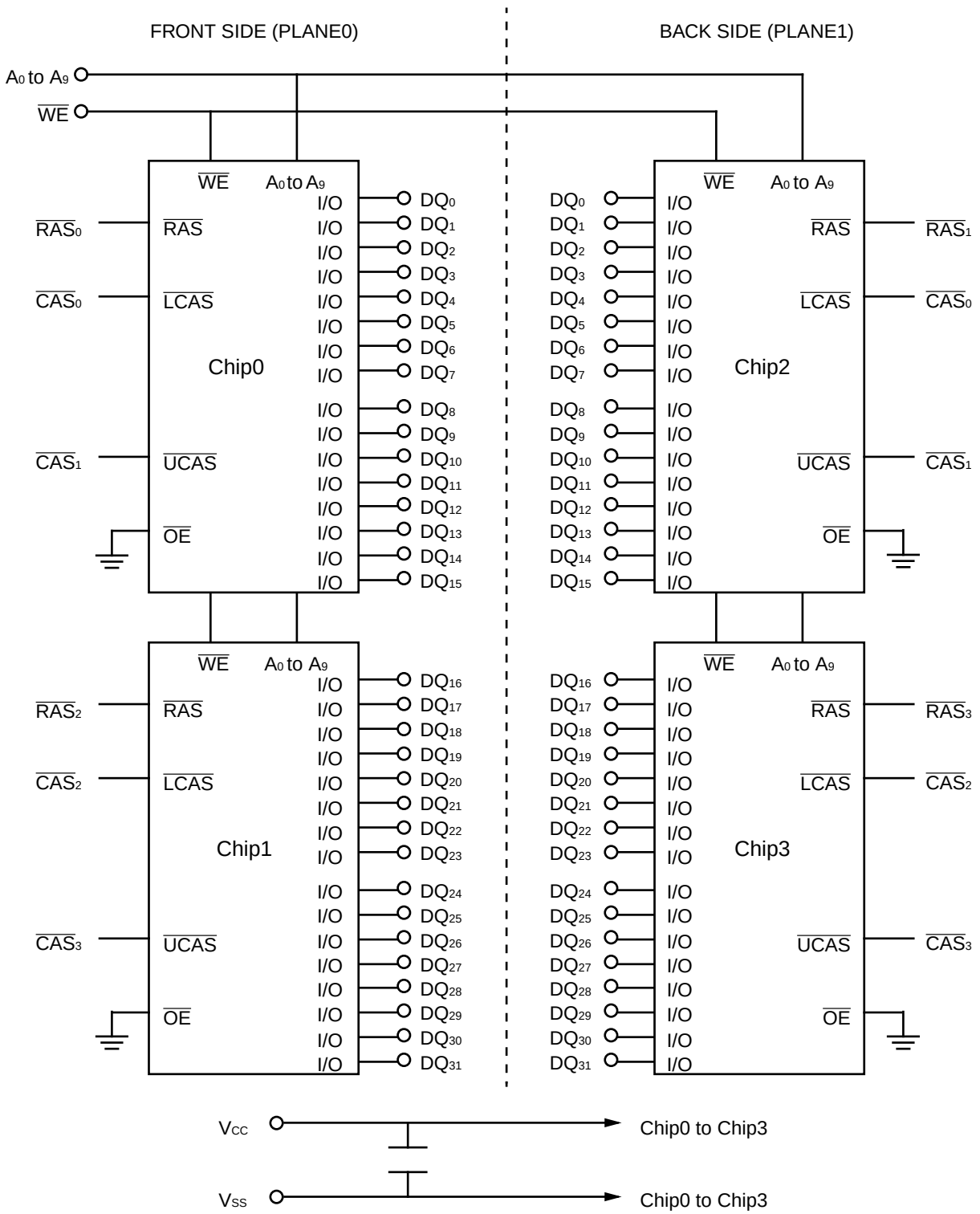


(MSS-72P-P85)

DQ_0	2	1	V_{SS}
DQ_1	4	3	DQ_{16}
DQ_2	6	5	DQ_{17}
DQ_3	8	7	DQ_{18}
V_{CC}	10	9	DQ_{19}
A_0	12	11	N.C.
A_2	14	13	A_1
A_4	16	15	A_3
A_6	18	17	A_5
DQ_4	20	19	N.C.
DQ_5	22	21	DQ_{20}
DQ_6	24	23	DQ_{21}
DQ_7	26	25	DQ_{22}
A_7	28	27	DQ_{23}
V_{CC}	30	29	N.C.
A_9	32	31	A_8
$\overline{RAS}_2$	34	33	$\overline{RAS}_3$
N.C.	36	35	N.C.
N.C.	38	37	N.C.
$\overline{CAS}_0$	40	39	V_{SS}
$\overline{CAS}_3$	42	41	$\overline{CAS}_2$
$\overline{RAS}_0$	44	43	$\overline{CAS}_1$
N.C.	46	45	$\overline{RAS}_1$
N.C.	48	47	$\overline{WE}$
DQ_{24}	50	49	DQ_8
DQ_{25}	52	51	DQ_9
DQ_{26}	54	53	DQ_{10}
DQ_{27}	56	55	DQ_{11}
DQ_{28}	58	57	DQ_{12}
DQ_{29}	60	59	V_{CC}

Pin #	Symbol	-60	-70
67	PD_1	N.C.	N.C.
68	PD_2	N.C.	N.C.
69	PD_3	N.C.	V_{SS}
70	PD_4	N.C.	N.C.

Fig.1 – BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage	V_{IN}	–0.5 to +7.0	V
Output Voltage	V_{OUT}	–0.5 to +7.0	V
Short Circuit Output Current	I_{OUT}	–50 to +50	mA
Power Dissipation	P_D	4	W
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, All Inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = 5.0 V)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	—	36	pF
Input Capacitance, $\overline{RAS}_0$ to $\overline{RAS}_3$	C_{IN2}	—	12	pF
Input Capacitance, $\overline{CAS}_0$ to $\overline{CAS}_3$	C_{IN3}	—	16	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	26	pF
I/O Capacitance, (DQ_0 to DQ_{31})	C_{DQ}	—	26	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Output High Voltage	*1		V_{OH}	I_{OH} = –5 mA	2.4	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = 4.2 mA	—	0.4	V
Input Leakage Current		$\overline{RAS}$	$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC}, 4.5 V ≤ V_{CC} ≤ 5.5 V, V_{SS} = 0 V, all other pins not under test = 0 V	–20	20	µA
		$\overline{CAS}$			–20	20	
		Address, $\overline{WE}$			–20	20	
Output Leakage Current			$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V, Data out disabled	–20	20	µA
Operating Current (Average Power Supply Current)	*2	MB8502E032AA-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min.	—	324	mA
		MB8502E032AA-70			—	304	
Standby Current (Power Supply Current)		TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	8	mA
		CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V	—	4	
Refresh Current #1 (Average Power Supply Current)	*2	MB8502E032AA-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min.	—	324	mA
		MB8502E032AA-70			—	304	
Hyper Page Mode Current	*2	MB8502E032AA-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{HPC} = min.	—	204	mA
		MB8502E032AA-70			—	184	
Refresh Current #2 (Average Power Supply Current)	*2	MB8502E032AA-60	I_{CC5}	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.	—	324	mA
		MB8502E032AA-70			—	304	
Refresh Current #3 (Average Power Supply Current)			I_{CC9}	Self Refresh	—	4	mA

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > –0.3 V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8502E032AA-60		MB8502E032AA-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	104	—	124	—	ns
3	Access Time from $\overline{RAS}$	*4,7	t_{RAC}	—	60	—	70	ns
4	Access Time from $\overline{CAS}$	*5,7	t_{CAC}	—	15	—	17	ns
5	Column Address Access Time	*6,7	t_{AA}	—	30	—	35	ns
6	Output Hold Time		t_{OH}	3	—	3	—	ns
7	Output Hold Time from $\overline{CAS}$		t_{OHC}	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*8	t_{OFF}	—	15	—	17	ns
10	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*8	t_{OFR}	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{WE}$	*8	t_{WEZ}	—	15	—	17	ns
12	Transition Time		t_T	1	50	1	50	ns
13	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	50	—	ns
14	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
15	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	17	—	ns
16	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	ns
17	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*9,10	t_{RCD}	14	45	14	53	ns
18	$\overline{CAS}$ Pulse Width		t_{CAS}	10	—	13	—	ns
19	$\overline{CAS}$ Hold Width		t_{CSH}	40	—	50	—	ns
20	$\overline{CAS}$ Precharge Time (Normal)	*17	t_{CPN}	10	—	10	—	ns
21	Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
22	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
23	Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
24	Column Address Hold Time		t_{CAH}	10	—	10	—	ns
25	Column Address Hold Time from $\overline{RAS}$		t_{AR}	24	—	24	—	ns
26	$\overline{RAS}$ to Column Address Delay Time	*11	t_{RAD}	12	30	12	35	ns
27	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
28	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	23	—	28	—	ns
29	Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
30	Read Command Hold Time Referenced to $\overline{RAS}$	*12	t_{RRH}	0	—	0	—	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB8502E032AA-60		MB8502E032AA-70		Unit
				Min.	Max.	Min.	Max.	
31	Read Command Hold Time Referenced to $\overline{CAS}$	*12	t_{RCH}	0	—	0	—	ns
32	Write Command Set Up Time	*13,18	t_{WCS}	0	—	0	—	ns
33	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
34	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	24	—	24	—	ns
35	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
36	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	17	—	ns
37	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	10	—	13	—	ns
38	DIN Set Up Time		t_{DS}	0	—	0	—	ns
39	DIN Hold Time		t_{DH}	10	—	10	—	ns
40	Data Hold Time from $\overline{RAS}$		t_{DHR}	24	—	24	—	ns
41	$\overline{RAS}$ to $\overline{WE}$ Delay Time	*18	t_{RWD}	77	—	89	—	ns
42	$\overline{CAS}$ to $\overline{WE}$ Delay Time	*18	t_{CWD}	32	—	36	—	ns
43	Column Address to $\overline{WE}$ Delay Time	*18	t_{AWD}	47	—	54	—	ns
44	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	5	—	5	—	ns
45	$\overline{CAS}$ Set Up Time (C-B-R Refresh)		t_{CSR}	0	—	0	—	ns
46	$\overline{CAS}$ Hold Time (C-B-R Refresh)		t_{CHR}	10	—	12	—	ns
47	$\overline{RAS}$ to Data in Delay Time		t_{RDD}	15	—	17	—	ns
48	$\overline{CAS}$ to Data in Delay Time		t_{CDD}	15	—	17	—	ns
49	DIN to $\overline{CAS}$ Delay Time	*15	t_{DZC}	0	—	0	—	ns
50	$\overline{WE}$ Precharge Time		t_{WPZ}	8	—	8	—	ns
51	$\overline{WE}$ to Data in Delay Time		t_{WED}	15	—	17	—	ns
52	Hyper Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	100000	—	100000	ns
53	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	30	—	ns
54	Access Time from $\overline{CAS}$ Precharge	*7,16	t_{CPA}	—	35	—	40	ns
55	Hyper Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
56	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns
57	Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	*18	t_{CPWD}	52	—	59	—	ns
58	$\overline{RAS}$ Pulse Width (Self Refresh)	*19	t_{RASS}	100	—	100	—	µs
59	$\overline{RAS}$ Precharge Time (Self Refresh)	*19	t_{RPS}	104	—	124	—	ns
60	$\overline{CAS}$ Hold Time (Self Refresh)	*19	t_{CHS}	–50	—	–50	—	ns

Notes: *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume t_T = 5 ns.

*3. V_{IH} (min) and V_{IL} (max) are reference levels for measureing the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. t_{OFF}, t_{OEZ}, t_{OFR} and t_{WEZ} are specified that output buffer change to high-impedance state.

*9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*10. t_{RCD} (min) = t_{RAH} (min)+ 2 t_T + t_{ASC} (min).

*11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. Assumes that $t_{WCS} < t_{WCS}$ (min).

*15. Either t_{DZC} or t_{DZO} must be satisfied.

*16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).

*17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

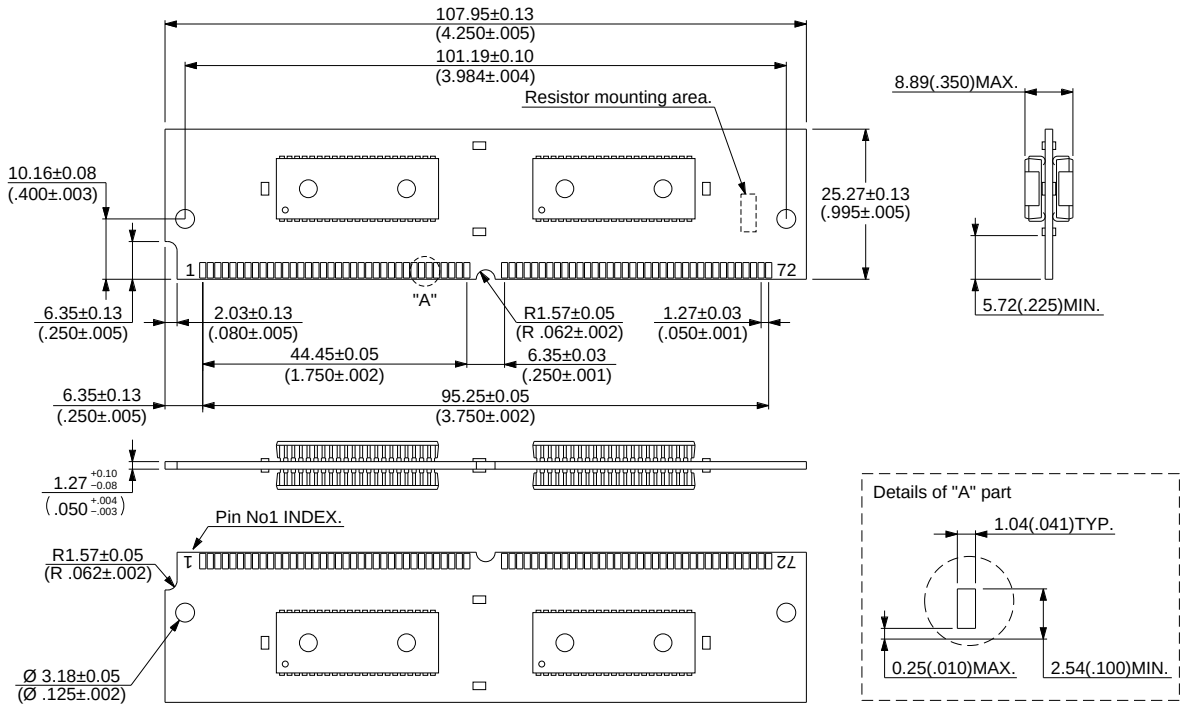
*18. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high-impedance state thoughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} specifications.

*19. Assumes that self refresh.

*Source: See MB8118165A Data Sheet for details on the electricals.

■ PACKAGE DIMENSIONS

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P85)



Dimensions in mm (inches)

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