

# 74LVC2G00

## Dual 2-input NAND gate

Rev. 04 — 15 May 2006

Product data sheet

## 1. General description

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The 74LVC2G00 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G00 provides the 2-input NAND gate function.

## 2. Features

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- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Complies with JEDEC standard:
  - ◆ JESD8-7 (1.65 V to 1.95 V)
  - ◆ JESD8-5 (2.3 V to 2.7 V)
  - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-C exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C

**PHILIPS**

### 3. Ordering information

Table 1. Ordering information

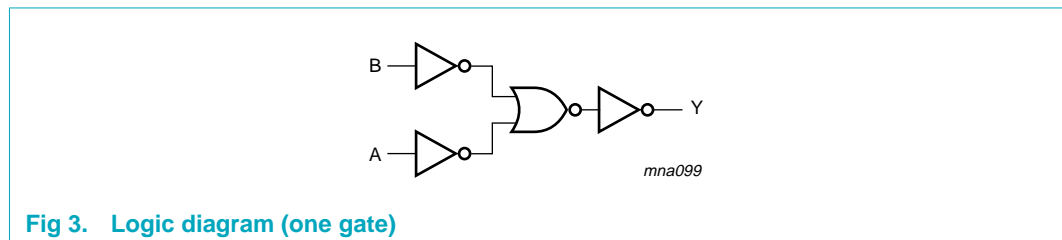
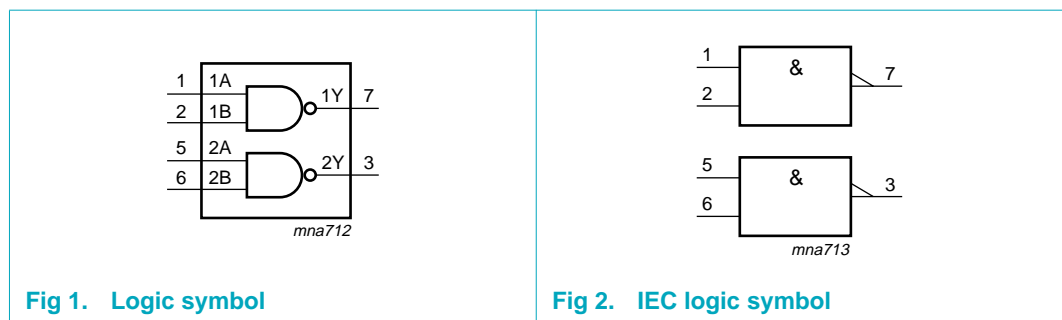
Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G00DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G00GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G00GM	-40 °C to +125 °C	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-1

### 4. Marking

Table 2. Marking

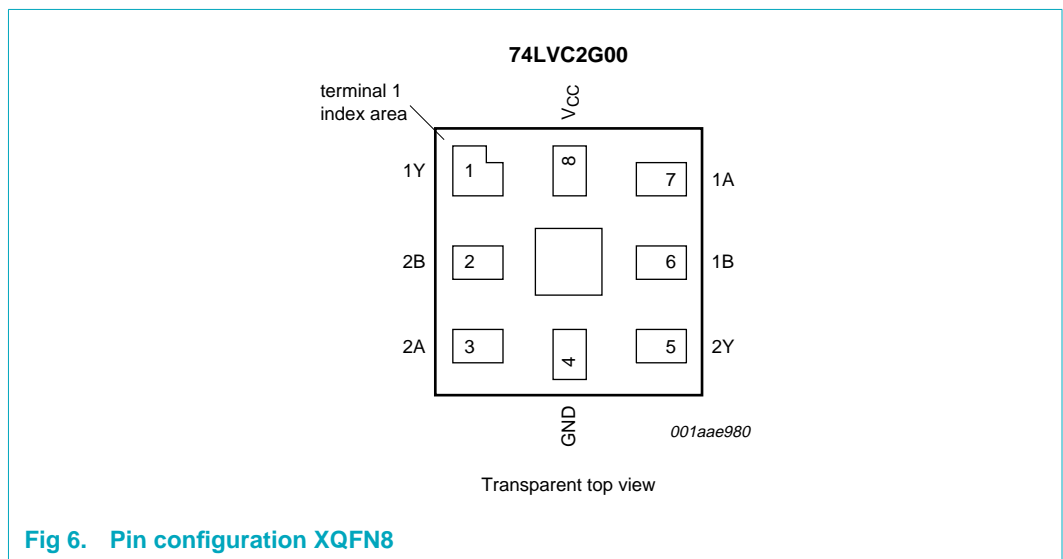
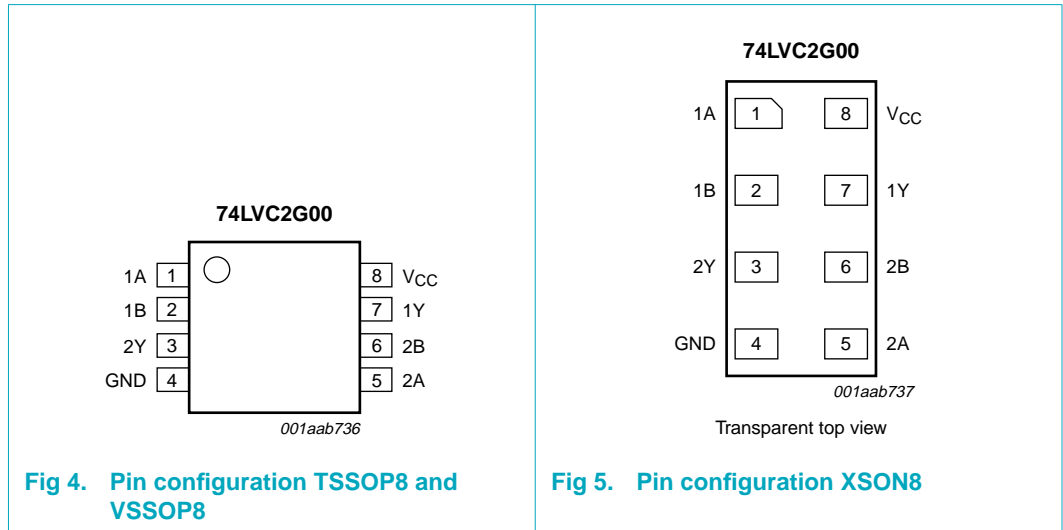
Type number	Marking code
74LVC2G00DP	V00
74LVC2G00DC	V00
74LVC2G00GT	V00
74LVC2G00GM	V00

### 5. Functional diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin			Description
	TSSOP8, VSSOP8	XSON8	XQFN8	
1A	1	1	7	data input 1A
1B	2	2	6	data input 1B
2Y	3	3	5	data output 2Y
GND	4	4	4	ground (0 V)
2A	5	5	3	data input 2A

Table 3. Pin description ...continued

Symbol	Pin			Description
	TSSOP8, VSSOP8	XSON8	XQFN8	
2B	6	6	2	data input 2B
1Y	7	7	1	data output 1Y
V <sub>CC</sub>	8	8	8	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4. Function table<sup>[1]</sup>

Input		Output	
nA	nB	nY	
L	L	H	
L	H	H	
H	L	H	
H	H	L	

- [1] H = HIGH voltage level;  
L = LOW voltage level.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> -0.5	+6.5	V
V <sub>O</sub>	output voltage	Active mode	<sup>[1]</sup> -0.5	V <sub>CC</sub> + 0.5	V
		Power-down mode	<sup>[1][2]</sup> -0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-	-50	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub>	-	±50	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	quiescent supply current		-	100	mA
I <sub>GND</sub>	ground current		-	-100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	-	300	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] When V<sub>CC</sub> = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.  
 [3] For TSSOP8 package: above 55 °C the value of P<sub>tot</sub> derates linearly with 2.5 mW/K.  
 For VSSOP8 package: above 110 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
 For TXSON8 and XQFN8 packages: above 45 °C the value of P<sub>tot</sub> derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	Active mode	0	-	$V_{CC}$	V
		Power-down mode	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$	0	-	10	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40 \text{ °C to } +85 \text{ °C}</math> [1]</b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	1.53	-	V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	2.13	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	2.50	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3	2.60	-	V
		$I_O = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8	4.10	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH} \text{ or } V_{IL}$				
		$I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.1	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	0.08	0.45	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	0.14	0.3	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	0.19	0.4	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	0.37	0.55	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.43	0.55	V
$I_{LI}$	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 5.5 \text{ V}$	-	$\pm 0.1$	$\pm 5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_I \text{ or } V_O = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	$\pm 0.1$	$\pm 10$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	0.1	10	$\mu\text{A}$

**Table 7. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta I_{CC}$	additional quiescent supply current	per pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	5	500	$\mu$ A
$C_i$	input capacitance		-	2.5	-	pF
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$V_{IH}$	HIGH-state input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5$ V to 5.5 V	$0.7 \times V_{CC}$	-	-	V
$V_{IL}$	LOW-state input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
$V_{OH}$	HIGH-state output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4$ mA; $V_{CC} = 1.65$ V	0.95	-	-	V
		$I_O = -8$ mA; $V_{CC} = 2.3$ V	1.7	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	1.9	-	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V	2.0	-	-	V
$V_{OL}$	LOW-state output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100$ $\mu$ A; $V_{CC} = 1.65$ V to 5.5 V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 1.65$ V	-	-	0.70	V
		$I_O = 8$ mA; $V_{CC} = 2.3$ V	-	-	0.45	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	-	0.60	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V	-	-	0.80	V
$I_{LI}$	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 5.5$ V	-	-	$\pm 20$	$\mu$ A
		$V_I$ or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	-	$\pm 20$	$\mu$ A
$I_{OFF}$	power-off leakage current	$V_I$ or $V_O = 5.5$ V; $V_{CC} = 0$ V	-	-	$\pm 20$	$\mu$ A
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	$\mu$ A
$\Delta I_{CC}$	additional quiescent supply current	per pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.3$ V to 5.5 V	-	-	5000	$\mu$ A

[1] All typical values are measured at  $T_{amb} = 25$  °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay input nA, nB to output nY	see <a href="#">Figure 7</a>					
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	3.5	8.6	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	2.3	4.8	ns	
		V <sub>CC</sub> = 2.7 V	0.7	3.0	5.6	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7	2.2	4.3	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.3	ns	
C <sub>PD</sub>	power dissipation capacitance	per gate; V <sub>I</sub> = GND to V <sub>CC</sub>	[2]	-	14	-	pF
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay input nA, nB to output nY	see <a href="#">Figure 7</a>					
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.2	-	10.8	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	-	6.0	ns	
		V <sub>CC</sub> = 2.7 V	0.7	-	7.0	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7	-	5.4	ns	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	-	4.2	ns	

[1] All typical values are measured at nominal V<sub>CC</sub> and T<sub>amb</sub> = 25 °C.

[2] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

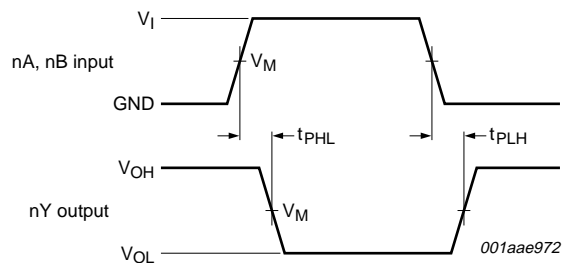
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

## 12. Waveforms



Measurement points are given in [Table 9](#).

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

**Fig 7. Input (nA, nB) to output (nY) propagation delays**

Table 9. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$

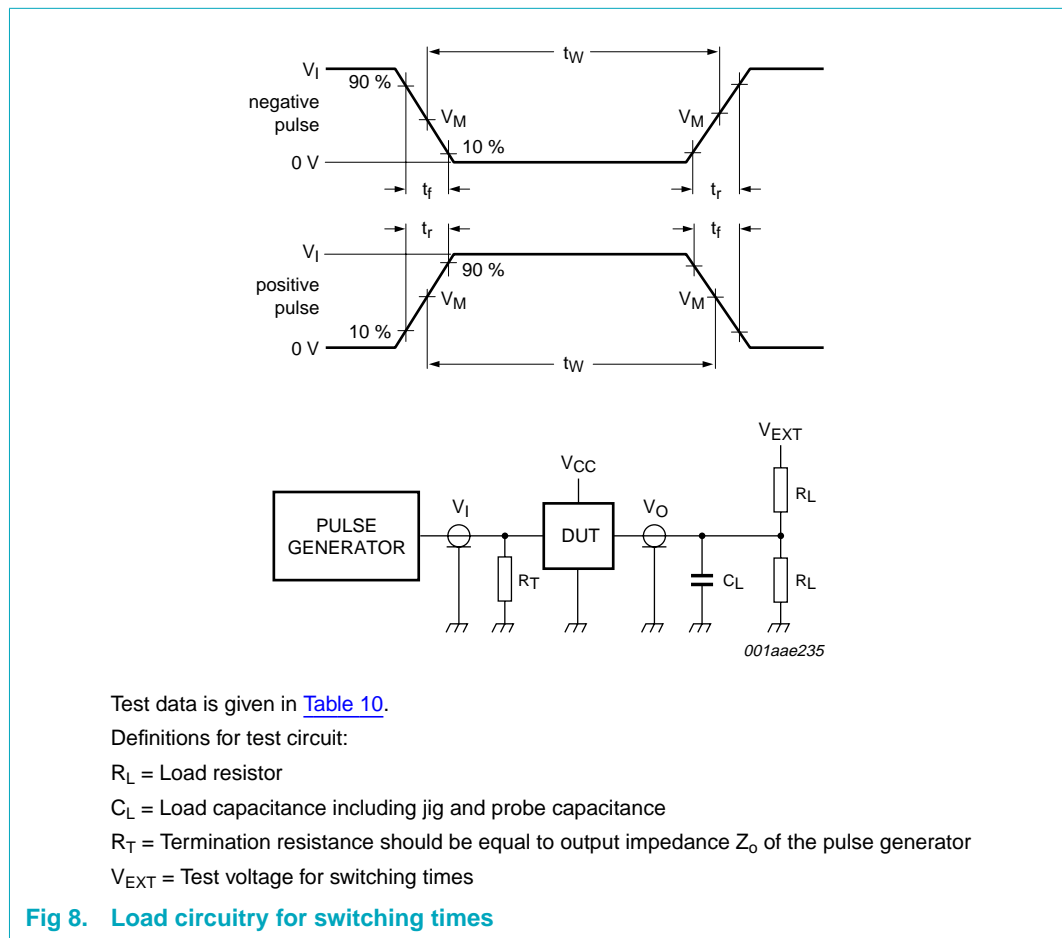


Table 10. Test data

Supply voltage	Input		Load		$V_{EXT}$
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open



13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

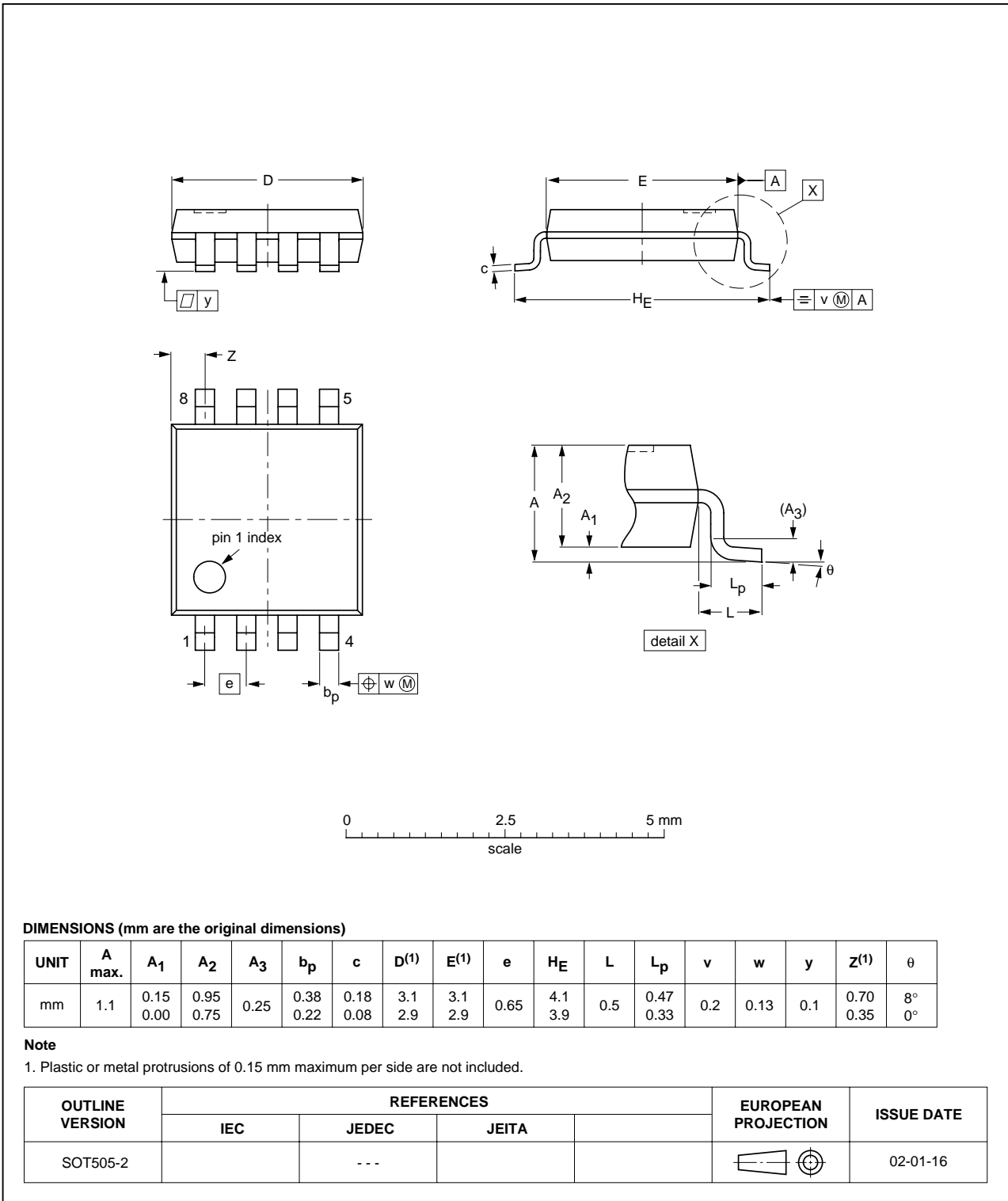


Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

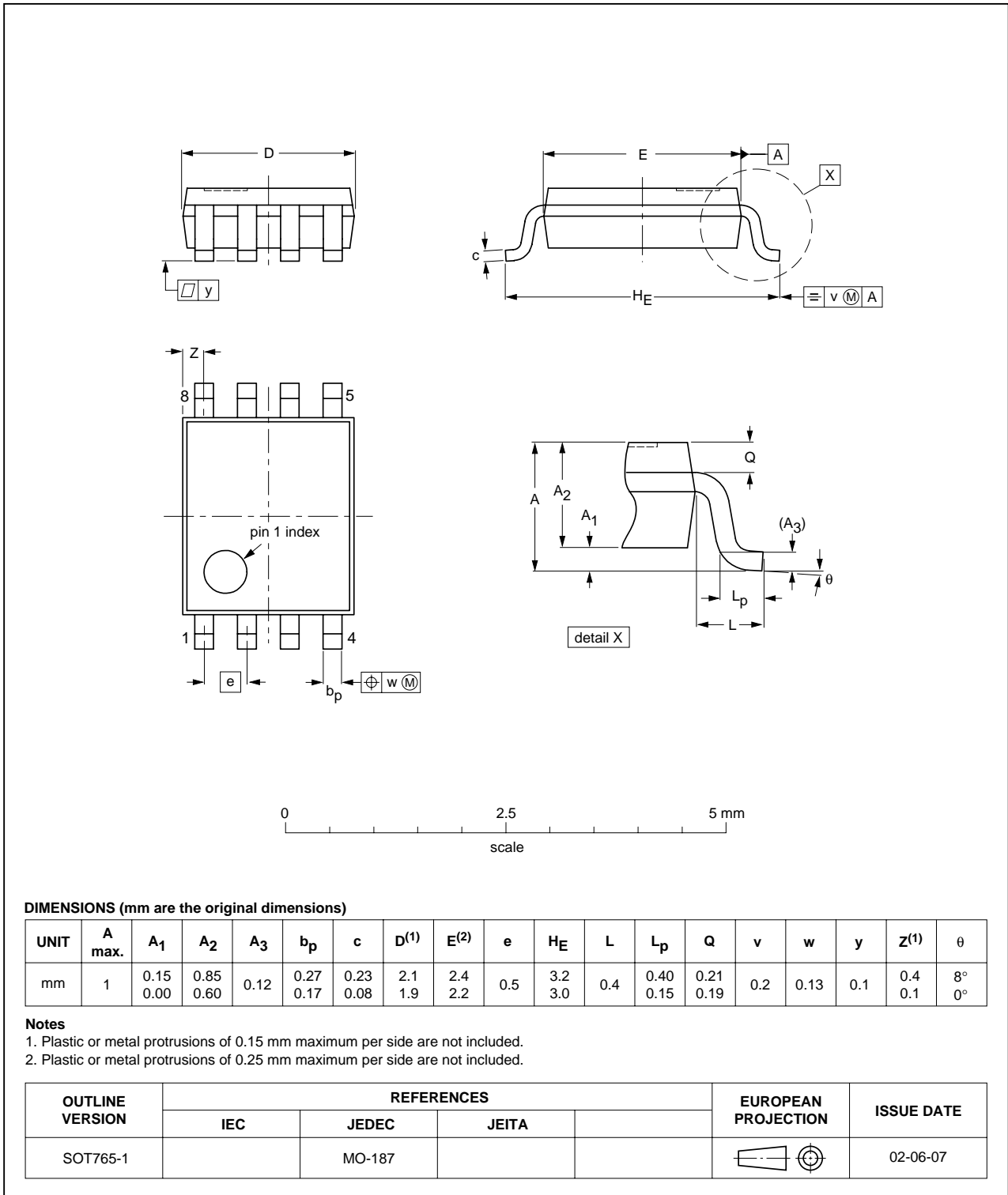


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

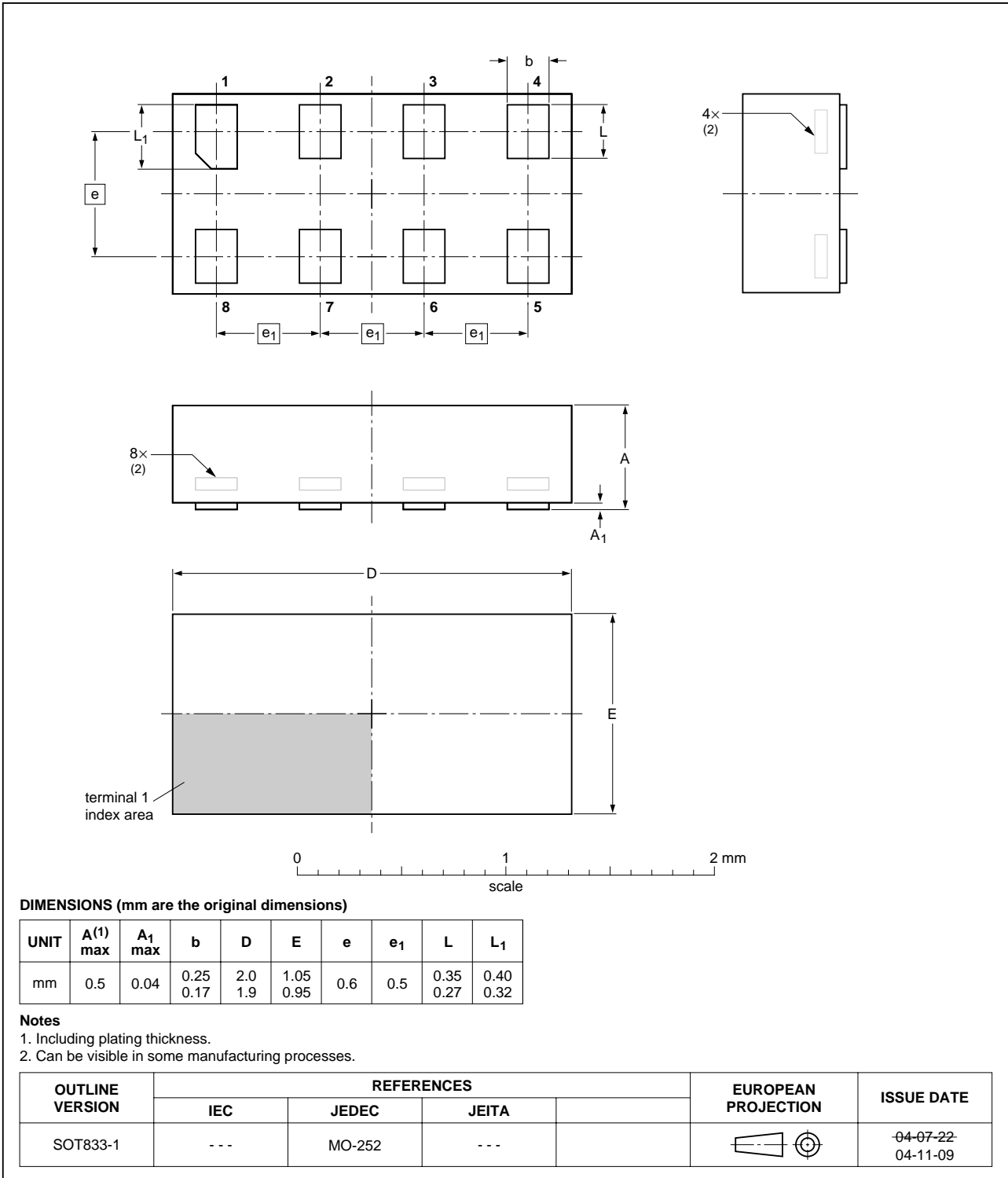


Fig 11. Package outline SOT833-1 (XSON8)

XQFN8: plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-1

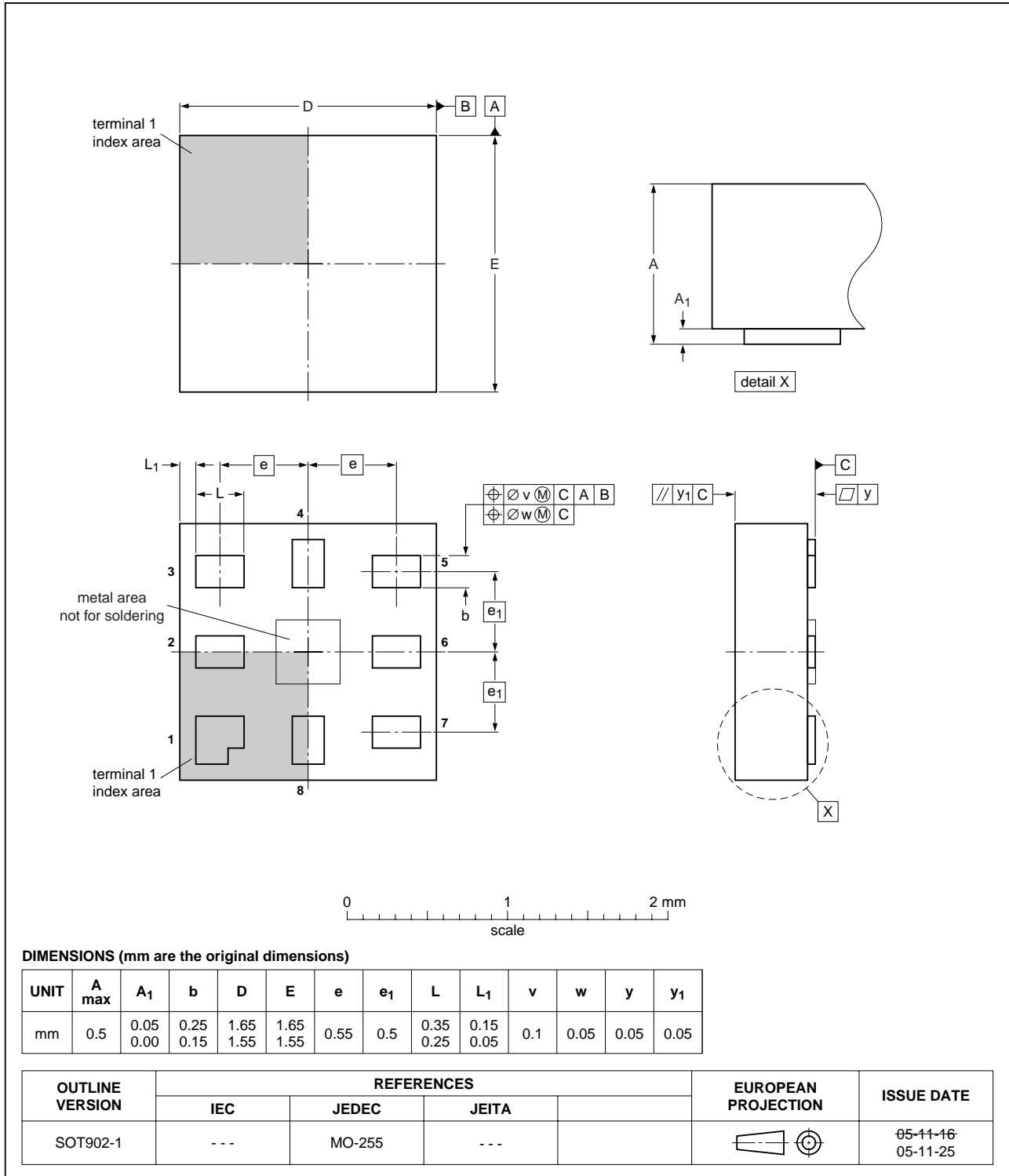


Fig 12. Package outline SOT902-1 (XQFN8)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G00_4	20060515	Product data sheet	-	74LVC2G00_3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li>Added: type number 74LVC2G00GM (XQFN8 package)</li> </ul>			
74LVC2G00_3 (9397 750 14531)	20050201	Product specification	-	74LVC2G00_2
74LVC2G00_2 (9397 750 13771)	20040923	Product specification	-	74LVC2G00_1
74LVC2G00_1 (9397 750 11953)	20031117	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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