

# MC100EPT22

## 3.3V Dual LVTTTL/LVCMOS to Differential LVPECL Translator

### Description

The MC100EPT22 is a dual LVTTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead package and the single gate of the EPT22 makes it ideal for those applications where space, performance, and low power are at a premium. Because the mature MOSAIC 5 process is used, low cost and high speed can be added to the list of features.

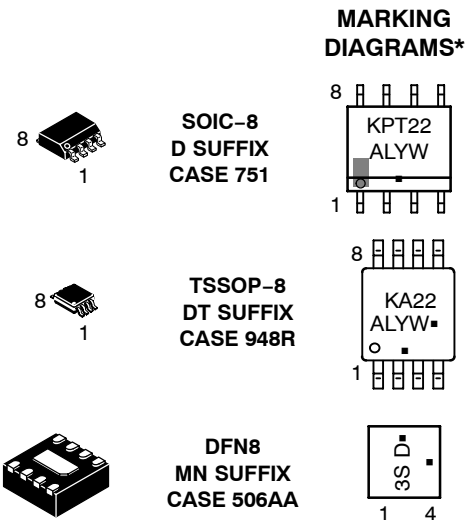
### Features

- 420 ps Typical Propagation Delay
- Maximum Frequency > 1.1 GHz Typical
- Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.6\text{ V}$  with  $GND = 0\text{ V}$
- PNP LVTTTL Inputs for Minimal Loading
- Q Output Will Default HIGH with Inputs Open
- The 100 Series Contains Temperature Compensation.
- Pb-Free Packages are Available



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D = Date Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

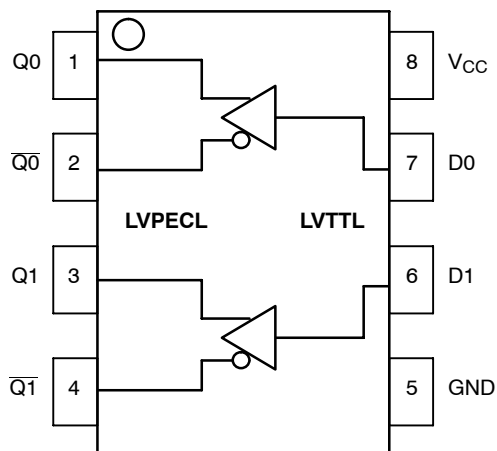
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
Q0, Q1, $\overline{Q0}$ , $\overline{Q1}$	LVPECL Differential Outputs
D0, D1	LVTTTL Inputs
V <sub>CC</sub>	Positive Supply
GND	Ground

**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 2. ATTRIBUTES**

Characteristics	Value	
Internal Input Pulldown Resistor	N/A	
Internal Input Pullup Resistor	N/A	
ESD Protection	Human Body Model	> 4 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	SOIC-8	Level 1
	TSSOP-8	Level 1
	DFN8	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	164 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Power Supply	GND = 0 V		6	V
V <sub>I</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6 to 0	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T <sub>sol</sub>	Wave Solder	Pb Pb-Free		265 265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

**Table 4. TTL INPUT DC CHARACTERISTICS** V<sub>CC</sub> = 3.3 V, GND = 0 V, T<sub>A</sub> = -40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = 2.7 V			20	μA
I <sub>IHH</sub>	Input HIGH Current MAX	V <sub>IN</sub> = V <sub>CC</sub>			100	μA
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0.5 V			-0.6	mA
V <sub>IK</sub>	Input Clamp Voltage	I <sub>IN</sub> = -18 mA			-1.0	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 5. PECL OUTPUT DC CHARACTERISTICS** V<sub>CC</sub> = 3.3 V, GND = 0.0 V (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>CC</sub>	Power Supply Current	32	43	55	35	45	60	37	46	62	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V <sub>OL</sub>	Output LOW Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Output parameters vary 1:1 with V<sub>CC</sub>.
3. All loading with 50 Ω to V<sub>CC</sub> - 2.0 V.

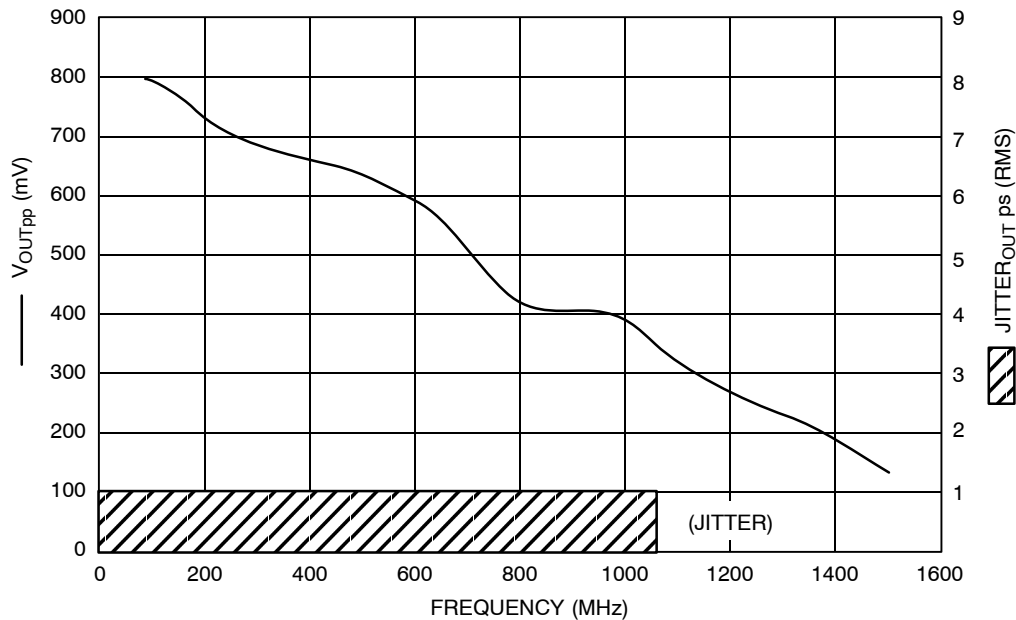
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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0.0\text{ V}$  (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (Figure 2)	0.8	1.1		0.8	1.1		0.8	1.1		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential	250	400	650	250	420	675	300	500	700	ps
$t_{skew}$	Within-Device Skew (Note 5) Device-to-Device Skew (Note 6)		50 200	100 400		50 200	100 425		50 200	100 400	ps
$t_{JITTER}$	Random Clock Jitter (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
$t_r$ $t_f$	Output Rise/Fall Times (20% - 80%) Q, $\bar{Q}$	50	110	200	60	120	220	70	140	250	ps

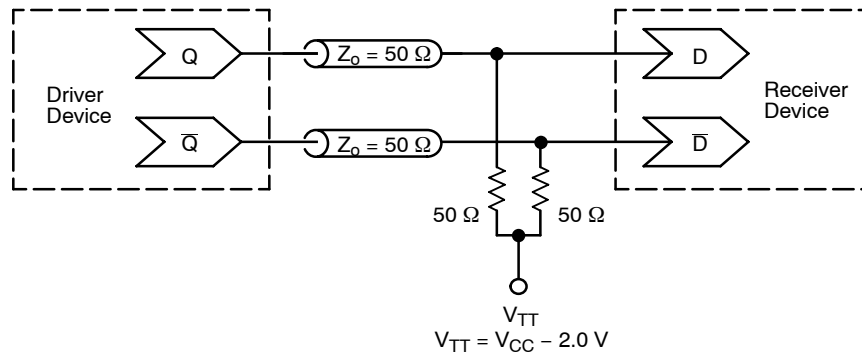
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Measured using a 2.4 V source, 50% duty cycle clock source. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
5. Skew is measured between outputs under identical transitions and conditions on any one device.
6. Device-to-Device Skew for identical transitions at identical  $V_{CC}$  levels.



**Figure 2.  $F_{max}$ /Jitter**

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**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100EPT22D	SOIC-8	98 Units / Rail
MC100EPT22DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100EPT22DR2	SOIC-8	2500 / Tape & Reel
MC100EPT22DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100EPT22DT	TSSOP-8	100 Units / Rail
MC100EPT22DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EPT22DTR2	TSSOP-8	2500 / Tape & Reel
MC100EPT22DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EPT22MNR4	DFN8	1000 / Tape & Reel
MC100EPT22MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

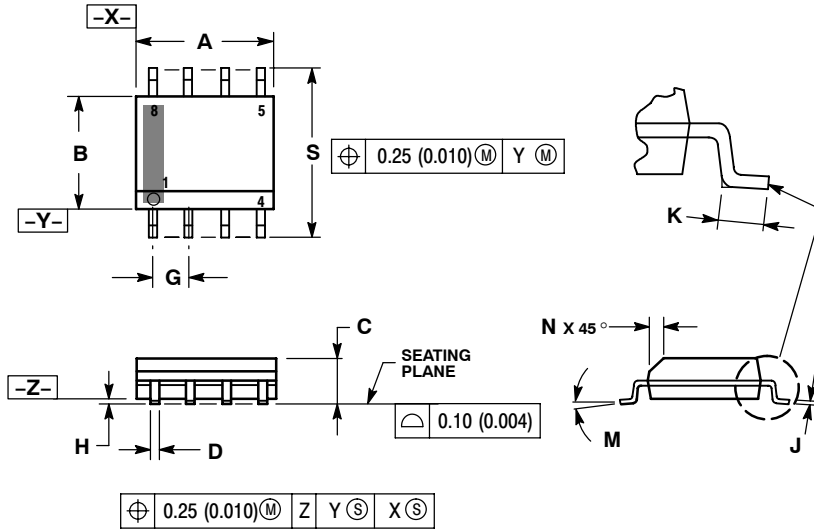
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AG

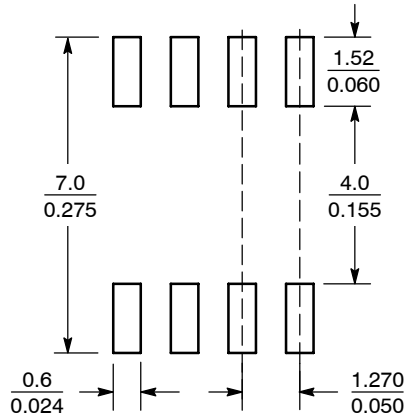


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



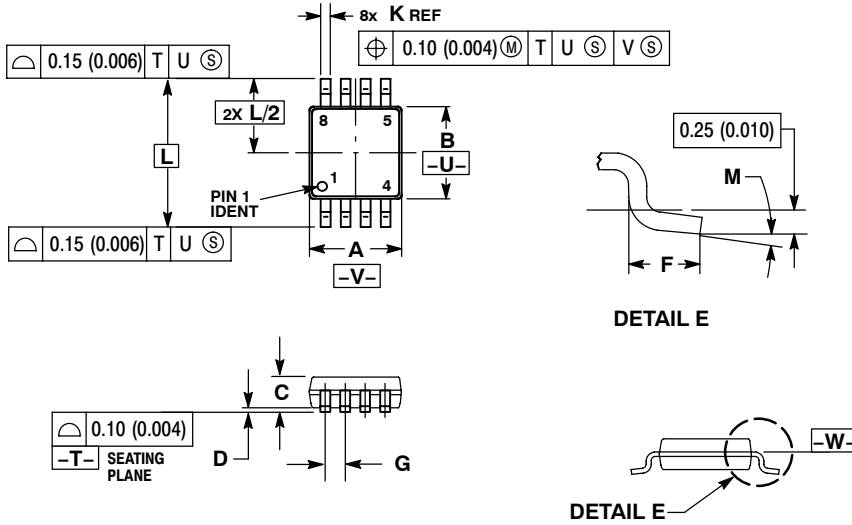
SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

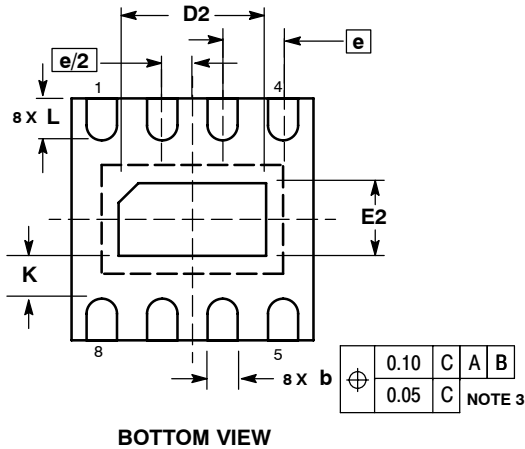
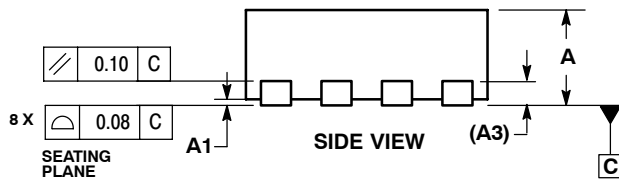
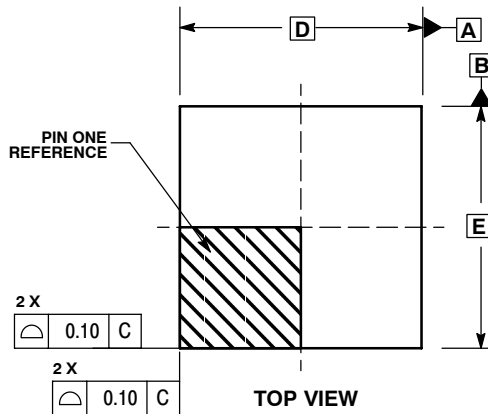
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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