LINEAR SYSTEMS

LS830
MONOLITHIC DUAL
N-CHANNEL JFET

micross

Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS830 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS830 features a 5-mV offset and 10-µV/°C drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS830 Applications:

- Wideband Differential Amps
- High-Speed,Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES	
ULTRA LOW DRIFT	$\lvert V_{GS1-2} / T \rvert \le 5\mu V/°C$ TYP.
ULTRA LOW LEAKGE	I_G = 80fA TYP.
LOW NOISE	e_n = 70nV/√Hz TYP.
LOW CAPACITANCE	C_{ISS} = 3pF MAX.

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-65°C to +150°C
Operating Junction Temperature		+150°C
Maximum Voltage and Current for Each Transistor – Note 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10µA
Maximum Power Dissipation		
Device Dissipation @ Free Air – Total		40mW @ +125°C

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED				
SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$\lvert V_{GS1-2} / T \rvert$ max.	DRIFT VS. TEMPERATURE	5	µV/°C	V_{DG}=10V, I_D=30µA T_A=-55°C to +125°C
$\lvert V_{GS1-2} \rvert$ max.	OFFSET VOLTAGE	25	mV	V_{DG}=10V, I_D=30µA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

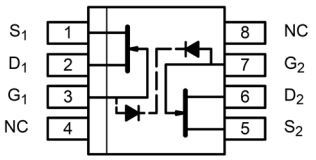
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	40	60	--	V	V_{DS} = 0 I_D=1nA
BV_{GGO}	Gate-To-Gate Breakdown	40	--	--	V	I_G= 1nA I_D= 0 I_S= 0
	TRANSCONDUCTANCE					
Y_{fss}	Full Conduction	70	300	500	µmho	V_{DG}= 10V V_{GS}= 0V f = 1kHz
Y_{fs}	Typical Operation	50	100	200	µmho	V_{DG}= 10V I_D= 30µA f = 1kHz
$\lvert Y_{FS1-2} / Y_{FS} \rvert$	Mismatch	--	0.6	3	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	0.5	--	10	mA	V_{DG}= 10V V_{GS}= 0V
$\lvert I_{DSS1-2} / I_{DSS} \rvert$	Mismatch at Full Conduction	--	1	5	%	
	GATE VOLTAGE					
V_{GS}(off) or V_p	Pinchoff voltage	0.6	2	4.5	V	V_{DS}= 10V I_D= 1nA
V_{GS}(on)	Operating Range	--	--	4	V	V_{DS}=10V I_D=30µA
	GATE CURRENT					
$-I_G$max.	Operating	--	--	0.1	pA	V_{DG}= 10V I_D= 30µA
$-I_G$max.	High Temperature	--	--	0.1	nA	T_A= +125°C
$-I_{GSS}$max.	At Full Conduction	--	--	0.2	pA	V_{DS} =0
$-I_{GSS}$max.	High Temperature	5	5	0.5	nA	V_{GS}= 0V, V_{GS}= -20V, T_A= +125°C
I_{GGO}	Gate-to-Gate Leakage	--	1	--	pA	V_{GG} = 20V
	OUTPUT CONDUCTANCE					
Y_{oss}	Full Conduction	--	--	5	µmho	V_{DG}= 10V V_{GS}= 0V
Y_{os}	Operating	--	--	0.5	µmho	V_{DG}= 10V I_D= 30µA
CMR	**COMMON MODE REJECTION**					
	-20 log $\lvert V_{GS1-2} / V_{DS} \rvert$	--	90	--	dB	ΔV_{DS} = 10 to 20V I_D=30µA
	-20 log $\lvert V_{GS1-2} / V_{DS} \rvert$	--	90	--		ΔV_{DS} = 5 to 10V I_D=30µA
	NOISE					
NF	Figure	--	--	1	dB	V_{DS}= 10V V_{GS}= 0V R_G= 10MΩ f= 100Hz NBW= 6Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DS}=10V I_D=30µA f=10Hz NBW=1Hz
	CAPACITANCE					
C_{iss}	Input	--	--	3	pF	V_{DS}= 10V, V_{GS}= 0V, f= 1MHz
C_{rss}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V, V_{GS}= 0V, f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DS}= 10V, I_D=30µA

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS830 / LS830 in PDIP & SOIC
LS830 / LS830 available as bare die
Please contact Micross for full package and die dimensions

PDIP & SOIC (Top View)



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