

# THC63LVD1027

## 85MHz 10Bits Dual LVDS Repeater

### General Description

The THC63LVD1027 LVDS(Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.

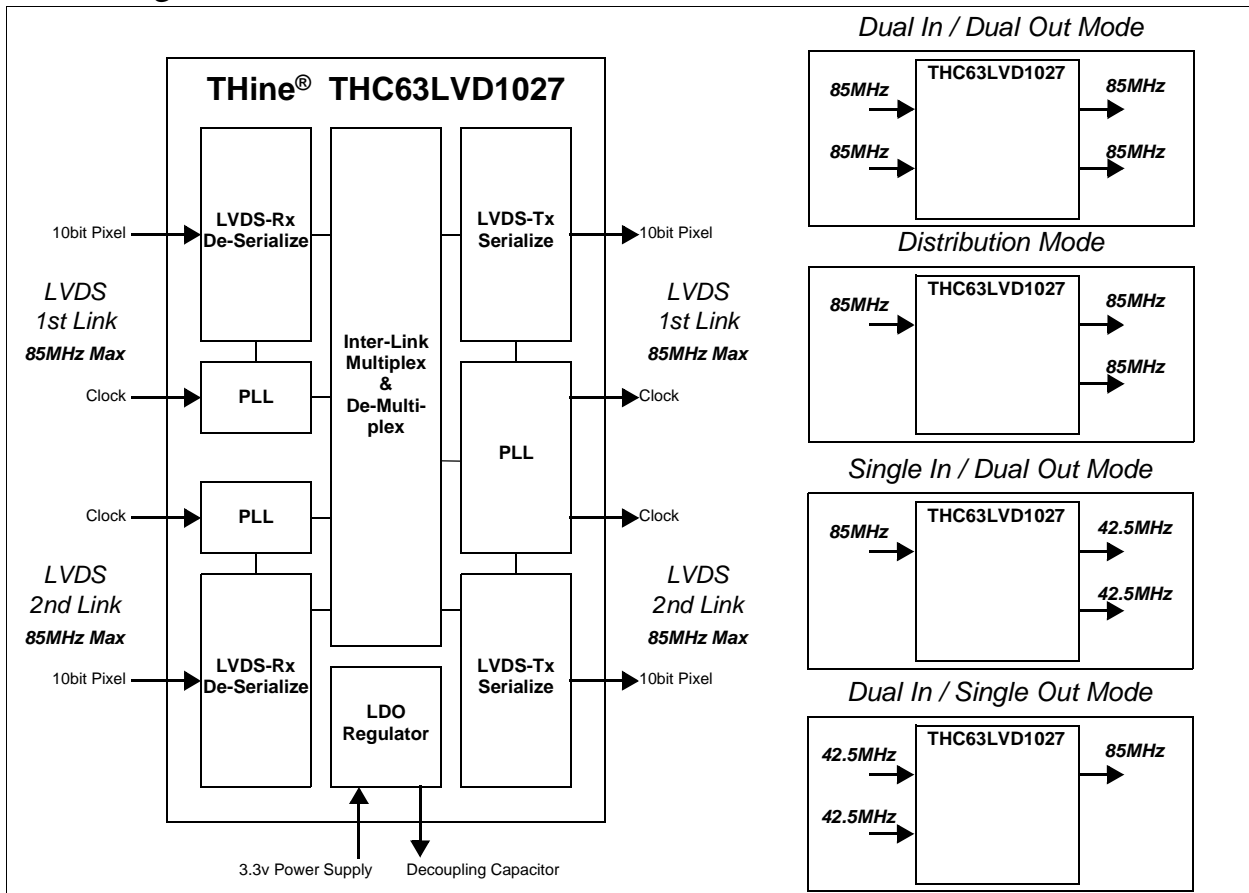
THC63LVD1027 receives the dual channel LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.

At a transmit clock frequency of 85MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE) are transmitted at an effective rate of 595Mbps per LVDS channel.

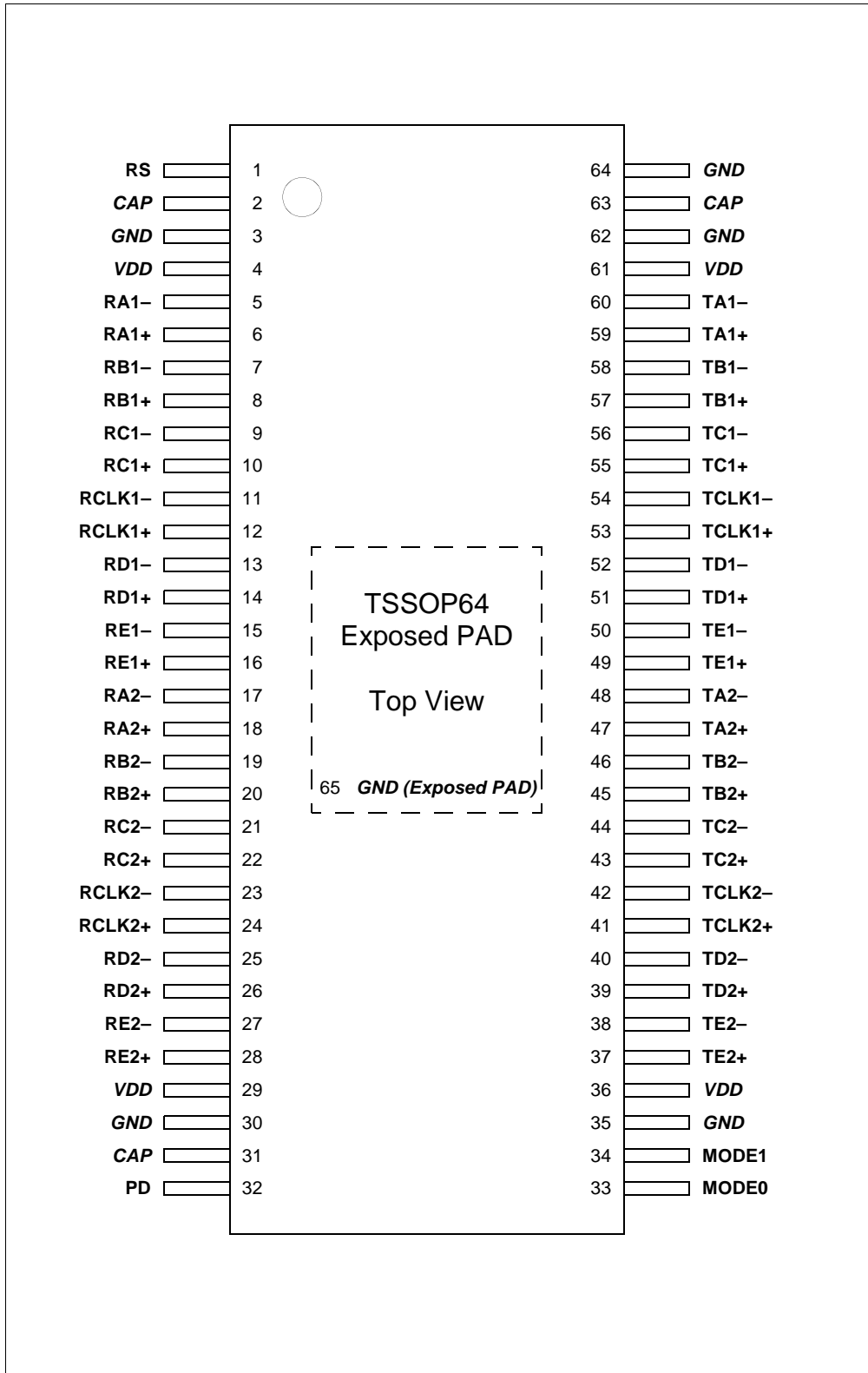
### Features

- Up to 85MHz 10bit dual channel LVDS Receiver
- Up to 85MHz 10bit dual channel LVDS Transmitter
- Wide LVDS input skew margin:  $\pm 480\text{ps}$  at 75MHz
- Accurate LVDS output timing:  $\pm 250\text{ps}$  at 75MHz
- Reduced swing LVDS output mode supported to suppress the system EMI
- Various line rate conversion modes supported  
Dual link input / Dual link output [clkout=1x clkin]  
Single link input / Dual link output [clkout=1/2x clkin]  
Dual link input / Single link output [clkout=2x clkin]
- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- No external components required for PLLs
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)

### Block Diagram



Pin Out



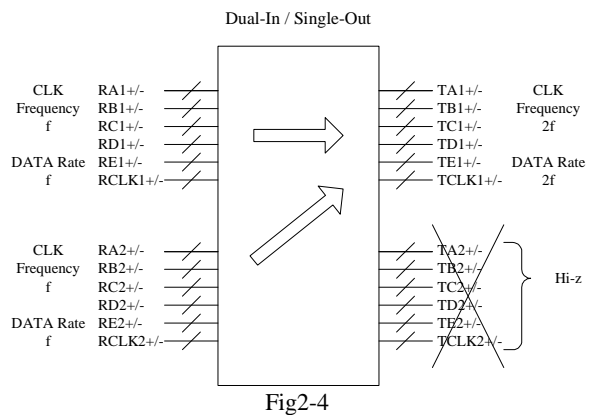
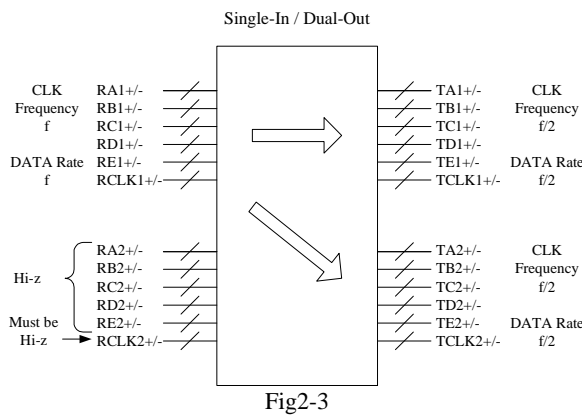
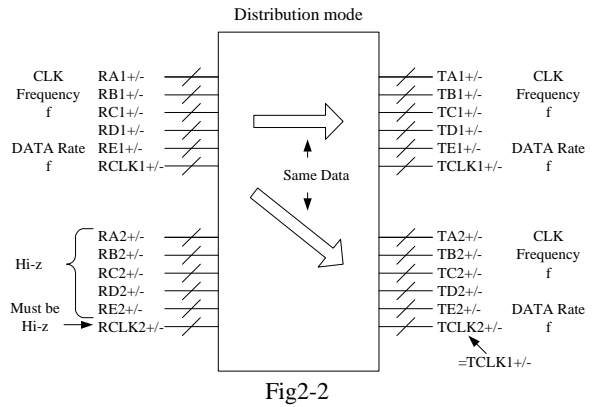
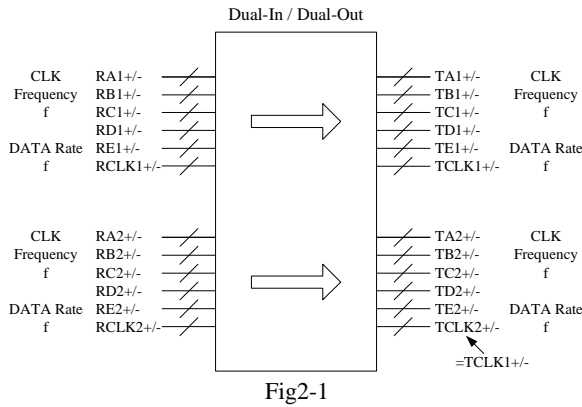
## Pin Description

Pin Name	Direction	Type	Description																								
RA1+/-	Input	LVDS	LVDS data input for channel A of 1st Link																								
RB1+/-			LVDS data input for channel B of 1st Link																								
RC1+/-			LVDS data input for channel C of 1st Link																								
RD1+/-			LVDS data input for channel D of 1st Link																								
RE1+/-			LVDS data input for channel E of 1st Link																								
RCLK1+/-			LVDS clock input for 1st Link																								
RA2+/-			LVDS data input for channel A of 2nd Link																								
RB2+/-			LVDS data input for channel B of 2nd Link																								
RC2+/-			LVDS data input for channel C of 2nd Link																								
RD2+/-			LVDS data input for channel D of 2nd Link																								
RE2+/-			LVDS data input for channel E of 2nd Link																								
RCLK2+/-			LVDS clock input for 2nd Link In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z. (see "Mode selection" below in this page.)																								
TA1+/-			Output	LVDS	LVDS data output for channel A of 1st Link																						
TB1+/-					LVDS data output for channel B of 1st Link																						
TC1+/-	LVDS data output for channel C of 1st Link																										
TD1+/-	LVDS data output for channel D of 1st Link																										
TE1+/-	LVDS data output for channel E of 1st Link																										
TCLK1+/-	LVDS clock output for 1st Link																										
TA2+/-	LVDS data output for channel A of 2nd Link																										
TB2+/-	LVDS data output for channel B of 2nd Link																										
TC2+/-	LVDS data output for channel C of 2nd Link																										
TD2+/-	LVDS data output for channel D of 2nd Link																										
TE2+/-	LVDS data output for channel E of 2nd Link																										
TCLK2+/-	LVDS clock output for 2nd Link																										
PD	Input	LV-TTL			<b>Power Down</b> H: Normal operation L: Power down state, all LVDS output signals turn to Hi-Z																						
RS					<b>LVDS output swing level selection</b> H: Normal swing L: Reduced swing																						
MODE1 MODE0			<b>Mode selection</b>																								
			<table border="1"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>RCLK2+/-</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>clkin</td> <td>Dual-in / Dual-out mode</td> </tr> <tr> <td>L</td> <td>L</td> <td>Hi-Z</td> <td>Distribution mode</td> </tr> <tr> <td>H</td> <td>L</td> <td>Hi-Z</td> <td>Single-in / Dual-out mode</td> </tr> <tr> <td>L</td> <td>H</td> <td>clkin</td> <td>Dual-in / Single-out mode</td> </tr> <tr> <td>H</td> <td>H</td> <td>-</td> <td>Reserved</td> </tr> </tbody> </table>	MODE1	MODE0	RCLK2+/-	Description	L	L	clkin	Dual-in / Dual-out mode	L	L	Hi-Z	Distribution mode	H	L	Hi-Z	Single-in / Dual-out mode	L	H	clkin	Dual-in / Single-out mode	H	H	-	Reserved
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H	H	-	Reserved																								
VDD	Power	—	<b>3.3v power supply pins</b>																								
GND			<b>Ground pins (Exposed PAD is also Ground)</b>																								
CAP			<b>Decoupling capacitor pins</b> These pins should be connected to external decoupling capacitors (CCAP). Recommended CCAP is 0.1uF																								

## Mode Setting

Input/Output	RCLK2+/-	MODE1 (Input mode)	MODE0 (Output mode)
		H: Single L: Dual	H: Single L: Dual
Dual-In/Dual-Out (Fig.2-1, 3-1)	CLK in	L	L
Distribution (Fig.2-2, 3-2)	Hi-z	L	L
Single-In/Dual-Out (Fig.2-3, 3-3)	Hi-z	H	L
Dual-In/Single-Out (Fig.2-4, 3-4)	CLK in	L	H
Reserved	--	H	H

## Signal Flow for Each Setting



## Output Control / Fail Safe

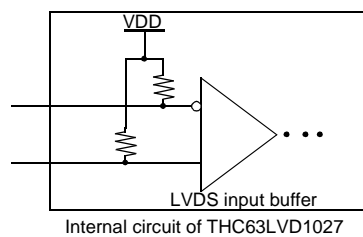
THC63LVD1027 has a function to control output depending on LVDS input condition.

PD	RCLK1+/-	RCLK2+/-	Output
L	*	*	All Hi-z
H	Hi-z	*	All Hi-z
H	CLK in	CLK in	Refer to <a href="#">p.4 Mode Setting #</a>
H	CLK in	Hi-z	Refer to <a href="#">p.4 Mode Setting #</a>

\*: Don't care

#: If a particular input data pair is Hi-z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting state of Hi-z.



## Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power Supply voltage	-0.3	4.0	V
LVDS Input Voltage	-0.3	V <sub>DD</sub> +0.3	V
Junction Temperature	—	125	°C
Storage Temperature	-55	125	°C
Reflow Peak Temperature / Time	—	260 / 10sec.	°C
Maximum Power Dissipation @+25°C	—	2.5	W

## Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
<b>T<sub>a</sub></b>	Ambient Temperature		-20	25	70	°C
<b>V<sub>DD</sub></b>	Power Supply voltage		3.0	3.3	3.6	V
<b>F<sub>clk</sub></b>	Dual-in / Dual-out	Input	20	—	85	MHz
		Output	20	—	85	MHz
	Distribution	Input	20	—	85	MHz
		Output	20	—	85	MHz
	Single-in / Dual-out	Input	40	—	85	MHz
		Output	20	—	42.5	MHz
	Dual-in / Single-out	Input	20	—	42.5	MHz
		Output	40	—	85	MHz

## Power Dissipation

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I <sub>ccw</sub>	Operating Current (Worst Case Pattern) Fig1	Dual-in/Dual-out	CLKIN=40MHz	R <sub>L,TX</sub> = 100Ω CL=5pF RS=V <sub>DD</sub> Fig2	—	—	265	mA
			CLKIN=65MHz		—	—	305	mA
			CLKIN=75MHz		—	—	325	mA
			CLKIN=85MHz		—	—	340	mA
		Distribution	CLKIN=40MHz		—	—	215	mA
			CLKIN=65MHz		—	—	235	mA
			CLKIN=75MHz		—	—	245	mA
			CLKIN=85MHz		—	—	260	mA
		Single-in/Dual-out	CLKIN=40MHz		—	—	175	mA
			CLKIN=65MHz		—	—	190	mA
			CLKIN=75MHz		—	—	200	mA
			CLKIN=85MHz		—	—	210	mA
		Dual-in/Single-out	CLKIN=20MHz		—	—	215	mA
			CLKIN=32.5MHz		—	—	235	mA
			CLKIN=37.5MHz		—	—	245	mA
			CLKIN=42.5MHz		—	—	260	mA
I <sub>ccs</sub>	Power Down Current	—	—	—	—	8	mA	

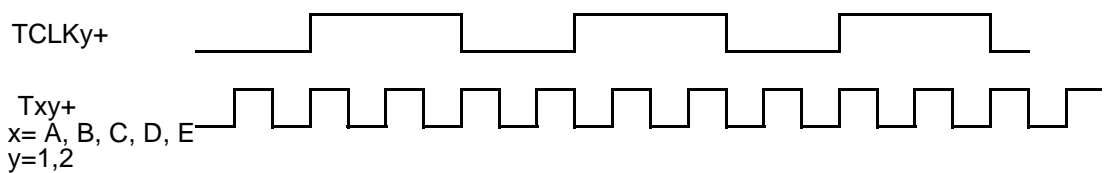
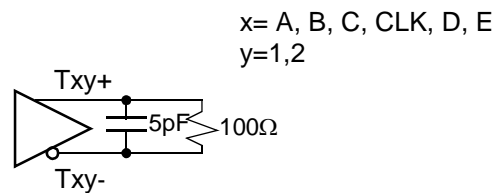


Fig1. Test Pattern (LVDS Output Full Toggle Pattern)



LVDS Output Load

Fig2. LVDS Output Load

## Electrical Characteristics

### THC63LVD1027 DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>cap</sub>	Capacitor pin appearance voltage	C <sub>CAP</sub> = 0.1μF	—	1.8	—	V
V <sub>IL_TTL</sub>	LV-TTL Input Low Voltage	—	GND	—	0.8	
V <sub>IH_TTL</sub>	LV-TTL Input High Voltage	—	2.0	—	VDD	
I <sub>IN_TTL</sub>	LV-TTL Input Leakage Current	—	-4	—	+4	μA

### LVDS Receiver DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>IN_RX</sub>	LVDS-Rx Input voltage range	—	0.3	—	2.1	V
V <sub>IC_RX</sub>	LVDS-Rx Common voltage	—	0.6	1.2	1.8	
V <sub>TH_RX</sub>	LVDS-Rx differential High threshold	V <sub>IC_RX</sub> = 1.2V	—	—	+100	mV
V <sub>TL_RX</sub>	LVDS-Rx differential Low threshold		-100	—	—	
V <sub>ID_RX</sub>	LVDS-Rx differential Input Voltage	—	100	—	600	
I <sub>IN_RX</sub>	LVDS-Rx Input Leakage current	—	-0.3	—	0.3	mA

### LVDS Transmitter DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units		
V <sub>OC_TX</sub>	LVDS-Tx Common voltage	—	1.125	1.25	1.375	V		
ΔV <sub>OC_TX</sub>	Change in VOC between complementary output states	—	—	—	35	mV		
V <sub>OD_TX</sub>	LVDS-Tx differential Output Voltage	R <sub>L_TX</sub> = 100Ω	Normal swing	250	350	450	mV	
			Reduced swing	100	200	300		
ΔV <sub>OD_TX</sub>	Change in VOD between complementary output states		—	—	—	35	mV	
I <sub>OS_TX</sub>	LVDS-Tx Output Short current		V <sub>out</sub> = GND	-24	—	—	mA	
I <sub>OZ_TX</sub>	LVDS-Tx Output Tri-state current		PD=GND	V <sub>out</sub> = GND to V <sub>cc</sub>	-10	—	+10	uA



### THC63LVD1027 AC Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{LT}$	Phase Lock Loop Set Time (Fig.3)	—	—	—	—	10	ms
$t_{DL}$	Data Latency (Fig.4)	Dual-in/Dual-out	CLKIN=75MHz	$9t_{RCP}+3$	$9t_{RCP}+5$	$9t_{RCP}+7$	ns
		Distribution	CLKIN=75MHz	$9t_{RCP}+3$	$9t_{RCP}+5$	$9t_{RCP}+7$	
		Single-in/Dual-out	CLKIN=75MHz	$(11+2/7)t_{RCP}+3$	$(11+2/7)t_{RCP}+5$	$(11+2/7)t_{RCP}+7$	
		Dual-in/Single-out	CLKIN=37.5MHz	$(8+5/14)t_{RCP}+3$	$(8+5/14)t_{RCP}+5$	$(8+5/14)t_{RCP}+7$	
$t_{DEH}$	DE input High time (Fig.5)	Single-in/ Dual-out	—	$2t_{RCP}$	—	—	ns
$t_{DEL}$	DE input Low time (Fig.5)		—	$2t_{RCP}$	—	—	
$t_{DEINT}$	DE input Period (Fig.5)		—	$4t_{RCP}$	Must be $2nt_{RCP}$ (n=integer)	—	

### AC Timing Diagrams

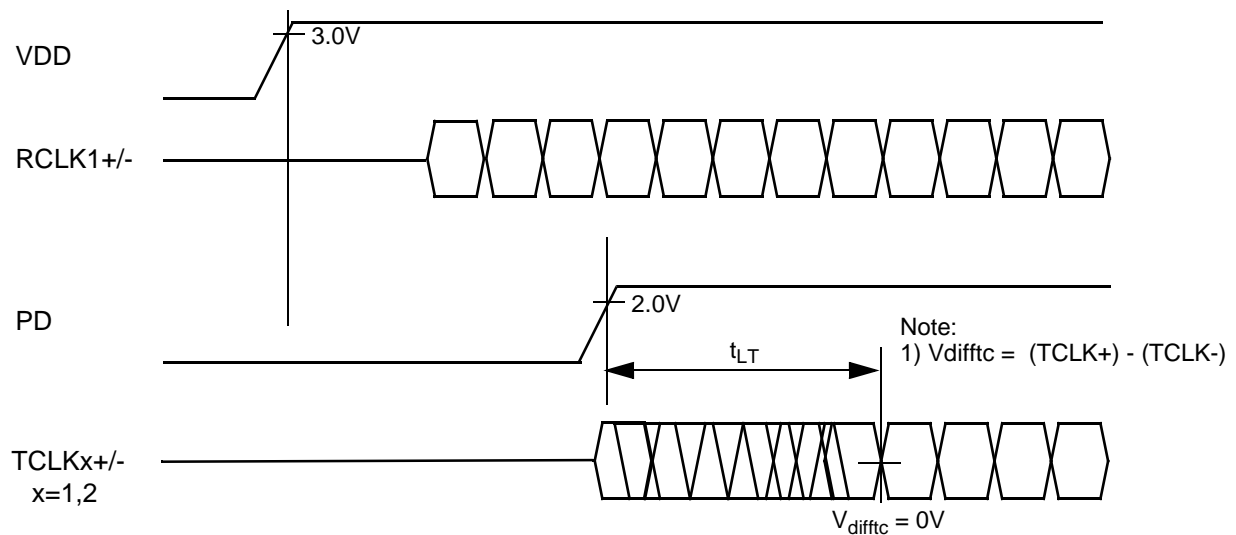


Fig.3. Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

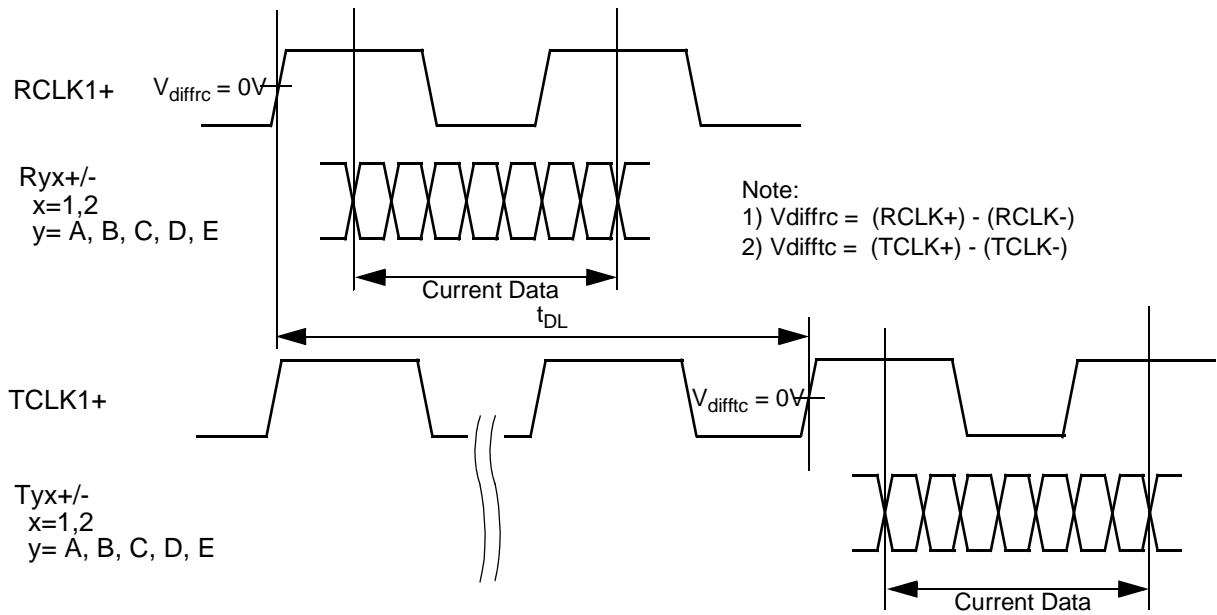


Fig.4. DATA Latency

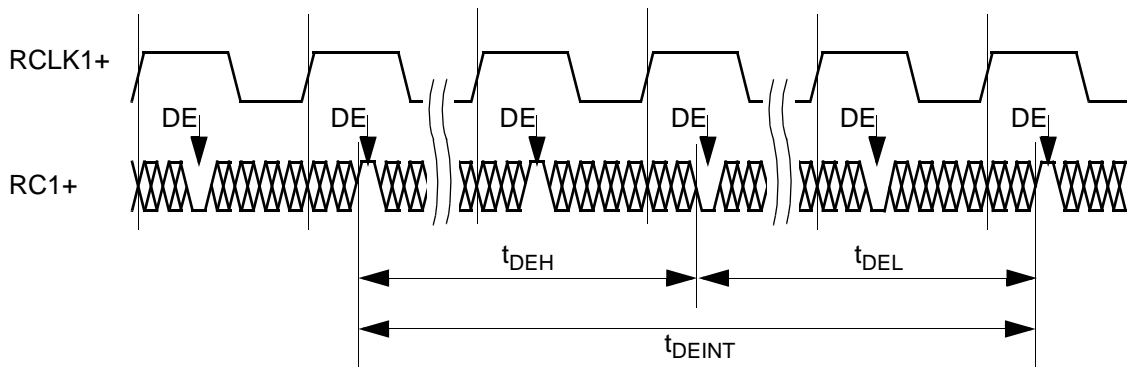
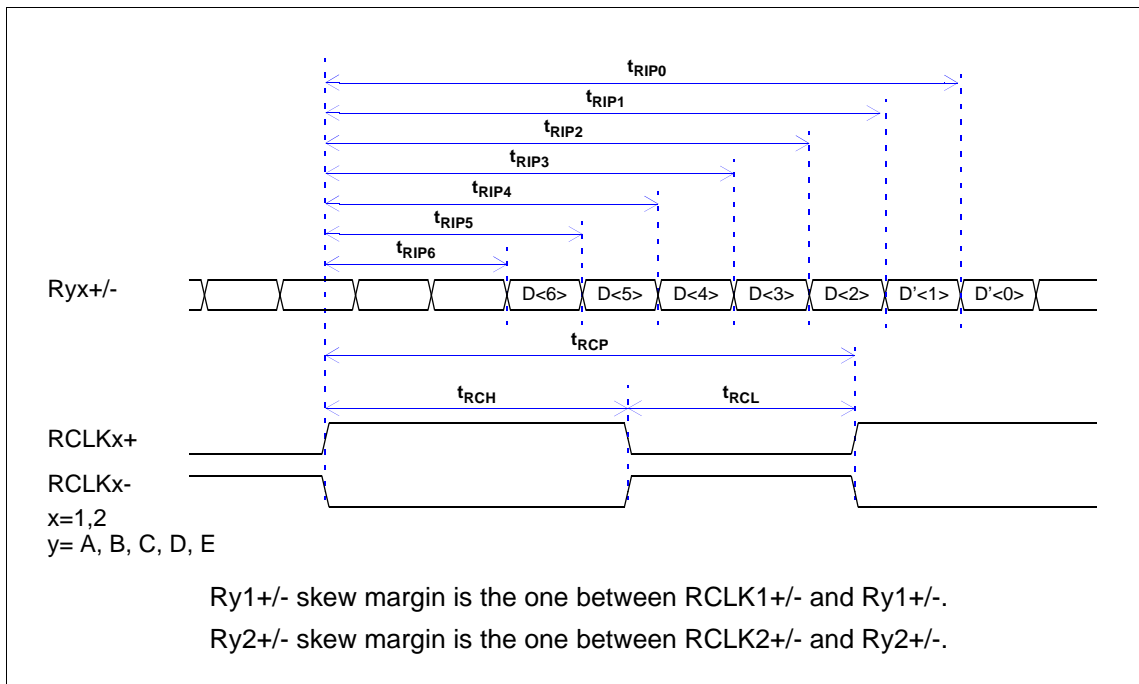


Fig.5. Single link input / Dual link output mode RC1(DE) input timing

### LVDS Receiver AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RCP}$	LVDS Clock Period	—	11.76	—	50	ns
$t_{RCH}$	LVDS Clock High duration	—	$2/7 t_{RCP}$	$4/7 t_{RCP}$	$5/7 t_{RCP}$	
$t_{RCL}$	LVDS Clock Low duration	—	$2/7 t_{RCP}$	$3/7 t_{RCP}$	$5/7 t_{RCP}$	
$t_{RSUP}$	LVDS data input setup margin	CLKIN=75MHz	480	—	—	ps
$t_{RHLD}$	LVDS data input hold margin	CLKIN=75MHz	480	—	—	
$t_{RIP6}$	LVDS data input position 6	—	$2/7 t_{RCP} - t_{RHLD}$	$2/7 t_{RCP}$	$2/7 t_{RCP} + t_{RSUP}$	ps
$t_{RIP5}$	LVDS data input position 5	—	$3/7 t_{RCP} - t_{RHLD}$	$3/7 t_{RCP}$	$3/7 t_{RCP} + t_{RSUP}$	
$t_{RIP4}$	LVDS data input position 4	—	$4/7 t_{RCP} - t_{RHLD}$	$4/7 t_{RCP}$	$4/7 t_{RCP} + t_{RSUP}$	
$t_{RIP3}$	LVDS data input position 3	—	$5/7 t_{RCP} - t_{RHLD}$	$5/7 t_{RCP}$	$5/7 t_{RCP} + t_{RSUP}$	
$t_{RIP2}$	LVDS data input position 2	—	$6/7 t_{RCP} - t_{RHLD}$	$6/7 t_{RCP}$	$6/7 t_{RCP} + t_{RSUP}$	
$t_{RIP1}$	LVDS data input position 1	—	$7/7 t_{RCP} - t_{RHLD}$	$7/7 t_{RCP}$	$7/7 t_{RCP} + t_{RSUP}$	
$t_{RIP0}$	LVDS data input position 0	—	$8/7 t_{RCP} - t_{RHLD}$	$8/7 t_{RCP}$	$8/7 t_{RCP} + t_{RSUP}$	
$t_{CK12}$	Skew Time between RCLK1 and RCLK2 (Fig.6)	—	$-0.3 t_{RCP}$	—	$0.3 t_{RCP}$	ps

### LVDS Receiver Input Timing



LVDS Receiver Input Timing (Continued)

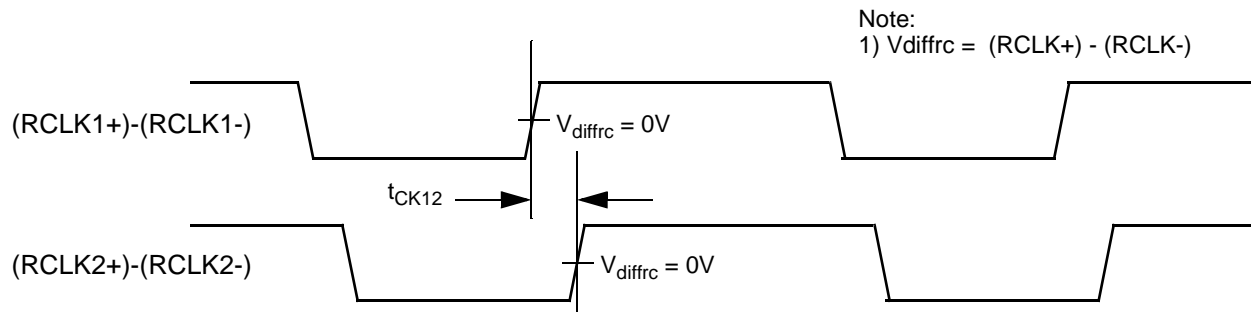


Fig.6. Skew Time between RCLK1 and RCLK2

### LVDS Transmitter AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{TCP}$	LVDS Clock Period	—	11.76	—	50	ns
$t_{TCH}$	LVDS Clock High duration	—	—	$4/7 t_{TCP}$	—	
$t_{TCL}$	LVDS Clock Low duration	—	—	$3/7 t_{TCP}$	—	
$t_{TSUP}$	LVDS data output setup	CLKOUT=75MHz	—	—	250	ps
$t_{THLD}$	LVDS data output hold	CLKOUT=75MHz	—	—	250	
$t_{TOP6}$	LVDS data output position 6	—	$2/7 t_{TCP} - t_{THLD}$	$2/7 t_{TCP}$	$2/7 t_{TCP} + t_{TSUP}$	ps
$t_{TOP5}$	LVDS data output position 5	—	$3/7 t_{TCP} - t_{THLD}$	$3/7 t_{TCP}$	$3/7 t_{TCP} + t_{TSUP}$	
$t_{TOP4}$	LVDS data output position 4	—	$4/7 t_{TCP} - t_{THLD}$	$4/7 t_{TCP}$	$4/7 t_{TCP} + t_{TSUP}$	
$t_{TOP3}$	LVDS data output position 3	—	$5/7 t_{TCP} - t_{THLD}$	$5/7 t_{TCP}$	$5/7 t_{TCP} + t_{TSUP}$	
$t_{TOP2}$	LVDS data output position 2	—	$6/7 t_{TCP} - t_{THLD}$	$6/7 t_{TCP}$	$6/7 t_{TCP} + t_{TSUP}$	
$t_{TOP1}$	LVDS data output position 1	—	$7/7 t_{TCP} - t_{THLD}$	$7/7 t_{TCP}$	$7/7 t_{TCP} + t_{TSUP}$	
$t_{TOP0}$	LVDS data output position 0	—	$8/7 t_{TCP} - t_{THLD}$	$8/7 t_{TCP}$	$8/7 t_{TCP} + t_{TSUP}$	
$t_{LVT}$	LVDS Transition Time (Fig7)	—	—	0.6	1.5	ns

### LVDS Transmitter Output Timing

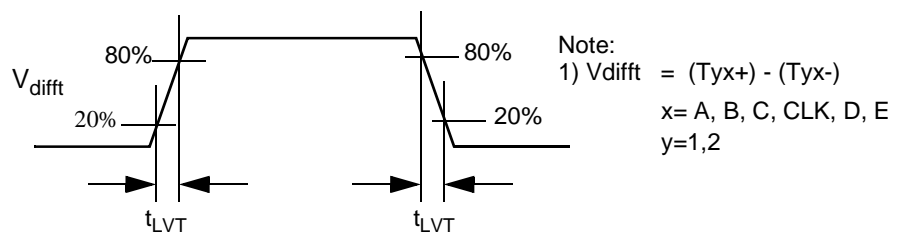
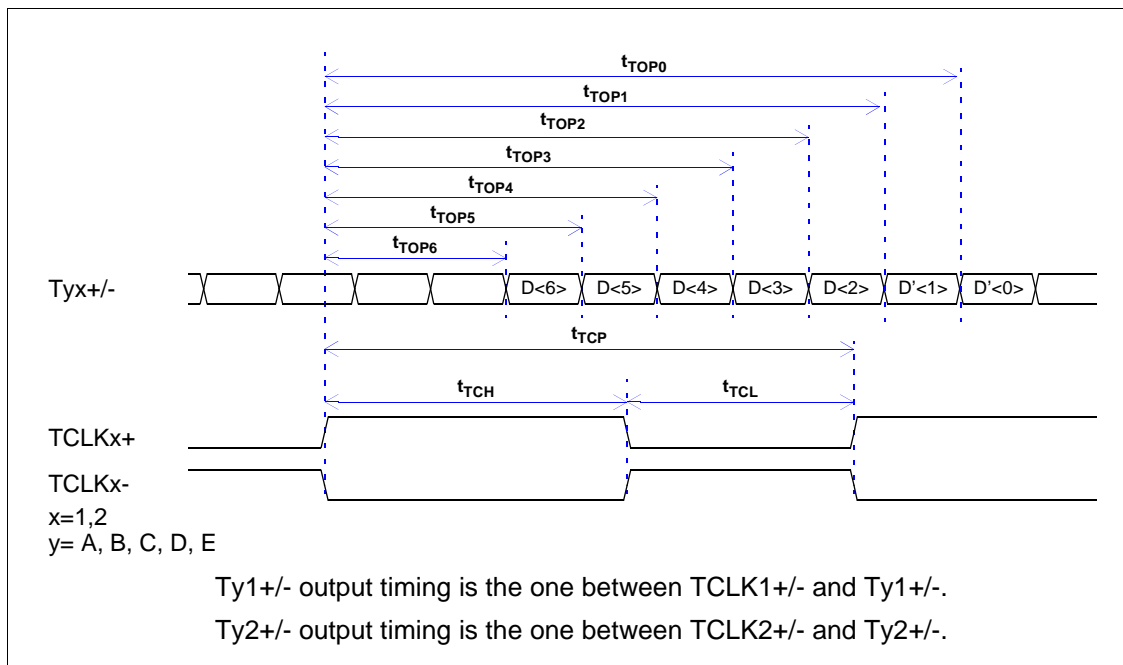
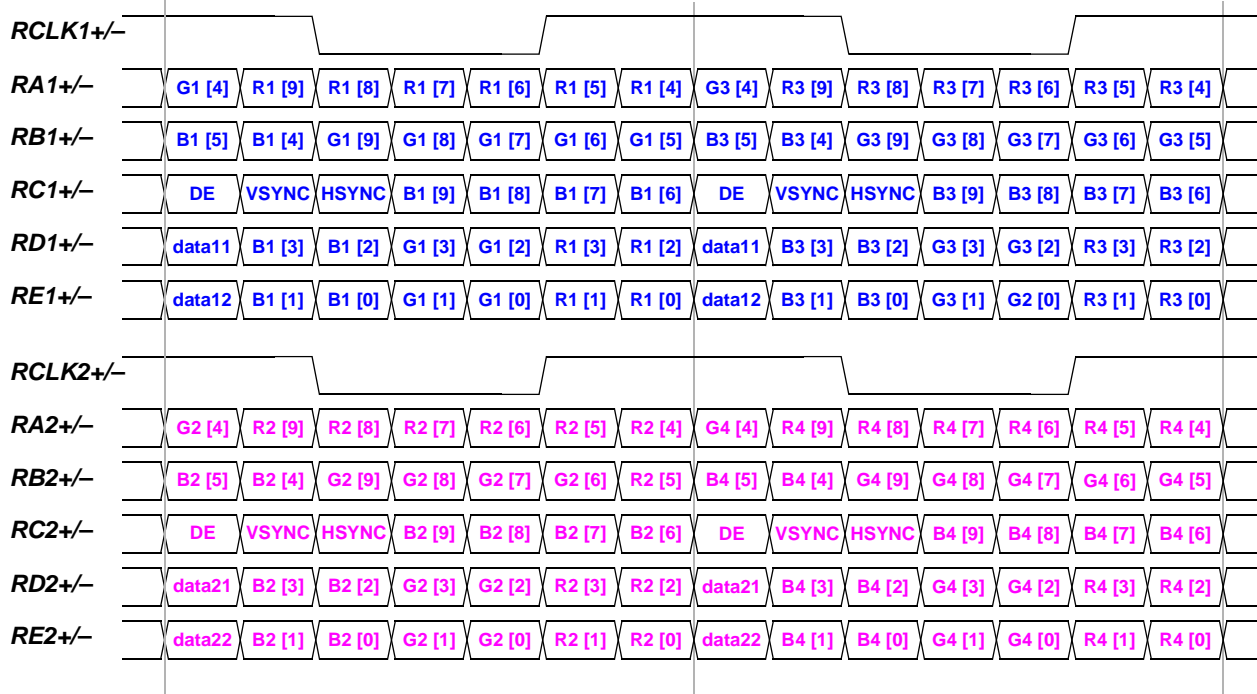


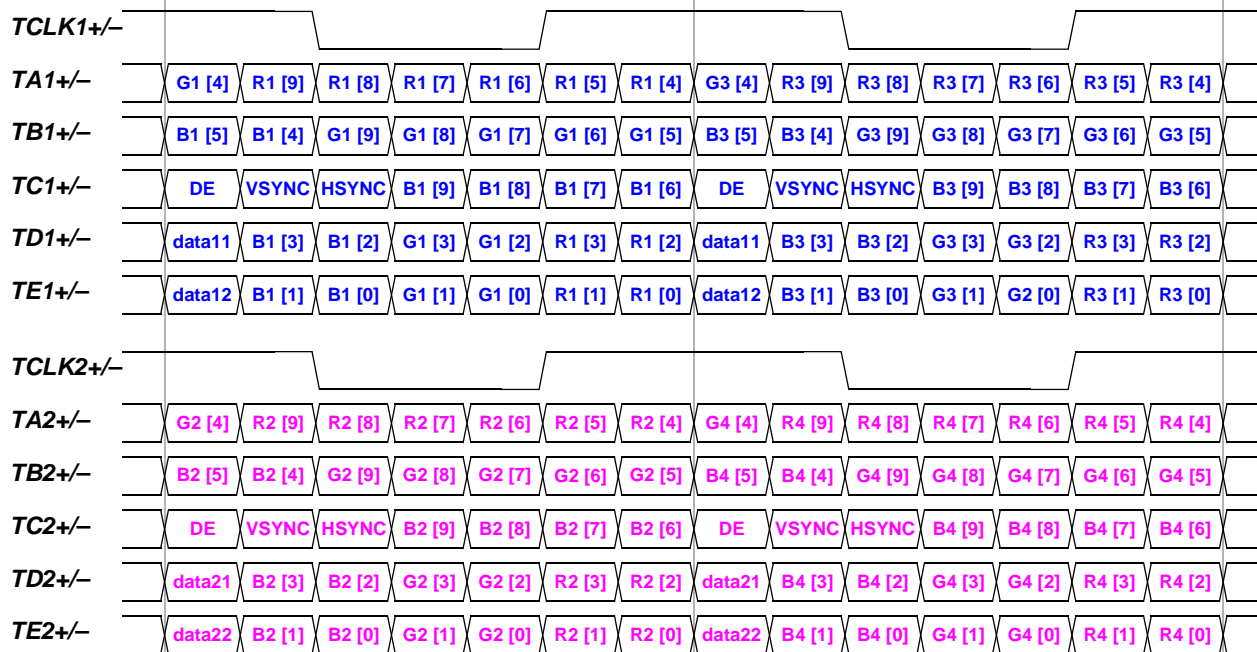
Fig7. LVDS Transition Time

## LVDS Data Mapping Dual-in / Dual-out mode

### LVDS-Rx Input Mapping



### LVDS-Tx Output Mapping



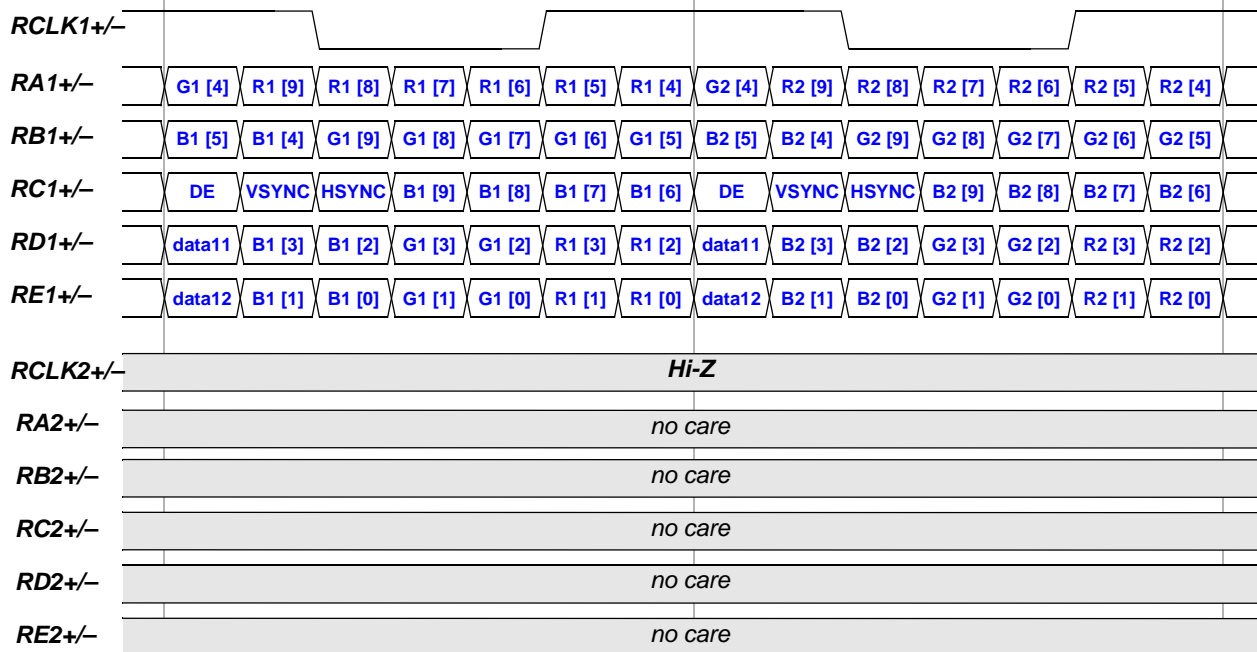
( Regardless of the Data Latency )

Data bits "data11, data12, data21, data22" are available for additional data transmission.

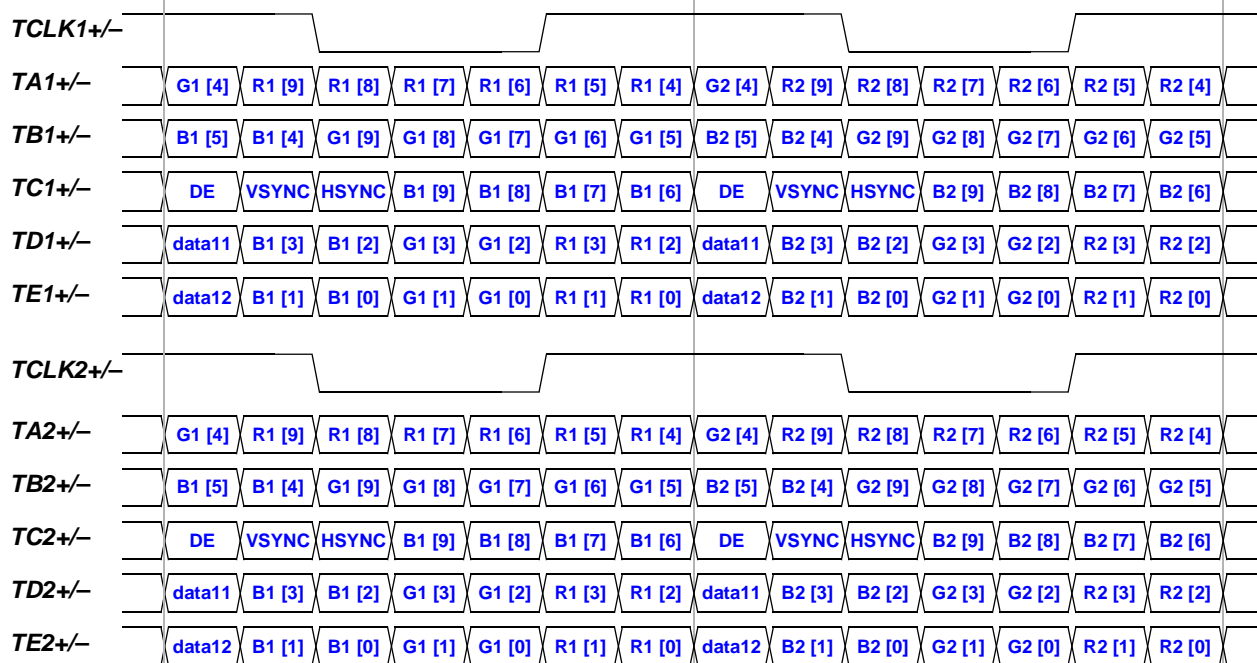
## Distribution Mode

In Distribution mode, RCLK2+/- must be High-Z.

### LVDS-Rx Input Mapping



### LVDS-Tx Output Mapping



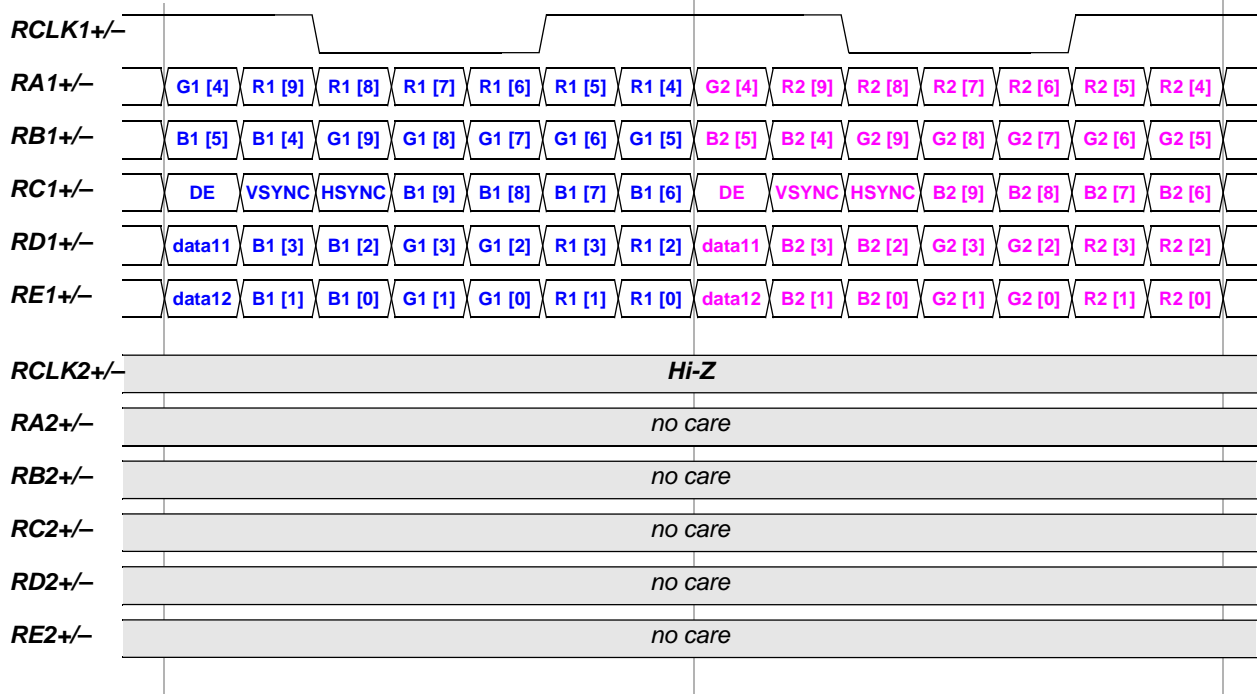
(Regardless of the Data Latency)

Data bits "data11, data12" are available for additional data transmission.

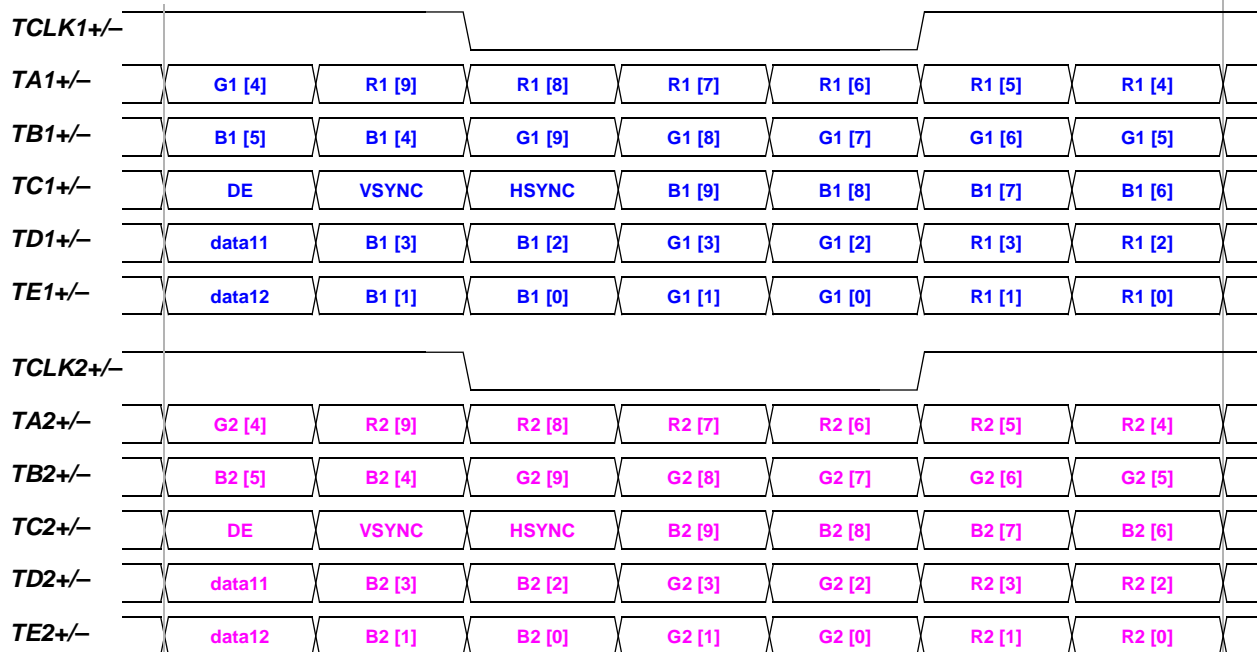
### Single-in / Dual-out mode

In Single-in / Dual-out mode, RCLK2+/- must be High-Z.

#### LVDS-Rx Input Mapping



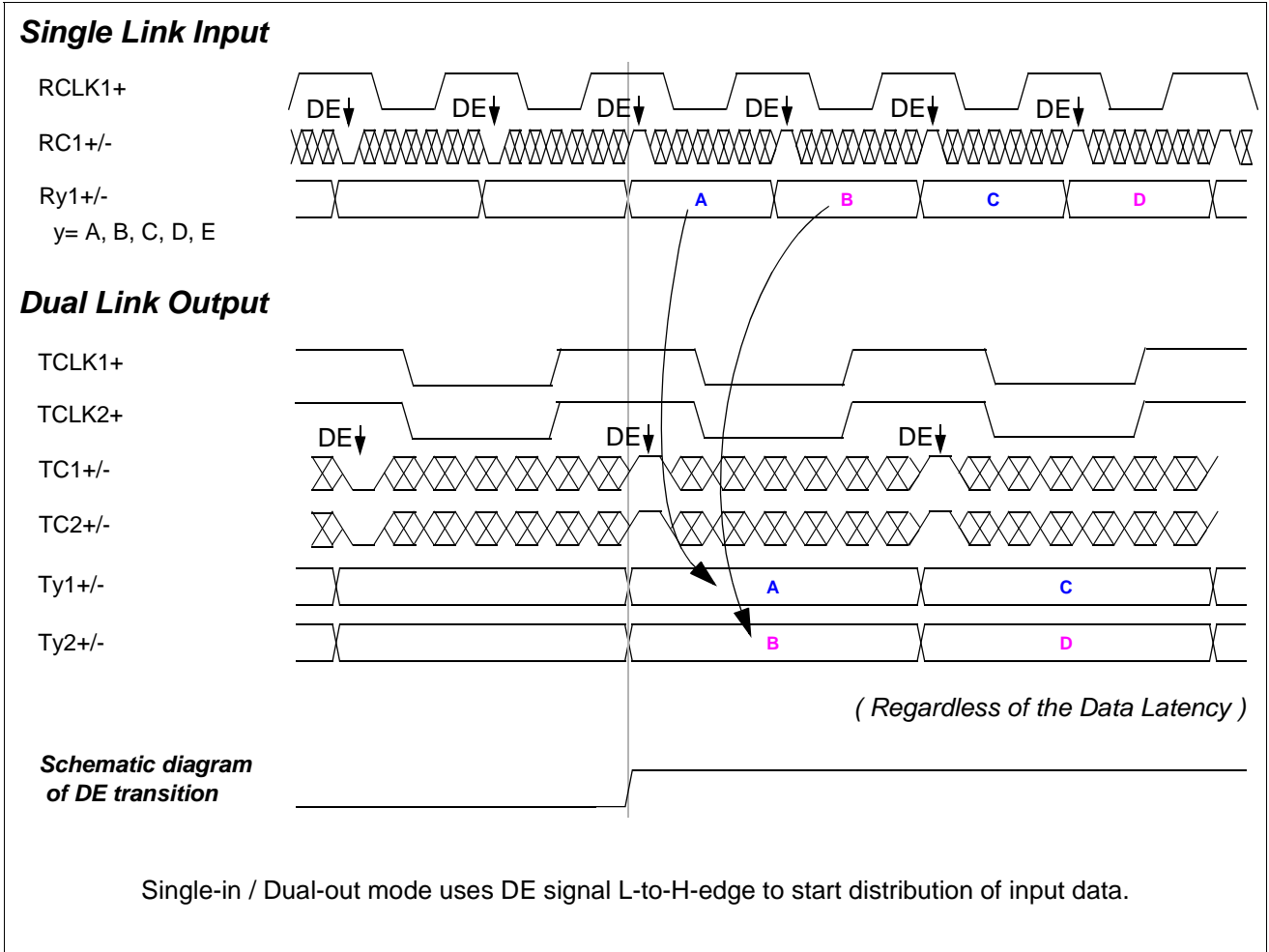
#### LVDS-Tx Output Mapping



( Regardless of the Data Latency )

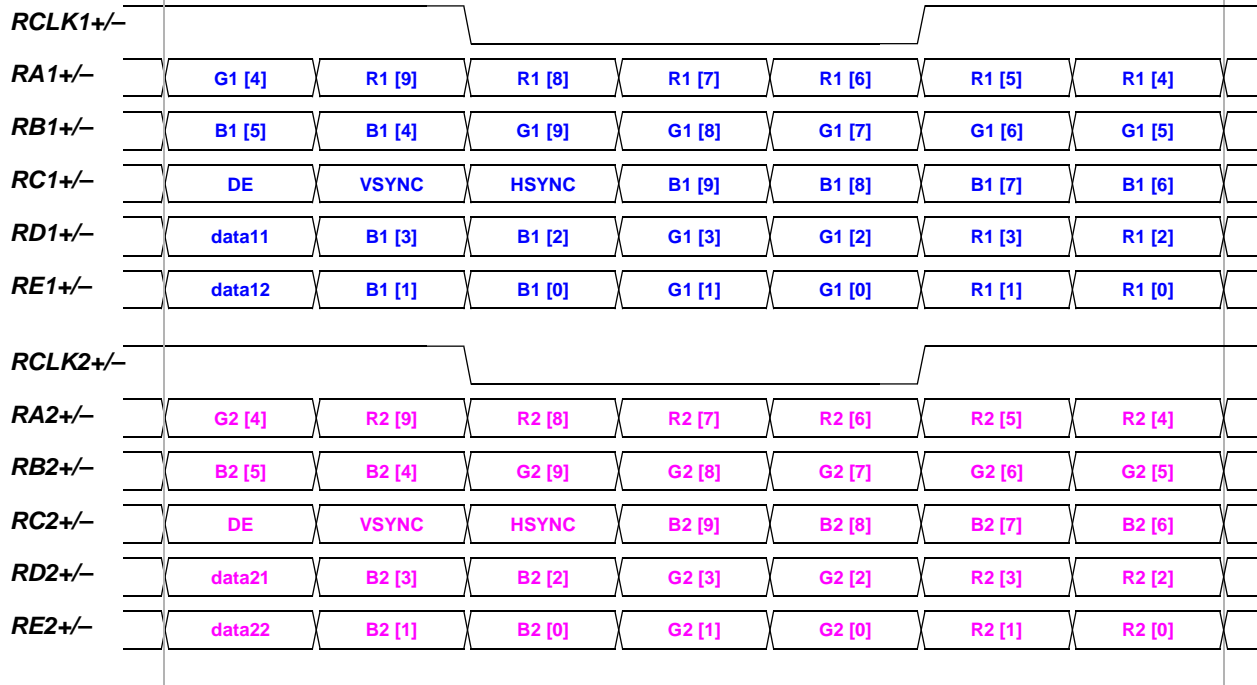
Data bits "data11, data12" are available for additional data transmission.



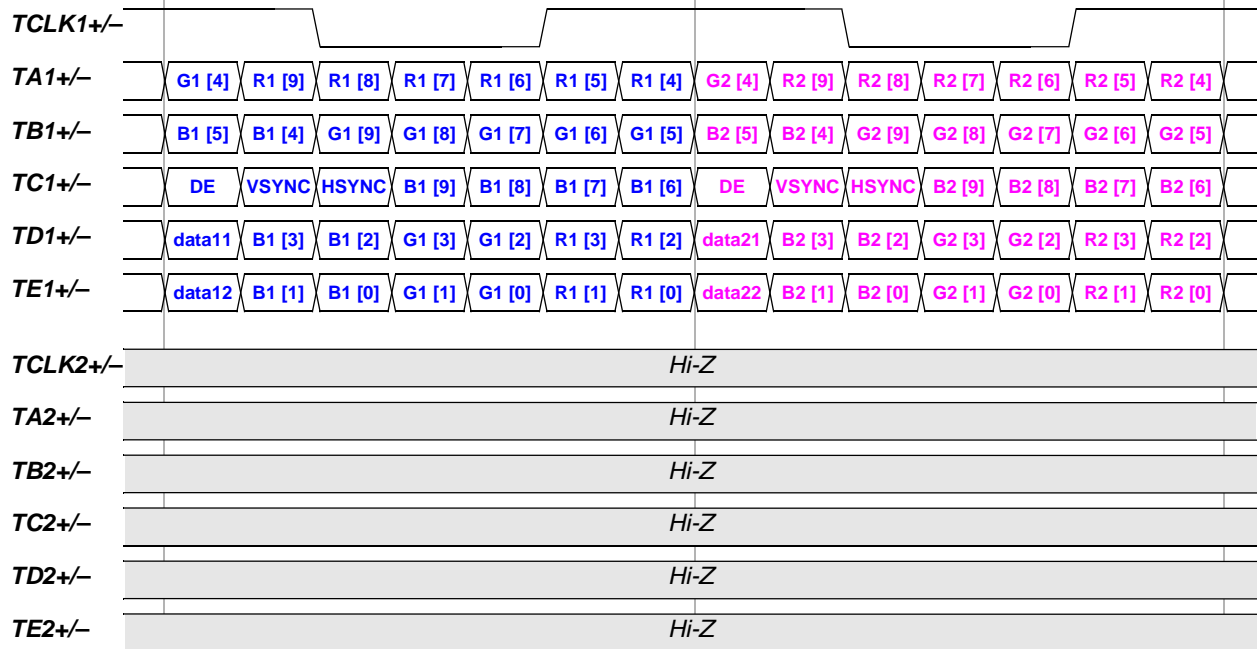


## Dual-in / Single-out mode

### LVDS-Rx Input Mapping



### LVDS-Tx Output Mapping



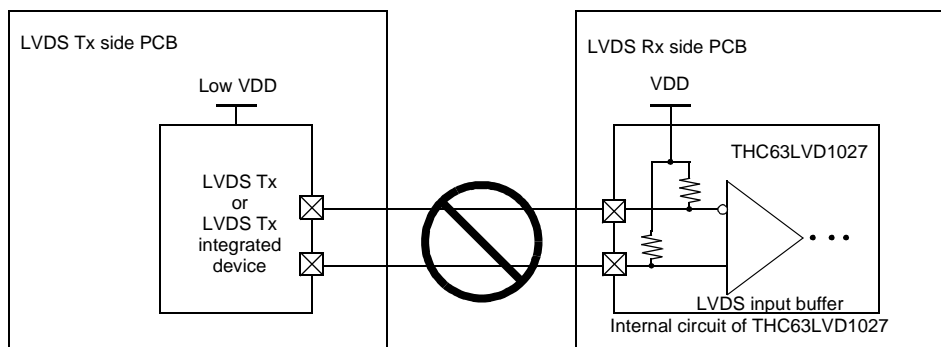
( Regardless of the Data Latency )

Data bits "data11, data12, data21, data22" are available for additional data transmission.

Note

1) LVDS input pin connection

When LVDS line is not driven from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.



2) Power On Sequence

Don't input RCLK#+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.

### 3)Cable Connection and Disconnection

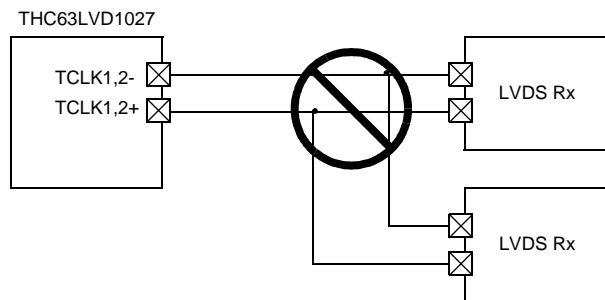
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

### 4)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

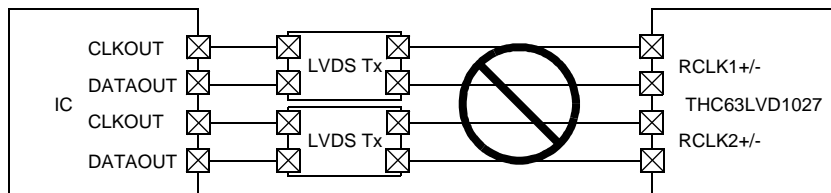
### 5)Multi Drop Connection

Multi drop connection is not recommended.

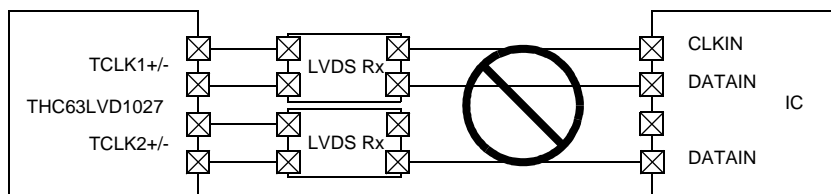


### 6)Asynchronous use

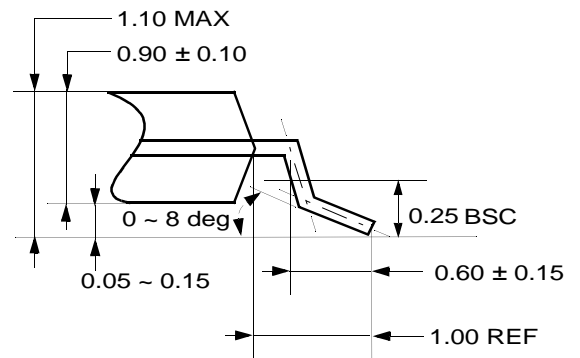
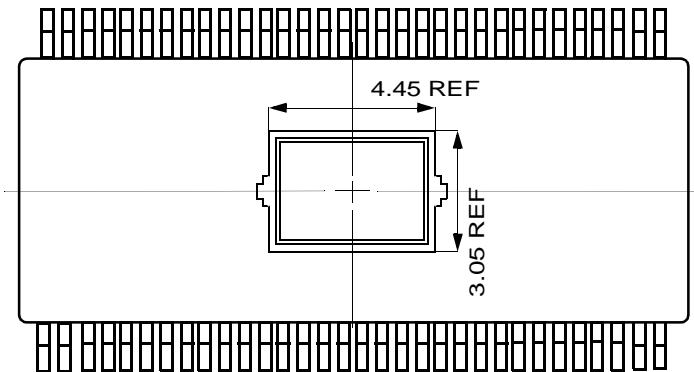
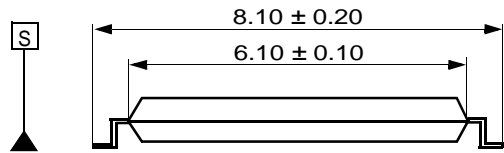
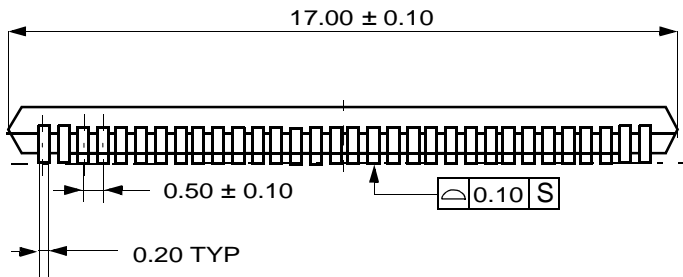
Asynchronous use such as following systems are not recommended. Page.11 tCK12 spec should be kept.



Asynchronous use such as following systems are not recommended.



Package



Detail of Lead End

Unit: mm

Exposed PAD is GND and must be soldered to PCB.

## Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copy right, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
4. Note that if infringement of any third party's industrial ownership should occur by using this product, we will be exempted from the responsibility unless it directly relates to the production process or functions of the product.
5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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