19-5967; Rev 0; 6/11

EVALUATION KIT AVAILABLE

MAX15118

High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

General Description

The MAX15118 high-efficiency, current-mode step-down regulator with integrated power switches operates from 2.7V to 5.5V and delivers up to 18A of output current in a small 2mm x 3.5mm package. The MAX15118 offers excellent efficiency with skip mode capability at light-load conditions, yet provides unmatched efficiency under heavy load conditions. The combination of small size and high efficiency makes this device suitable for both portable and nonportable applications.

The MAX15118 utilizes a current-mode control architecture with a high-gain transconductance error amplifier, which allows a simple compensation scheme and enables a cycle-by-cycle current limit with fast response to line and load transients. A factory-trimmed switching frequency of 1MHz (PWM operation) allows for a compact, all-ceramic capacitor design.

Integrated switches with low on-resistance ensure high efficiency at heavy loads while minimizing critical inductances. The MAX15118's simple layout and footprint assure first-pass success in new designs.

Other features of the MAX15118 include a capacitor-programmable soft-start to reduce inrush current, safe startup into a prebiased output, an enable input, and a power-good output for power sequencing.

The regulator is available in a 28-bump (4 x 7), 2.10mm x 3.56mm WLP package, and is fully specified over the -40°C to +85°C extended temperature range.

Features

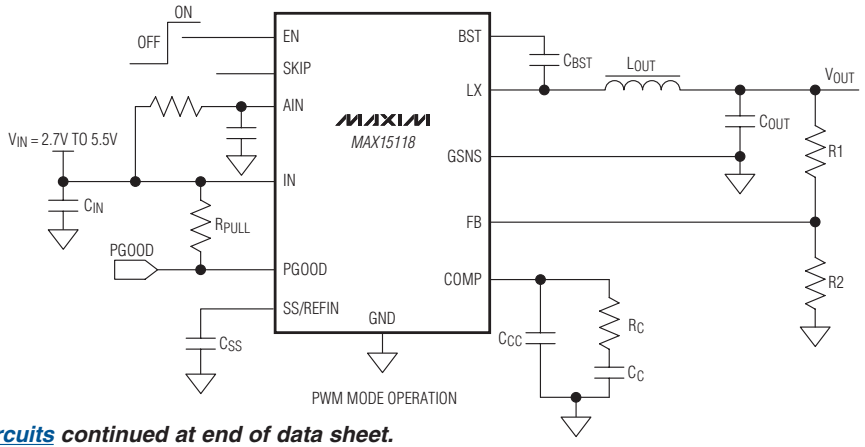
- **Continuous 18A Output Current Over Temperature**
- **±1% Feedback Accuracy Over Load, Line, and Temperature**
- **Operates from 2.7V to 5.5V Supply**
- **Input Undervoltage Lockout**
- **Adjustable Output Range from 0.6V Up to 0.94 x V_{IN}**
- **Programmable Soft-Start**
- **Factory-Trimmed 1MHz Switching Frequency**
- **Stable with Low-ESR Ceramic Output Capacitors**
- **Safe-Startup into a Prebiased Output**
- **External Reference Input**
- **Selectable Skip Mode Option for Improved Efficiency at Light Loads**
- **Enable Input/PGOOD Output Allows Sequencing**
- **Remote Ground Sense for Improved Accuracy**
- **Thermal and Overcurrent Protection**
- **Tiny 2.10mm x 3.56mm, 28-Bump WLP Package**

Applications

Notebooks
Servers
Distributed Power Systems
DDR Memory
Base Stations

***Ordering Information* appears at end of data sheet.**

Typical Operating Circuits



***Typical Operating Circuits* continued at end of data sheet.**

For related parts and recommended products to use with this part, refer to: ***www.maxim-ic.com/MAX15118.related***

ABSOLUTE MAXIMUM RATINGS

IN, PGOOD to GND .....-0.3V to +6V
EN, COMP, FB, SS/REFIN, GSNS, SKIP, LX to GND .....-0.3V to (V_{IN} + 0.3V)
LX to GND (for 50ns).....-1V to (V_{IN} + 1V)
LX to GND (for 10ns).....-2V to (V_{IN} + 2V)
BST to LX.....-0.3V to +6V
BST to GND.....-0.3V to +12V
BST to IN .....-0.3V to +6V
LX Continuous Current (Note 1)..... ±20A
Output Short-Circuit Duration .....Continuous
Continuous Power Dissipation
WLP (derate 81.53mW/°C above +70°C).....3.26W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature (Note 2) .....+110°C
Storage Temperature Range..... -65°C to +150°C
Bump Reflow Temperature (Note 3) .....+260°C

Note 1: LX has internal clamp diodes to GND and IN. Applications that forward bias these diodes must take care not to exceed the IC's package power dissipation limits.

Note 2: Limit the junction temperature to +110°C for continuous operation at maximum output current.

Note 3: The WLP package is constructed using a unique set of package techniques that impose a limit on the thermal profile. The device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, see the *Typical Operating Circuits*, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		2.7		5.5	V
IN Supply Current	I_{IN}	V_{EN} = V_{IN}, V_{FB} = 0.65V, no switching		4.8	7	mA
IN Shutdown Current	I_{SHDN}	V_{EN} = 0V		0.01	3	µA
IN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising, LX starts switching		2.6	2.68	V
IN Undervoltage Lockout Threshold Hysteresis		V_{IN} falling, LX stops switching		200		mV
ERROR AMPLIFIER						
Transconductance	g_M			1.2		mS
Voltage Gain	A_{VEA}			90		dB
FB Setpoint Voltage	V_{FB}	Over line, load, and temperature	0.594	0.600	0.606	V
FB Input Bias Current	I_{FB}		-500		+500	nA
COMP to Current-Sense Transconductance	g_{MC}			150		A/V
COMP Clamp Low Voltage		V_{FB} = 0.65V, $V_{SS/REFIN}$ = 0.6V		0.97		V
Slope Compensation Ramp Amplitude	V_{SLOPE}			130		mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, see the *Typical Operating Circuits*, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GROUND SENSE						
GSNS Output Current		$V_{SS/REFIN}$ = 0.6V, V_{GSNS} = 0V		56		µA
POWER SWITCHES						
Current-Limit Threshold		High-side switch		30		A
		Low-side switch, sinking		30		
		Low-side switch, sourcing		30		
LX Leakage Current		V_{EN} = 0V			3	µA
BST Leakage Current		V_{EN} = 0V			3	µA
BST On-Resistance	R_{ON_BST}	I_{BST} = 50mA		0.63		Ω
LX RMS Output Current			18			A
OSCILLATOR						
Switching Frequency	f_{SW}		850	1000	1150	kHz
Maximum Duty Cycle	D_{MAX}	PWM mode		94		%
		Skip mode		85		
Minimum Controllable On-Time	t_{ON}			70		ns
ENABLE FUNCTIONALITY						
EN Input High Threshold	V_{IH}	V_{EN} rising			1.4	V
EN Input Low Threshold	V_{IL}	V_{EN} falling	0.4			V
EN Input Leakage Current			-1		+1	µA
SKIP FUNCTIONALITY (Note 5)						
SKIP Input High Threshold		V_{SKIP} rising			1.4	V
SKIP Input Low Threshold		V_{SKIP} falling	0.4			V
SKIP Pulldown Resistor				210		kΩ
Minimum LX On-Current in Skip Mode				3.6		A
Zero-Crossing LX Threshold				0.5		A
SOFT-START AND PREBIAS FUNCTIONALITY						
Soft-Start Current	I_{SS}	$V_{SS/REFIN}$ = 0.45V, sourcing	6.8	10	12.5	µA
SS/REFIN Discharge Resistance	R_{SS}	$I_{SS/REFIN}$ = 10mA, sinking		7		Ω
SS/REFIN Prebias Mode Stop Voltage		$V_{SS/REFIN}$ rising		0.58		V
SS/REFIN External Reference Input Range					V_{IN} - 2.5	V
HICCUP MODE						
Number of Consecutive Current-Limit Events to Hiccup Mode	N_{HIC}			8		Events
Hiccup Mode Timeout				1024		Clock Cycles

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, see the *Typical Operating Circuits*, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

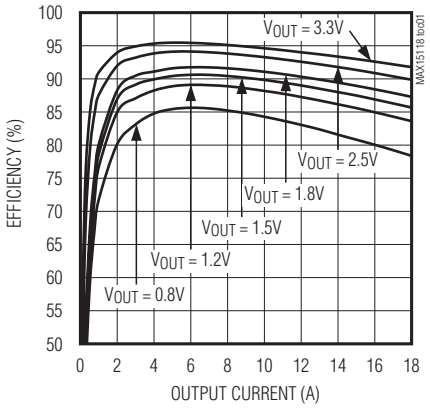
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-GOOD OUTPUT						
PGOOD Threshold		V_{FB} falling, PGOOD deasserts	0.514	0.530	0.542	V
PGOOD Threshold Hysteresis		V_{FB} rising		25		mV
PGOOD Output Voltage Low	V_{PG_OL}	I_{PGOOD} = 5mA, V_{EN} = 0V		18	50	mV
PGOOD Leakage Current	I_{PG_LK}	V_{PGOOD} = 5.5V, V_{FB} = 0.65V			1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	Die temperature rising		+150		°C
Thermal Shutdown Hysteresis				20		°C

Note 4: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 5: Connect SKIP to EN for skip mode functionality. Connect SKIP to GND for PWM mode functionality.

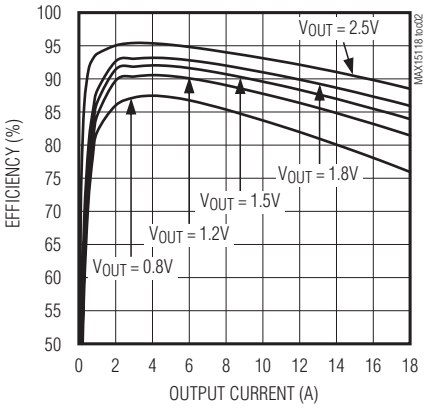
Typical Operating Characteristics

(V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS} = 0.1µF, see the *Typical Operating Circuits*, T_A = +25°C, unless otherwise noted.)

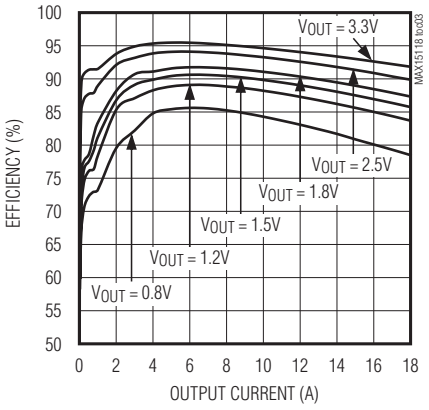
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 5V, PWM MODE)



EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 3.3V, PWM MODE)



EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 5V, SKIP MODE)

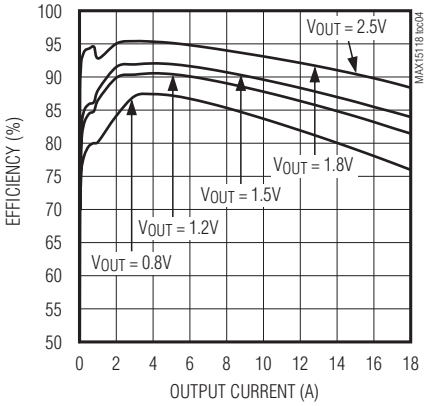


High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

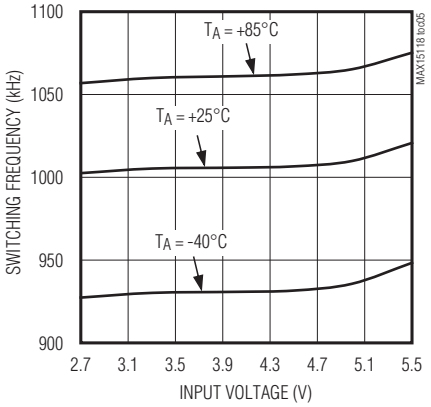
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS} = 0.1µF, see the *Typical Operating Circuits*, T_A = +25°C, unless otherwise noted.)

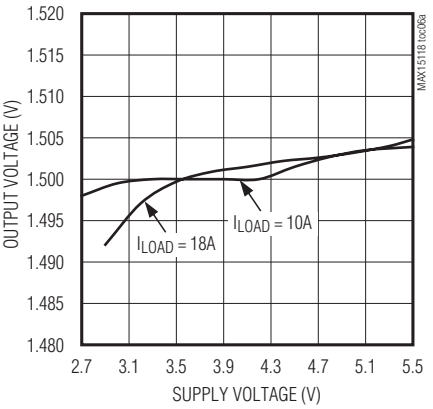
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 3.3V, SKIP MODE)



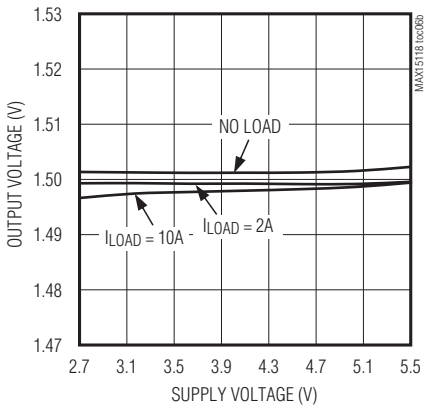
SWITCHING FREQUENCY vs. INPUT VOLTAGE



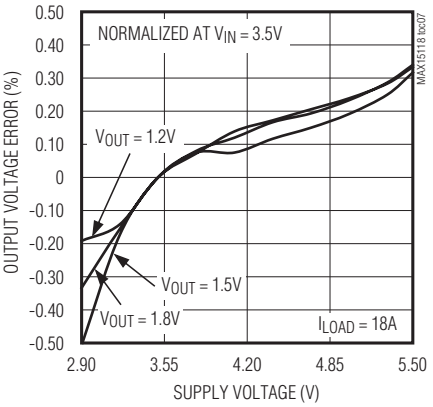
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (PWM MODE, V_{OUT} = 1.5V)



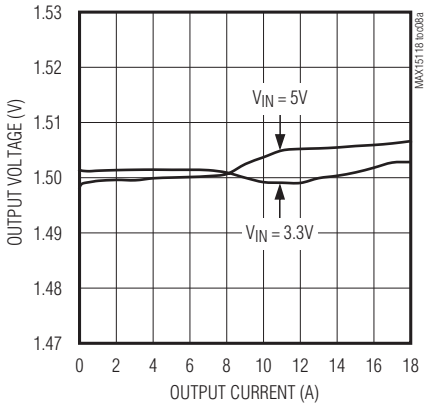
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE (SKIP MODE, V_{OUT} = 1.5V)



OUTPUT VOLTAGE ERROR vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE vs. OUTPUT CURRENT (PWM MODE, V_{OUT} = 1.5V)

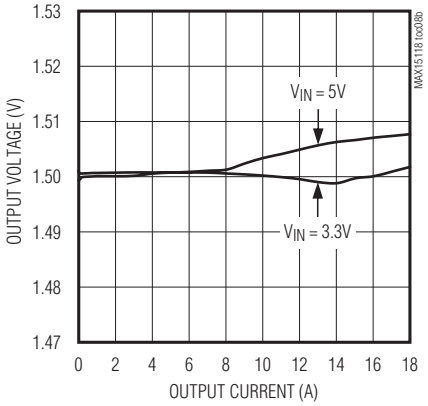


High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

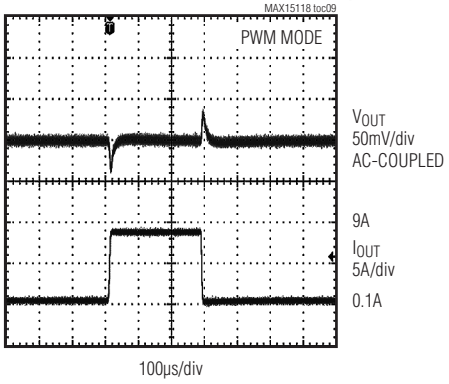
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS} = 0.1µF, see the *Typical Operating Circuits*, T_A = +25°C, unless otherwise noted.)

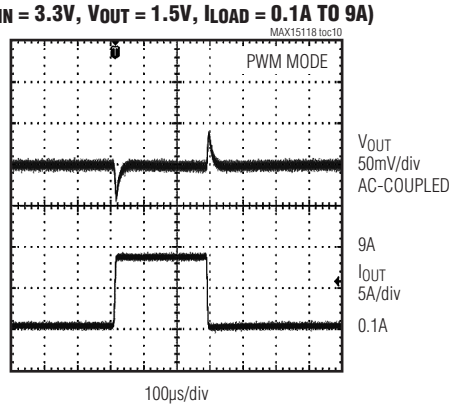
OUTPUT VOLTAGE vs. OUTPUT CURRENT (SKIP MODE, V_{OUT} = 1.5V)



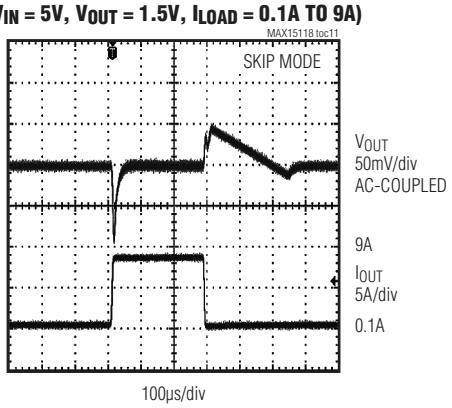
LOAD-TRANSIENT RESPONSE (V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 0.1A TO 9A)



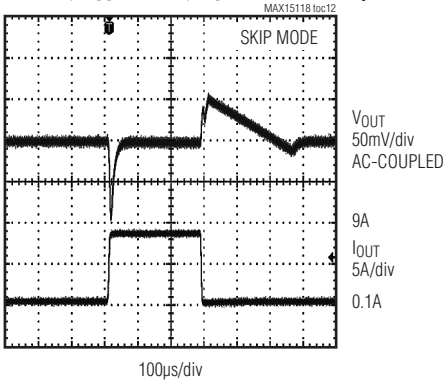
LOAD-TRANSIENT RESPONSE (V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{LOAD} = 0.1A TO 9A)



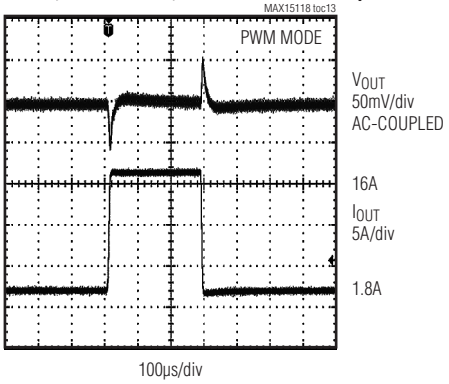
LOAD-TRANSIENT RESPONSE (V_{IN} = 5V, V_{OUT} = 1.5V, I_{LOAD} = 0.1A TO 9A)



LOAD-TRANSIENT RESPONSE (V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{LOAD} = 0.1A TO 9A)



LOAD-TRANSIENT RESPONSE (V_{IN} = 5V, V_{OUT} = 1.5V, I_{LOAD} = 1.8A TO 16A)

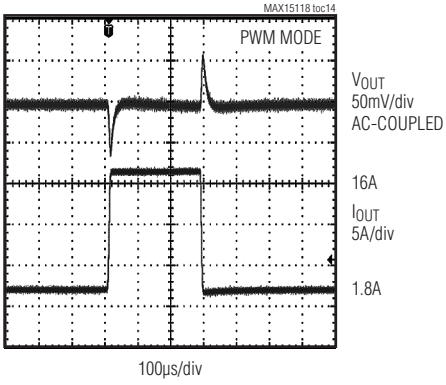


High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

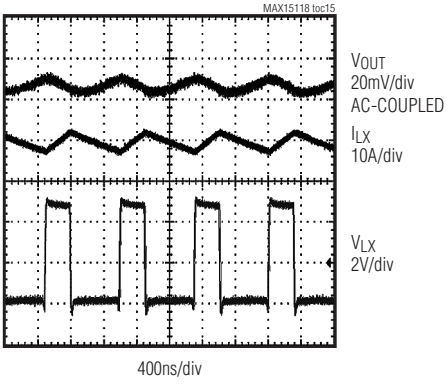
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS} = 0.1µF, see the *Typical Operating Circuits*, T_A = +25°C, unless otherwise noted.)

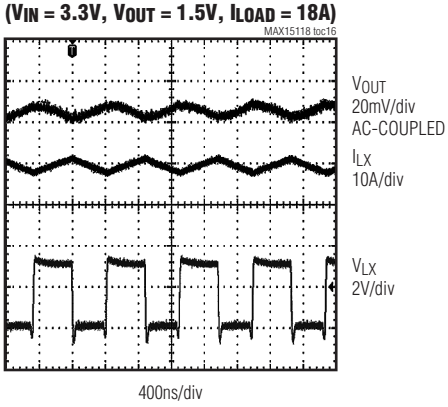
LOAD-TRANSIENT RESPONSE
(V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{LOAD} = 1.8A TO 16A)



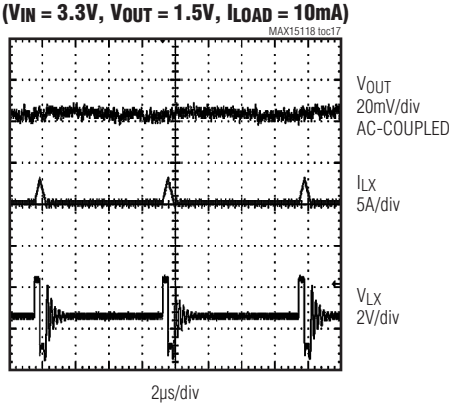
SWITCHING WAVEFORMS
(V_{IN} = 5V, V_{OUT} = 1.5V, I_{LOAD} = 1.8A)



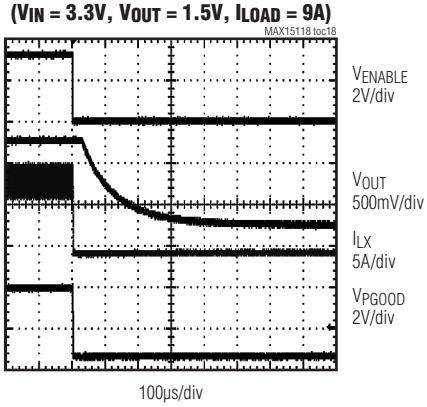
SWITCHING WAVEFORMS
(V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{LOAD} = 18A)



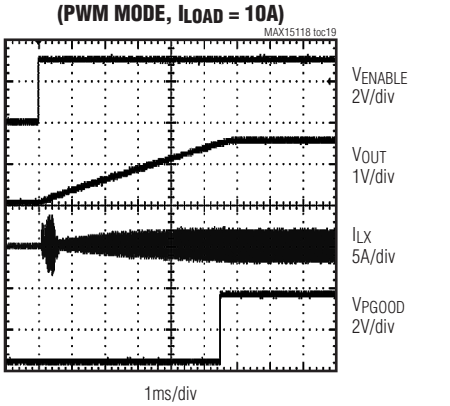
SWITCHING WAVEFORMS IN SKIP MODE
(V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{LOAD} = 10mA)



SHUTDOWN WAVEFORMS
(V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{LOAD} = 9A)



SOFT-START WAVEFORMS
(PWM MODE, I_{LOAD} = 10A)

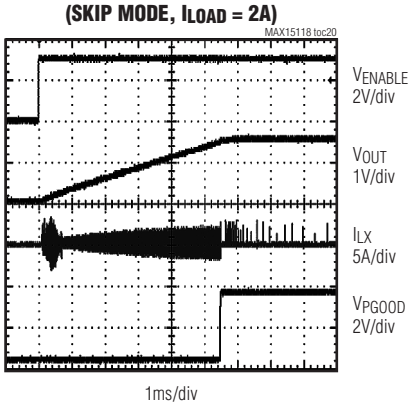


High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

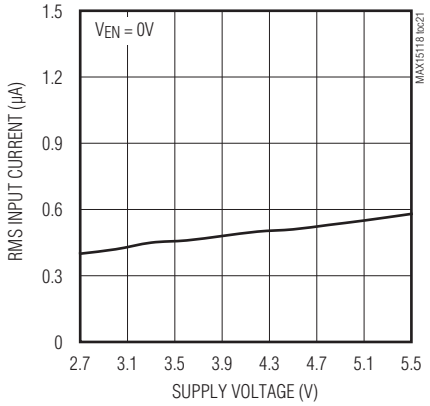
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS} = 0.1µF, see the *Typical Operating Circuits*, T_A = +25°C, unless otherwise noted.)

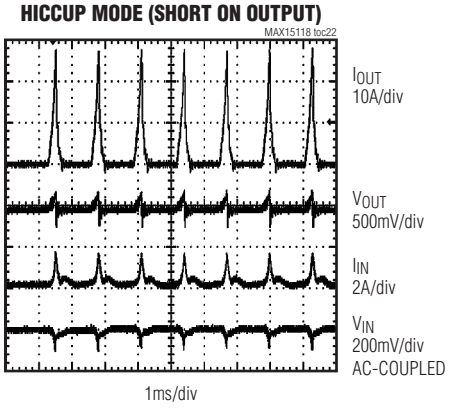
SOFT-START WAVEFORMS (SKIP MODE, I_{LOAD} = 2A)



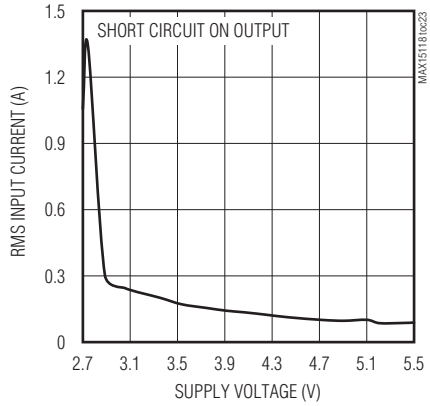
QUIESCENT CURRENT (SHUTDOWN)



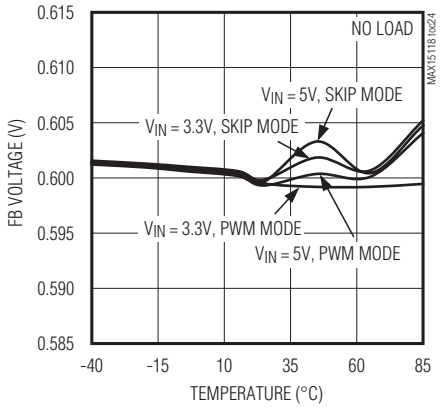
HICCUP MODE (SHORT ON OUTPUT)



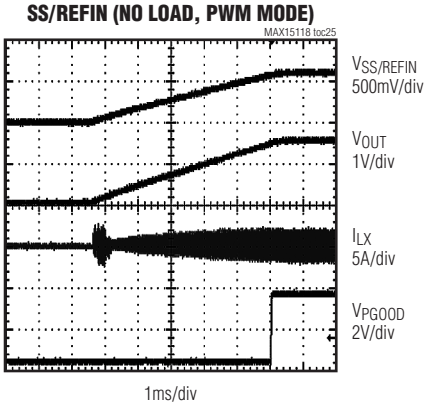
RMS INPUT CURRENT vs. SUPPLY VOLTAGE



FB VOLTAGE vs. TEMPERATURE (V_{OUT} = 1.5V)



SOFT-START WAVEFORMS WITH SS/REFIN (NO LOAD, PWM MODE)

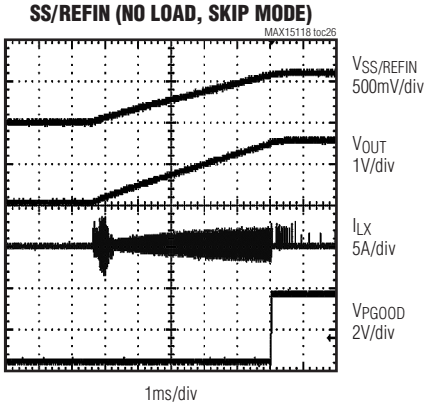


High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

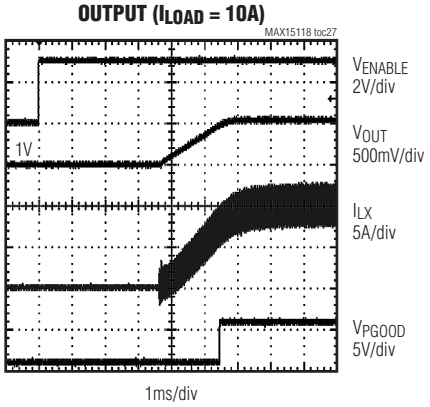
Typical Operating Characteristics (continued)

(V_{IN} = 5V, V_{OUT} = 1.5V, C_{SS} = 0.1µF, see the *Typical Operating Circuits*, T_A = +25°C, unless otherwise noted.)

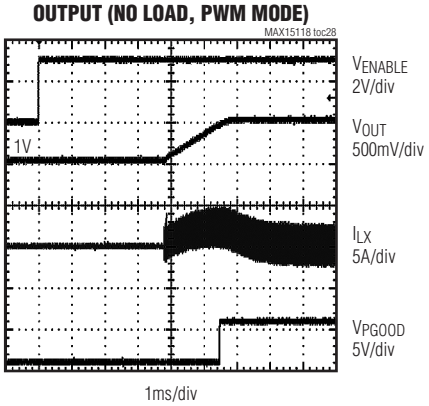
SOFT-START WAVEFORMS WITH SS/REFIN (NO LOAD, SKIP MODE)



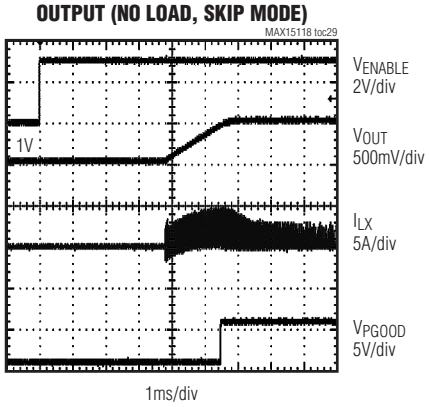
STARTING INTO A 1V PREBIASED OUTPUT (I_{LOAD} = 10A)



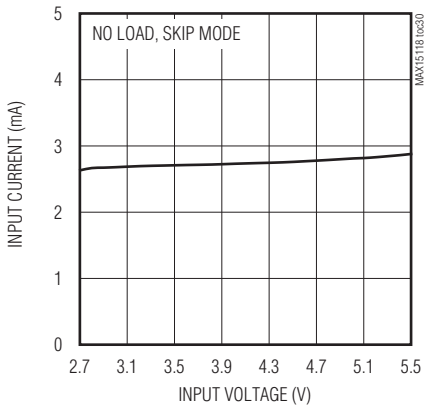
STARTING INTO A 1V PREBIASED OUTPUT (NO LOAD, PWM MODE)



STARTING INTO A 1V PREBIASED OUTPUT (NO LOAD, SKIP MODE)

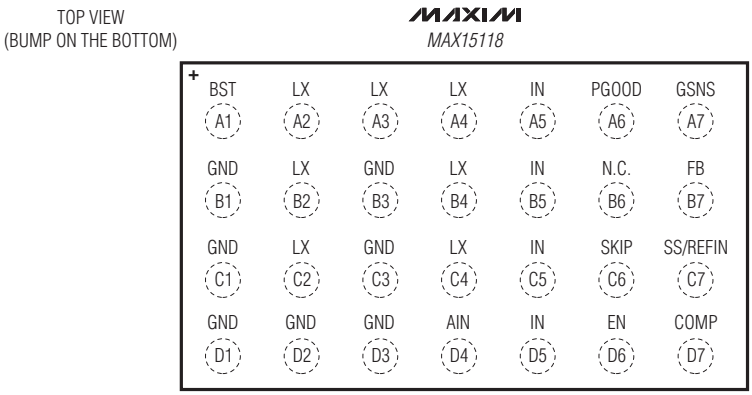


INPUT CURRENT vs. INPUT VOLTAGE



High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

Pin Configuration



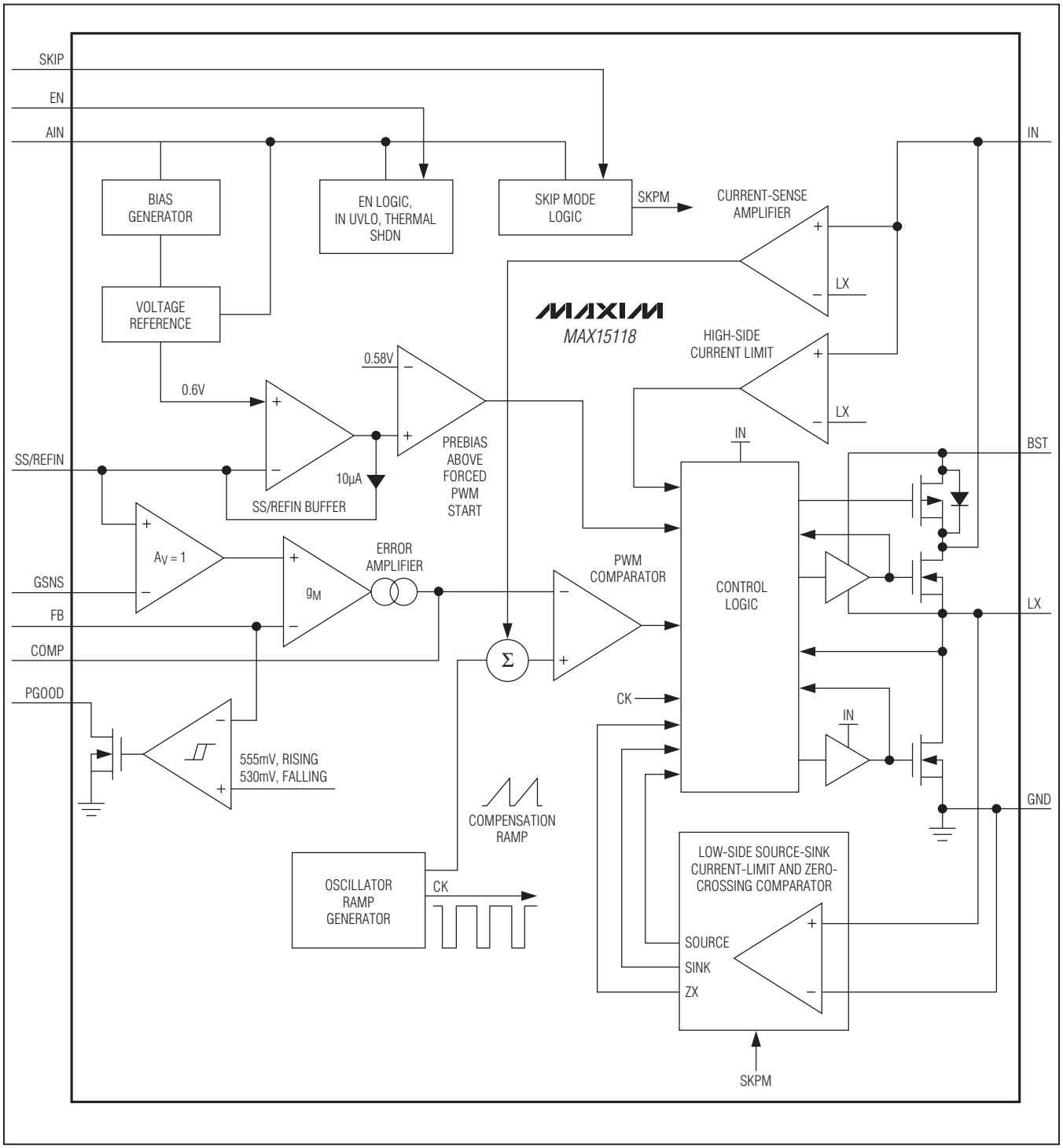
WLP

Pin Description

PIN	NAME	FUNCTION
A1	BST	Boost Input for the High-Side Switch Driver. Connect a capacitor from BST to LX.
A2, A3, A4, B2, B4, C2, C4	LX	Inductor Connection. Connect LX to the switching side of the inductor. LX is high impedance when the MAX15118 is in shutdown mode.
A5, B5, C5, D5	IN	Input Power Supply. Bypass IN to GND with at least two 22µF low-ESR ceramic capacitors with sufficient ripple current ratings.
A6	PGOOD	Power-Good Open-Drain Output. PGOOD asserts high when V_{FB} is above 0.555V (typ) and deasserts when V_{FB} falls below 0.530V (typ).
A7	GSNS	Remote Ground-Sense Input. Connect GSNS to the ground terminal of the load and to the bottom of the feedback resistors.
B1, B3, C1, C3, D1, D2, D3	GND	Ground Connection. GND is the source terminal of the internal low-side switch. Connect all GND bumps to a component-side PCB copper ground plane at a single point near the input bypass capacitor return terminal.
B6	N.C.	No Connection. Do not connect.
B7	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to the output capacitor return terminal to set the output voltage from 0.6V to 0.94 x V_{IN}.
C6	SKIP	Skip Mode Selector Input. Connect SKIP to EN for skip mode operation. Connect SKIP to GND or leave unconnected for continuous mode operation. Do not change the state of SKIP when EN is high.
C7	SS/REFIN	Soft-Start and External Voltage Reference Input. Connect a capacitor from SS/REFIN to GND to set the soft-start delay. See the *Setting the Soft-Start Time* section for more information. To use SS/REFIN as an external voltage reference, apply a voltage ranging from 0V to (V_{IN} - 2.5V) to SS/REFIN to externally control the soft-start time and feedback voltage.
D4	AIN	Filtered Input Voltage
D6	EN	Enable Input. Drive EN high to enable the MAX15118. Connect EN to IN for always-on operation.
D7	COMP	Error Amplifier Output. Connect the compensation network from COMP to GND. See the *Compensation Design Guidelines* section for more information.

High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

Functional Diagram



Detailed Description

The MAX15118 high-efficiency, current-mode switching regulator delivers up to 18A of output current. The regulator provides output voltages from 0.6V up to 0.94 x V_{IN} from 2.7V to 5.5V input supplies, making the device ideal for on-board point-of-load applications.

The MAX15118 delivers current-mode control architecture using a high-gain transconductance error amplifier. The current-mode control architecture facilitates easy compensation design and ensures cycle-by-cycle current limit with fast response to line and load transients.

The regulator features a 1MHz fixed switching frequency, allowing for all-ceramic capacitor designs and fast transient responses. The high operating frequency minimizes the size of external components.

The regulator offers a selectable skip-mode functionality to reduce current consumption and achieve a higher efficiency at light output loads. Integrated switches ensure high efficiency at heavy loads while minimizing critical inductances.

The MAX15118 features PWM current-mode control, allowing for an all-ceramic capacitor solution. The regulator offers capacitor-programmable soft-start to reduce input inrush current. The device safely starts up into a prebiased output. The MAX15118 includes an enable input and open-drain PGOOD output for sequencing with other devices.

Controller Function—PWM Logic

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The control logic block controls the break-before-make logic and all the necessary timing.

The high-side MOSFET turns on at the beginning of the oscillator cycle and turns off when the COMP voltage crosses the internal current-mode ramp waveform. The internal ramp is the sum of the compensation ramp and the current-mode ramp derived from the inductor current (current-sense block). The high-side MOSFET also turns off if either the maximum duty cycle (94%, typ) or the current limit is reached. The low-side MOSFET turns on for the remainder of the oscillation cycle.

Starting into a Prebiased Output

The MAX15118 can soft-start into a prebiased output without discharging the output capacitor. In safe prebiased startup, both low-side and high-side MOSFETs remain off to avoid discharging the prebiased output. PWM operation starts when the voltage on SS/REFIN crosses the voltage on FB.

The MAX15118 can start into a prebiased voltage higher than the nominal set point without abruptly discharging the output. Forced PWM operation starts when the SS/REFIN voltage reaches 0.58V (typ), forcing the converter to start. The low-side current limit is increased over 350µs to the maximum from the first LX pulse. When the low-side sink current-limit threshold of 30A is reached, the low-side switch turns off before the end of the clock period and the high-side switch turns on until one of the following conditions is satisfied:

- High-side source current hits the reduced high-side current limit (30A, typ); in this case, the high-side switch is turned off for the remaining time of the clock period.
- The clock period ends.

Reduced high-side current limit is activated to recirculate the current into the high-side power switch rather than into the internal high-side body diode

Low-side sink current limit is provided to protect the low-side switch from excessive reverse current during prebiased operation.

Enable Input and Power-Good (PGOOD) Output

The MAX15118 features independent enable control and a power-good signal that allows for flexible power sequencing. Drive the enable input (EN) high to enable the regulator, or connect EN to IN for always-on operation.

Power-good (PGOOD) is an open-drain output that asserts when V_{FB} is above 555mV (typ) and deasserts low if V_{FB} is below 530mV (typ).

Programmable Soft-Start (SS/REFIN)

The MAX15118 utilizes a soft-start feature to slowly ramp up the regulated output voltage to reduce input inrush current during startup. Connect a capacitor from SS/REFIN to GND to set the startup time (see the *Setting the Soft-Start Time* section for capacitor selection details).

Error Amplifier

A high-gain transconductance error amplifier provides accuracy for the voltage-feedback loop regulation. Connect the necessary compensation network between COMP and GND (see the *Compensation Design Guidelines* section). The error-amplifier transconductance is 1.2mS (typ). COMP clamp low is set to 0.97V (typ), just below the slope ramp compensation valley, helping COMP to rapidly return to the correct set point during load and line transients.

Ground-Sense Amplifier

The MAX15118 features a ground-sense amplifier to prevent output voltage droop under heavy load conditions. Connect GSNS to the negative terminal of the load output capacitor to properly Kelvin-sense the output ground. Route the GSNS trace away from the switching nodes.

PWM Comparator

The PWM comparator compares the COMP voltage to the current-derived ramp waveform (COMP voltage to LX current transconductance value is 150A/V, typ). To avoid instability due to subharmonic oscillations when the duty cycle is around 50% or higher, a slope compensation ramp is added to the current-derived ramp waveform. The compensation ramp slope is designed to ensure stable operation at any duty cycle up to 94%.

Overcurrent Protection and Hiccup Mode

When the converter output is shorted or the device is overloaded, each high-side MOSFET current-limit event turns off the high-side MOSFET and turns on the low-side MOSFET. On each current-limit event (either high-side or low-side) a 3-bit counter is incremented. The counter is reset after three consecutive switching cycles that do not reach the current limit. If the current-limit condition persists, the counter fills up reaching eight events. The control logic then keeps the low-side MOSFET turned on until the inductor current is fully discharged to avoid high currents circulating through the low-side body diode. The control logic turns off both high-side and low-side MOSFETs and waits for the hiccup period (1024 clock cycles, typ) before attempting a new soft-start sequence. The hiccup mode is also enabled during soft-start time.

Thermal Shutdown Protection

The MAX15118 contains an internal thermal sensor that limits the total power dissipation to protect the device in the event of an extended thermal fault condition. When the die temperature exceeds +150°C (typ), the thermal sensor shuts down the device, turning off the DC-DC converter to allow the die to cool. After the die temperature falls by 20°C (typ), the device restarts.

Skip Mode Operation

The MAX15118 features selectable skip mode operation when SKIP is connected to EN. When in skip mode, the LX output becomes high impedance when the inductor current falls below 0.5A (typ). The inductor current does not become negative. If during a clock cycle the inductor current falls below the 0.5A threshold (during off-time), the low-side turns off. At the next clock cycle, if the output voltage is above set point, the PWM logic keeps both high-side and low-side MOSFETs off. If instead the output voltage is below the set point, the PWM logic drives the high-side on until a reduced current limit threshold (3.6A, typ) is reached. In this way the system can skip cycles, reducing the frequency of operation, and switches only as needed to service load at the cost of an increase in output voltage ripple (see the *Skip Mode Frequency and Output Ripple* section). In skip mode, power dissipation is reduced and efficiency is improved at light loads because power MOSFETs do not switch at every clock cycle.

The MAX15118 automatically enters continuous mode regardless of the state of SKIP when the load current increases beyond the skip mode current limit.

Do not change the state of SKIP when EN is high.

Applications Information

Setting the Output Voltage

The MAX15118 output voltage is adjustable from 0.6V up to 94% of V_{IN} by connecting FB to the center tap of a resistor-divider between the output and GND (see the *Typical Operating Circuits*). Choose R1 and R2 values so that the DC errors due to the FB input bias current (±500nA) do not affect the output voltage accuracy. With lower value resistors, the DC error is reduced, but the amount of power consumed in the resistor-divider increases. R2 values between 1kΩ and 20kΩ are acceptable (see Table 1 for typical values). Once R2 is chosen, calculate R1 using:

$$R1 = R2 \times \left[(V_{OUT} / V_{FB}) - 1 \right]$$

where the feedback threshold voltage V_{FB} = 0.6V (typ). When regulating for an output of 0.6V in skip mode, short FB to OUT and keep R2 connected from FB to GND.

Inductor Selection

A high-valued inductor results in reduced inductor-ripple current, leading to a reduced output-ripple voltage. However, a high-valued inductor results in either a larger physical size or a high series resistance (DCR) and a lower saturation current rating. Typically, choose an inductor value to produce a current ripple, ΔI_L, equal to 30% of load current. Choose the inductor with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times LIR \times I_{LOAD}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where f_{SW} is the fixed 1MHz switching frequency, and LIR is the desired inductor current ratio (typically 0.3). In addition, the peak inductor current, I_{L_PK}, must always be below the high-side current-limit and the inductor saturation current rating, I_{L_SAT}. Ensure that the following relationship is satisfied:

$$I_{L\_PK} = I_{LOAD} + \frac{1}{2} \Delta I_{L(P-P)} < \min (24A, I_{L\_SAT})$$

where:

$$\Delta I_{L(P-P)} = \frac{(V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

Input Capacitor Selection

For a step-down converter, the input capacitor, C_{IN}, helps to keep the DC input voltage steady, in spite of discontinuous input AC current. Use low-ESR capacitors to minimize the voltage ripple due to ESR.

Size C_{IN} using the following formula:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

where ΔV_{IN_RIPPLE} is the maximum-allowed input-ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage, f_{SW} is the switching frequency (1MHz), and I_{LOAD} is the output load. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor.

Ensure that the input capacitor can accommodate the input-ripple current requirement imposed by the switching currents. The RMS input-ripple current is given by:

$$I_{RMS} = \left[\frac{\left[V_{OUT} \times (V_{IN} - V_{OUT}) \right]^{-1/2}}{V_{IN}} \right] \times I_{LOAD}$$

where I_{RMS} is the input RMS ripple current.

Use multiple capacitors in parallel to meet the RMS current rating requirement.

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output-ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output-voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESR)} = \Delta I_{P-P} \times ESR$$

and $V_{RIPPLE(ESL)}$ can be approximated as an inductive divider from LX to GND:

$$V_{RIPPLE\,(ESL)} = V_{LX} \times \frac{ESL}{L} = V_{IN} \times \frac{ESL}{L}$$

where V_{LX} swings from V_{IN} to GND.

The peak-to-peak inductor current (ΔI_{P-P}) is:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}}$$

When using ceramic capacitors, which generally have low-ESR, $\Delta V_{RIPPLE(C)}$ dominates. When using electrolytic capacitors, $\Delta V_{RIPPLE(ESR)}$ dominates. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

As a general rule, a smaller inductor ripple-current results in less output-ripple voltage. Since inductor-ripple current depends on the inductor value and input voltage, the output-ripple voltage decreases with larger inductance and increases with higher input voltages. However, the inductor-ripple current also impacts transient-response performance, especially at low V_{IN} to V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Load-transient response also depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to the predetermined value.

Use higher C_{OUT} values for applications that require light-load operation or transition between heavy load and light load, triggering skip mode, causing output undershooting or overshooting. When applying the load, limit the output undershooting by sizing C_{OUT} according to the following formula:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{3 f_{CO} \times \Delta V_{OUT}}$$

where ΔI_{LOAD} is the total load change, f_{CO} is the unity-gain bandwidth (or zero-crossing frequency), and ΔV_{OUT} is the desired output undershooting. When removing the load and entering skip mode, the device cannot control output overshooting, since it has no sink current capability; see the *Skip Mode Frequency and Output Ripple* section to properly size C_{OUT} under this circumstance.

A worst-case analysis in sizing the minimum output capacitance takes the total energy stored in the inductor into account, as well as the allowable sag/soar (undershoot/overshoot) voltage as follows:

$$C_{OUT\,(MIN)} = \frac{L \times \left(I^2_{OUT(MAX)} - I^2_{OUT(MIN)}\right)}{(V_{FIN} + V_{SOAR})^2 - V^2_{INIT}}, \text{voltage soar (overshoot)}$$

$$C_{OUT(MIN)} = \frac{L \times \left(I^2_{OUT(MAX)} - I^2_{OUT(MIN)}\right)}{V^2_{INIT} - (V_{FIN} - V_{SAG})^2}, \text{voltage sag (undershoot)}$$

where $I_{OUT(MAX)}$ and $I_{OUT(MIN)}$ are the initial and final values of the load current during the worst-case load dump, V_{INIT} is the initial voltage prior to the transient, V_{FIN} is the steady-state voltage after the transient, V_{SOAR} is the allowed voltage soar (overshoot) above V_{FIN}, and V_{SAG} is the allowable voltage sag below V_{FIN}. The terms (V_{FIN} + V_{SOAR}) and (V_{FIN} - V_{SAG}) represent the maximum/minimum transient output voltage reached during the transient, respectively.

Use these equations for initial output-capacitor selection. Determine final values by testing a prototype or an evaluation circuit under the worst-case conditions.

Skip Mode Frequency and Output Ripple

Enable skip mode in battery-powered systems for high efficiency at light loads. In skip mode the switching frequency (f_{SKIP}), as illustrated in Figure 1, is calculated as follows:

$$f_{SKIP} = \frac{1}{t_{ON} + t_{OFF1} + t_{OFF2}}$$

where:

$$t_{ON} = \frac{L}{V_{IN} - V_{OUT}} \times I_{SKIP\_LIMIT}$$

$$t_{OFF1} = \frac{L \times I_{SKIP\_LIMIT}}{V_{OUT}}$$

and:

$$t_{OFF2} = \frac{\Delta Q_{OUT}}{I_{LOAD}}$$

$$t_{OFF2} = \frac{L \times I_{SKIP\_LIMIT} \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right) \times \left(\frac{I_{SKIP\_LIMIT}}{2} - I_{LOAD}\right)}{I_{LOAD}}$$

Output ripple in skip mode is:

$$V_{OUT\_RIPPLE} = \left[\frac{L \times I_{SKIP\_LIMIT}}{C_{OUT} \times (V_{IN} - V_{OUT})} + R_{ESR\_COUT}\right] \times \left(I_{SKIP\_LIMIT} - I_{LOAD}\right)$$

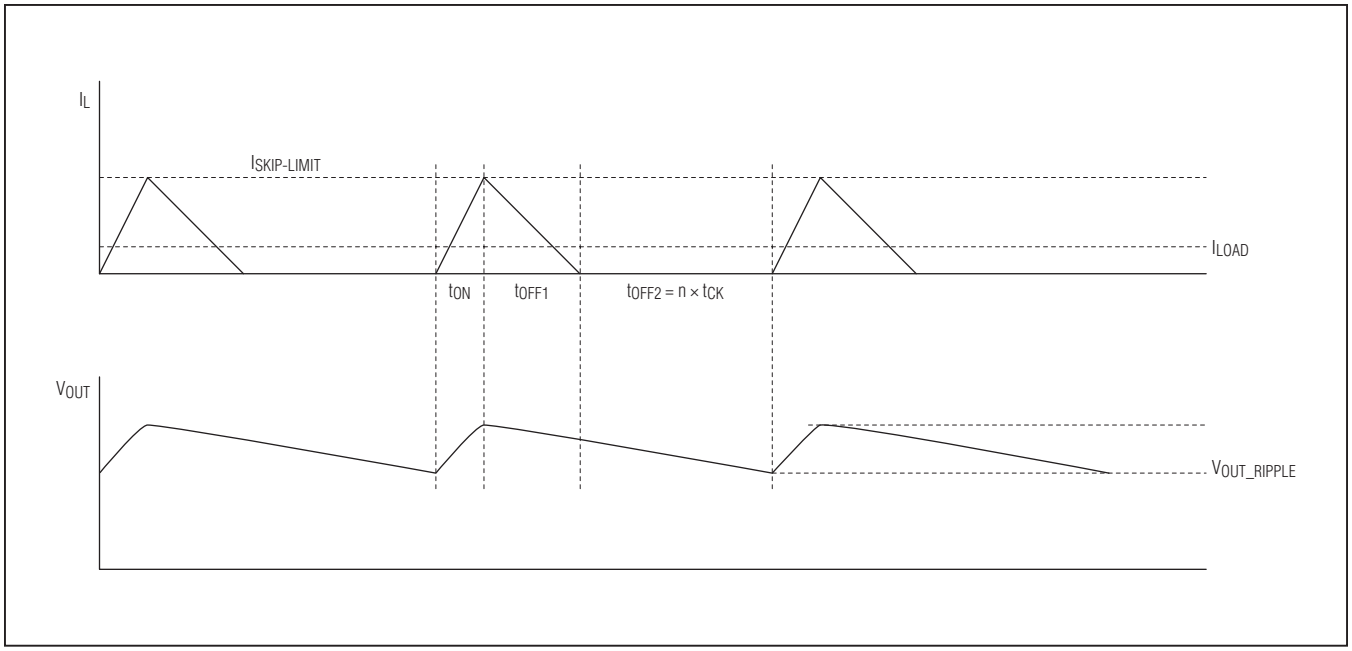


Figure 1. Skip Mode Waveform

High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

Compensation Design Guidelines

The MAX15118 uses a fixed-frequency, peak current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier). The regulator's duty cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source. As a result, the inductor's pole frequency is shifted beyond the gain bandwidth of the regulator. System stability is provided with the addition of a simple series capacitor-resistor from COMP to GND. This pole-zero combination serves to tailor the desired response of the closed-loop system. The basic regulator loop consists of a power modulator (composed of the regulator's pulse-width modulator, compensation ramp, control circuitry, MOSFETs, and inductor), the capacitive output filter and load, an output feedback divider, and a voltage-loop error amplifier with its associated compensation circuitry. See Figure 2 for a graphical representation. The power modulator's transfer function with respect to V_{COMP} is:

$$\frac{V_{OUT}}{V_{COMP}} = \frac{R_{LOAD} \times \overline{I_L}}{\left(\frac{\overline{I_L}}{G_{MOD}}\right)} = R_{LOAD} \times G_{MOD}$$

where $\overline{I_L}$ is the average inductor current, G_{MOD} is the power modulator's transconductance, and R_{LOAD} is the equivalent load resistance value.

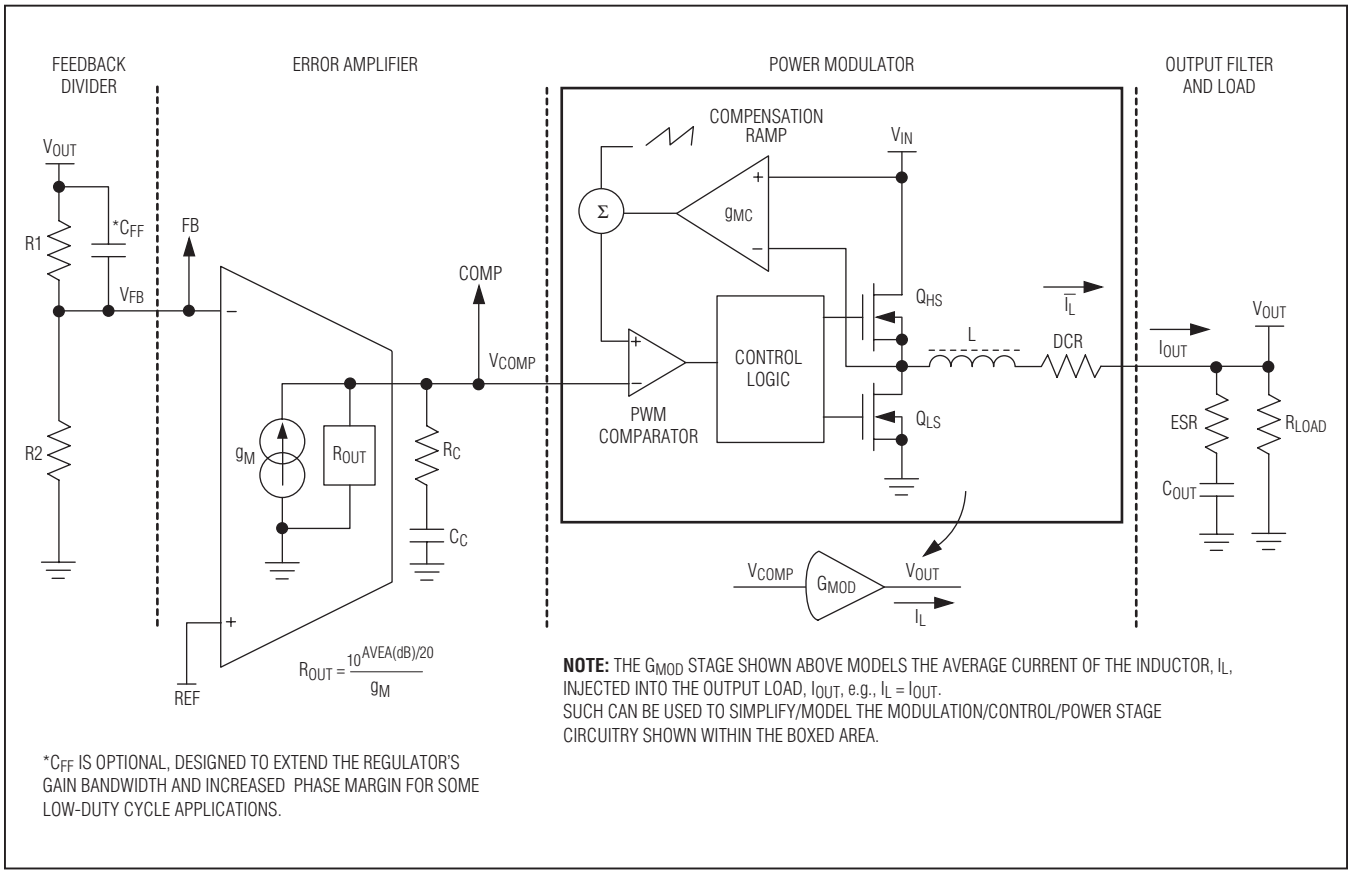


Figure 2. Peak Current-Mode Regulator Transfer Model

The peak current-mode controller's modulator gain is attenuated by the equivalent divider ratio of the load resistance and the current-loop gain. G_{MOD} becomes:

$$G_{MOD} = g_{MC} \times \frac{1}{1 + \frac{R_{LOAD}}{f_{SW} \times L} \times [K_S \times (1-D) - 0.5]}$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, f_{SW} is the switching frequency, L is the output inductance, D is the duty cycle (V_{OUT}/V_{IN}), and K_S is the slope compensation factor calculated as:

$$K_S = 1 + \frac{V_{SLOPE} \times f_{SW} \times L \times g_{MC}}{V_{IN} - V_{OUT}}$$

where V_{SLOPE} = 130mV and g_{MC} = 150A/V.

The power modulator's dominant pole is a function of the parallel effects of the load resistance and the current-loop gain's equivalent impedance. Assuming that ESR of the output capacitor is much smaller than the parallel combination of the load and the current loop, f_{PMOD} can be calculated as:

$$f_{PMOD} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} + \frac{[K_S \times (1-D) - 0.5]}{2\pi \times f_{SW} \times L \times C_{OUT}}$$

The power modulator zero is:

$$f_{ZMOD} = f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The total system transfer can be written as:

$$GAIN(s) = G_{FF}(s) \times G_{EA}(s) \times G_{MOD}(DC) \times G_{FILTER}(s) \times G_{SAMPLING}(s)$$

where:

$$G_{FF}(s) = \frac{R2}{R1 + R2} \times \frac{sC_{FF}R1 + 1}{sC_{FF}(R1 \| R2) + 1}$$

$$G_{EA}(s) = 10^{AVEA(dB)/20} \times \frac{sC_CR_C + 1}{sC_C\left(\frac{10^{AVEA(dB)/20}}{g_M}\right) + 1}$$

$$G_{FILTER}(s) = R_{LOAD} \times \frac{sC_{OUT}ESR + 1}{sC_{OUT}\left(\frac{1}{2\pi \times R_{LOAD}} + \frac{K_S \times (1-D) - 0.5}{2\pi \times f_{SW} \times L}\right)^{-1} + 1}$$

$$G_{SAMPLING}(s) = \frac{1}{\frac{s^2}{(\pi \times f_{SW})^2} + \frac{s}{\pi \times f_{SW} \times Q_C}} + 1$$

where $Q_C = \frac{1}{\pi \times [K_S \times (1-D) - 0.5]}$

The dominant poles and zeros of the transfer loop gain are:

$$f_{P1} << \frac{g_M}{2\pi \times C_C \times 10^{AVEA(dB)/20}}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT}\left(\frac{1}{R_{LOAD}} + \frac{K_S \times (1-D) - 0.5}{f_{SW} \times L}\right)^{-1}}$$

$$f_{P3} = \frac{f_{SW}}{2}$$

$$f_{Z1} = \frac{1}{2\pi \times C_CR_C}$$

$$f_{Z2} = \frac{1}{2\pi \times C_{OUT}ESR}$$

The order of pole occurrence is:

$$f_{P1} < f_{P2} < f_{Z1} < f_{CO} < f_{P3} < f_{Z2}$$

Figure 3 shows a graphical representation of the asymptotic system closed-loop response, including the dominant pole and zero locations.

The loop response's fourth asymptote (in bold, Figure 3) is the one of interest in establishing the desired crossover frequency (and determining the compensation component values). A lower crossover frequency provides for stable closed-loop operation at the expense of a slower load and line-transient response. Increasing the crossover frequency improves the transient response at the (potential) cost of system instability. A standard rule of thumb sets the crossover frequency ≤ 1/5 to 1/10 of the switching frequency.

Closing the Loop: Designing the Compensation Circuitry

1) Select the desired crossover frequency. Choose f_{CO} equal to 1/10th of f_{SW}, or $f_{CO} \cong 100kHz$.

2) Select R_C using the transfer-loop's fourth asymptote gain equal to unity (assuming $f_{CO} > f_{P1}$, f_{P2}, and f_{Z1}). R_C becomes:

$$R_C = \frac{R1+R2}{R2} \times \frac{\left(1+\frac{R_{LOAD} \times K_S[(1-D)-0.5]}{L \times f_{SW}}\right)}{g_M \times g_{MC} \times R_{LOAD}}$$

$$\times 2\pi \times f_{CO} \times C_{OUT} \times \left[ESR + \frac{1}{\frac{1}{R_{LOAD}} + \frac{K_S[(1-D)-0.5]}{L \times f_{SW}}}\right]$$

where K_S is calculated as:

$$K_S = 1 + \frac{V_{SLOPE} \times f_{SW} \times L \times g_{MC}}{V_{IN} - V_{OUT}}$$

and g_M = 1.2mS, g_{MC} = 150A/V, and V_{SLOPE} = 130mV.

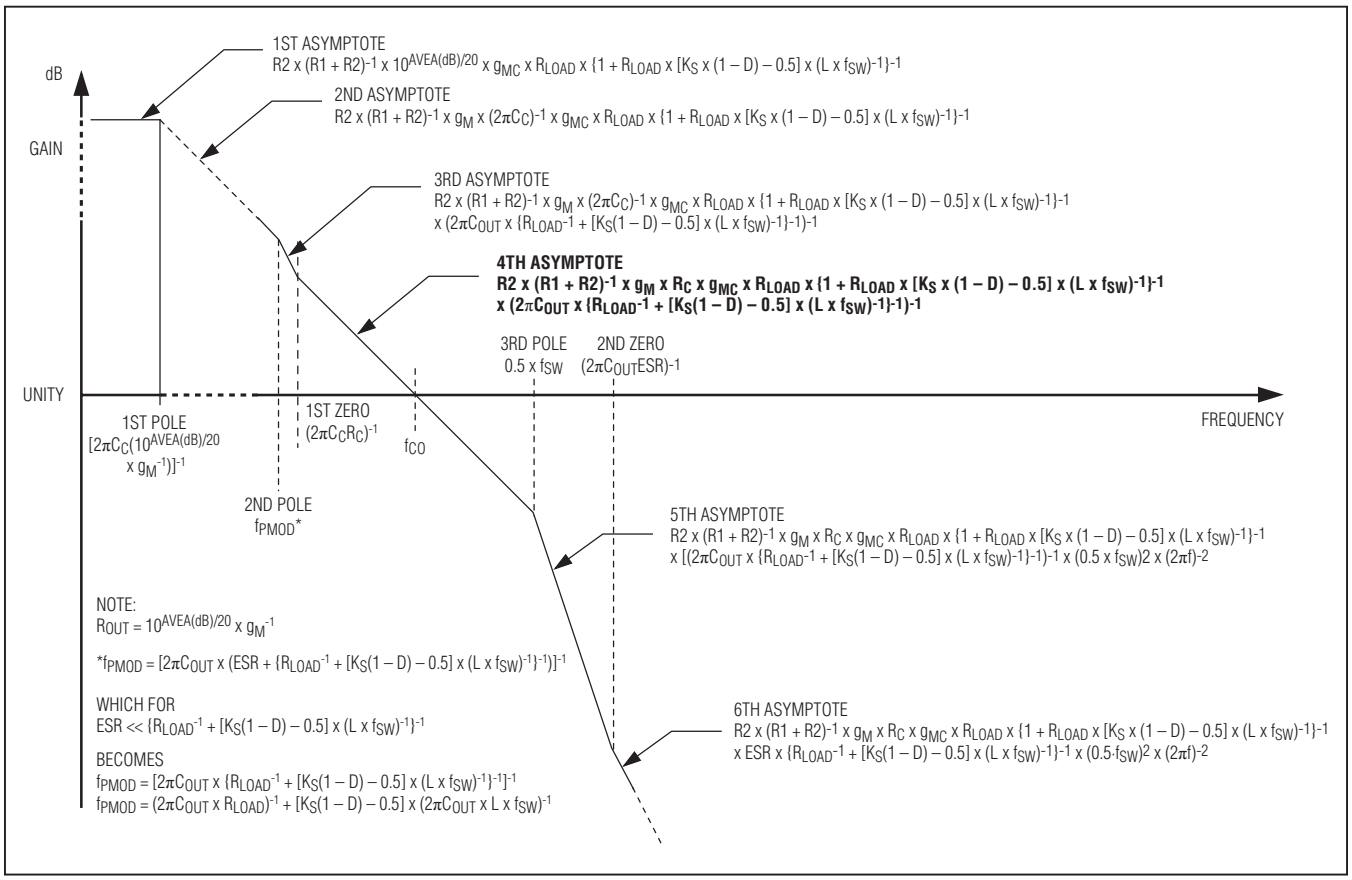


Figure 3. Asymptotic Loop Response of Peak Current-Mode Regulator

3) Select C_C. C_C is determined by selecting the desired first system zero, f_{Z1}, based on the desired phase margin. Typically, setting f_{Z1} below 1/5th of f_{CO} provides sufficient phase margin.

$$C_C \geq \frac{5}{2\pi \, f_{CO} \times R_C}$$

Optionally, for low duty-cycle applications, the addition of a phase-leading capacitor (C_{FF} in Figure 2) helps mitigate the phase lag of the damped half-frequency double pole. Adding a second zero near to but below the desired crossover frequency increases both the closed-loop phase margin and the regulator's unity-gain bandwidth (crossover frequency). Select the capacitor as follows:

$$C_{FF} = \frac{1}{2\pi \times f_{CO} \times (R1 \,||\, R2)}$$

Using C_{FF}, the zero-pole order is adjusted as follows:

$$f_{P1} < f_{P2} < f_{Z1} < 1/\left[2\pi C_{FF} R_1\right]$$
$$< 1/\left[2\pi C_{FF} (R1 || R2)\right] < f_{P3} < f_{Z2}$$

Setting the Soft-Start Time

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. Size the C_{SS} capacitor to achieve the desired soft-start time, t_{SS}, using:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{FB}}$$

I_{SS}, the soft-start current, is 10µA (typ) and V_{FB} is the 0.6V (typ) output feedback voltage threshold. When using large C_{OUT} capacitance values, the high-side current limit can trigger during the soft-start period. To ensure the correct soft-start time, t_{SS}, choose C_{SS} large enough to satisfy:

$$C_{SS} >> C_{OUT} \times \frac{V_{OUT} \times I_{SS}}{(24A - I_{LOAD}) \times V_{FB}}$$

An external tracking reference with steady-state value between 0V and (V_{IN} - 2.5V) can be applied to SS/REFIN. In this case, connect an RC network from the external tracking reference and SS/REFIN, as shown in Figure 4. The recommended value for R_{SS} is approximately 330Ω. R_{SS} is needed to ensure that, during hiccup period, SS/REFIN can be pulled down internally.

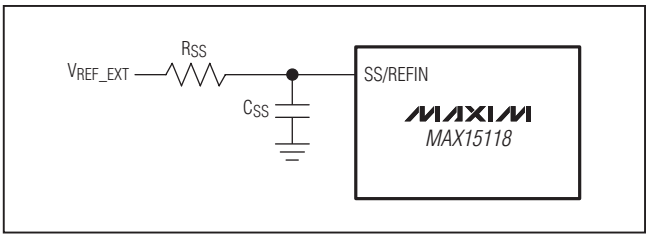


Figure 4. RC Network for External Reference at SS/REFIN

Design Examples

Table 1 provides values for various outputs based on the typical operating circuit.

Table 1. Suggested Component Values (see the Typical Operating Circuits)

V_{IN} (V)	V_{OUT} (V)	L (µH)	LIR (A/A)	C15 (nF)	R3 (kΩ)	C14 (pF)	R1 (kΩ)	R2 (kΩ)
3.3	0.8	0.15	0.22	6.8	2.94	22	1.78	5.36
3.3	1.2	0.15	0.28	4.7	2.21	22	5.36	5.36
3.3	1.5	0.15	0.30	3.3	3.83	22	8.06	5.36
3.3	1.8	0.15	0.30	3.3	4.22	22	10.7	5.36
3.3	2.5	0.15	0.22	3.3	5.62	22	16.9	5.36
5	0.8	0.15	0.25	6.8	2.94	22	1.78	5.36
5	1.2	0.15	0.34	4.7	2.21	22	5.36	5.36
5	1.5	0.15	0.39	3.3	3.83	22	8.06	5.36
5	1.8	0.22	0.29	3.3	3.92	22	10.7	5.36
5	2.5	0.22	0.32	3.3	5.1	22	16.9	5.36
5	3.3	0.22	0.28	2.2	4.64	22	24.3	5.36

Note: *C_{IN}, C_{OUT}, and other components are the same as in the standard MAX15118 Evaluation Kit.*

Power Dissipation

The MAX15118 is available in a 28-bump WLP package and can dissipate up to 3.26W at T_A = +70°C. When the die temperature exceeds +150°C, the thermal shutdown protection is activated (see the *Thermal Shutdown Protection* section).

Layout Procedure

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15118 Evaluation Kit (EV kit) layout for optimum performance. The MAX15118 EV kit board has a small, quiet, ground-shape SGND on the back side below the IC. This ground is the return for the control circuitry, especially the return of the compensation components. This SGND is returned to the IC ground through vias close to the ground bumps of the IC. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect a single ground plane immediately adjacent to the GND bumps of the IC.
2) Place capacitors on IN and SS/REFIN as close as possible to the IC and the corresponding pad using direct traces.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) An electrolytic capacitor is strongly recommended for damping when there is significant distance between the input power supply and the MAX15118.
5) Connect IN, LX, and GND separately to a large copper area to help cool the IC to further improve efficiency.
6) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
7) Route high-speed switching nodes (such as LX and BST) away from sensitive analog areas (such as FB and COMP).

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX15118EWI+	-40°C to +85°C	28 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

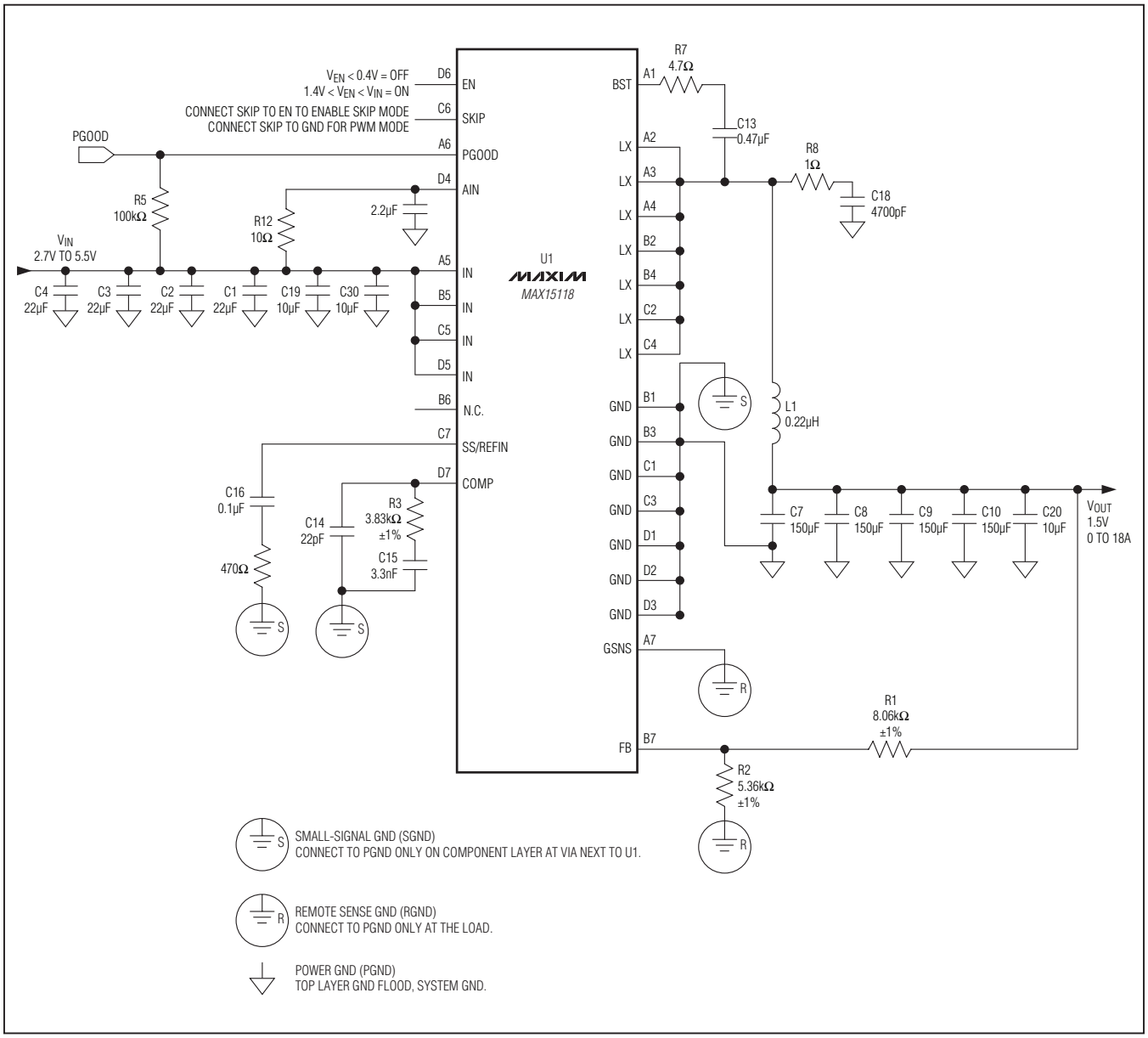
Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 WLP (2.10mm x 3.56mm)	W282B3Z+1	**21-0577**	Refer to **Application Note 1891**

High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

Typical Operating Circuits (continued)



High-Efficiency, 18A, Current-Mode Synchronous Step-Down Regulator with Integrated Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—