L638X TRICKS AND TIPS

by Gian Paolo Meloncelli

Topics covered:
- *Devices family*
- *Internal diode structure*
- *How to select Cboot*
- *Parasitic elements in the half bridge topology*
- *How to manage below ground voltage on out pin:*
    - *Out pin voltage that persists below the signal ground*
    - *Undershoot spike on the out pin*
    - *Tricks and layout suggestions*
- *L6386: how to deal with signal ground and power ground*

Devices Family

The ST L638X family includes four control ICs: L6384, L6385, L6386 and L6387.

They are realized in BCD off line technology: they are able to operate at voltage up to 600V. The logic inputs are CMOS logic compatible and the driving stages can source up to 400mA and sink 600mA. The bootstrap diode is integrated inside the ICs helping to reduce the PCB parts number and to increase the layout flexibility.

INTERNAL DIODE STRUCTURE

**Figure 1. Integrated bootstrap diode (principle schematic)**
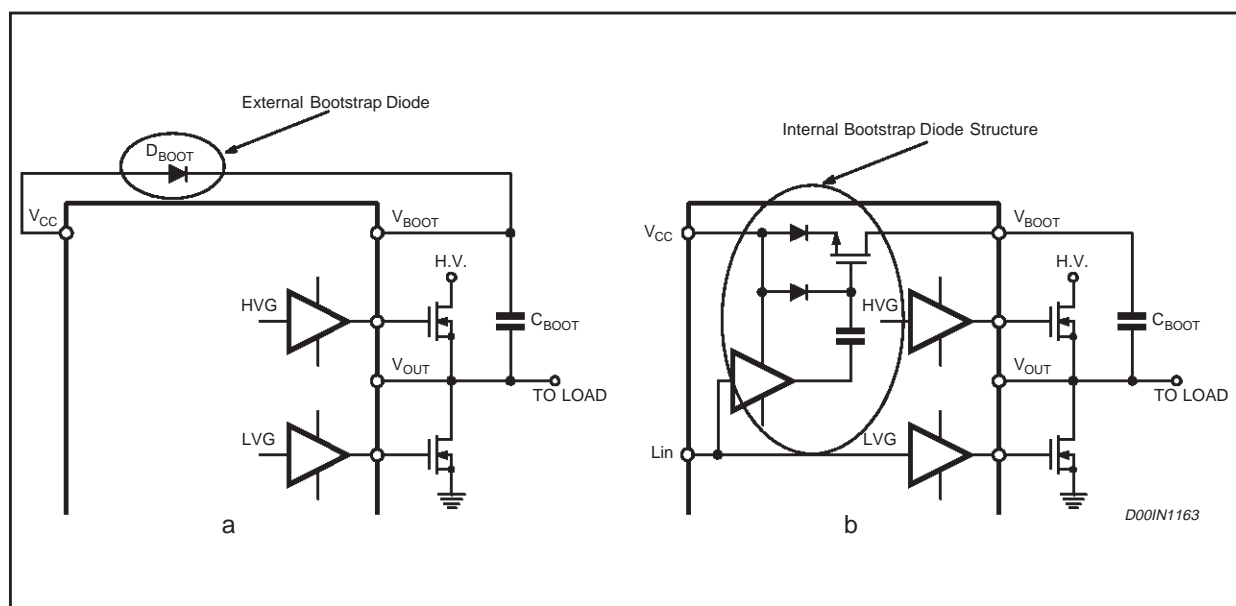
A floating supply is required to drive the high voltage section and the high side switch gate. For this reason we must use the bootstrap principle, normally accomplished by an high voltage fast recovery diode (fig.1a). The bootstrap capacitor is charged when the Vout become below the IC supply voltage: in this situation the current flows from the IC supply (Vcc pin) to the capacitor (fig.2). When the out pin is pulled up near to the high voltage rail (the low side switch is turned off and the high side switch on), the diode is reverse biased and the capacitor can "fly up" to the level of the high voltage bus plus Vcc. The high voltage section is supplied only by the bootstrap capacitor.

In the L638x family a patented integrated structure replaces the external diode. It is realized by an high voltage DMOS (typical Rdson 125Ω) driven synchronously with the low side driver (LVG), with a diode in series, as indicated in fig 1b.

When the internal bootstrap structure is used we have to remember that:

1.   The "internal diode" is a structure, and not an integrated discrete diode: this means that the diode structure is turned on (and it behaves like an external diode) only when the low side driver is on.

2.   When the low side driver is turned on, out pin voltage must be below the IC supply: otherwise the current can not flow from the supply to the bootstrap capacitor (fig 2).

**Figure 2. Bootstrap capacitor charging path**
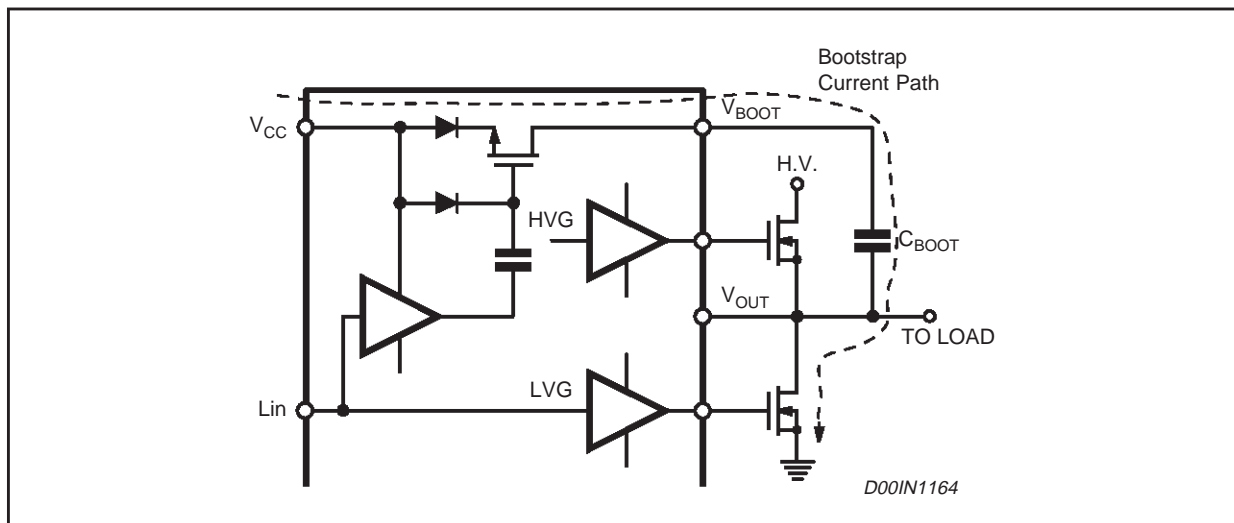
The following picture (figure 3a) shows an example in which the internal bootstrap diode can not be used:

when the low side driver is on (fig.3b) the voltage at the out pin is held to the high voltage bus and the current can not charge the bootstrap capacitor. The out pin voltage goes below the IC supply voltage 0V only when Vinput is low (Vout=-Vf-Rsense*Iload): but in this situation the internal diode is off, and the charging current can not flow in the capacitor.

For more detailed information on the internal diode behavior see AN1263 "Using the internal bootstrap charge capability of the L6384, 85, 86 and 87 in driving a six transistor inverter bridge".

Figure 3. In this example the external diode is mandatory.

(a)

(b) VInput High - Current Path -

(c) VInput Low - Current Path -

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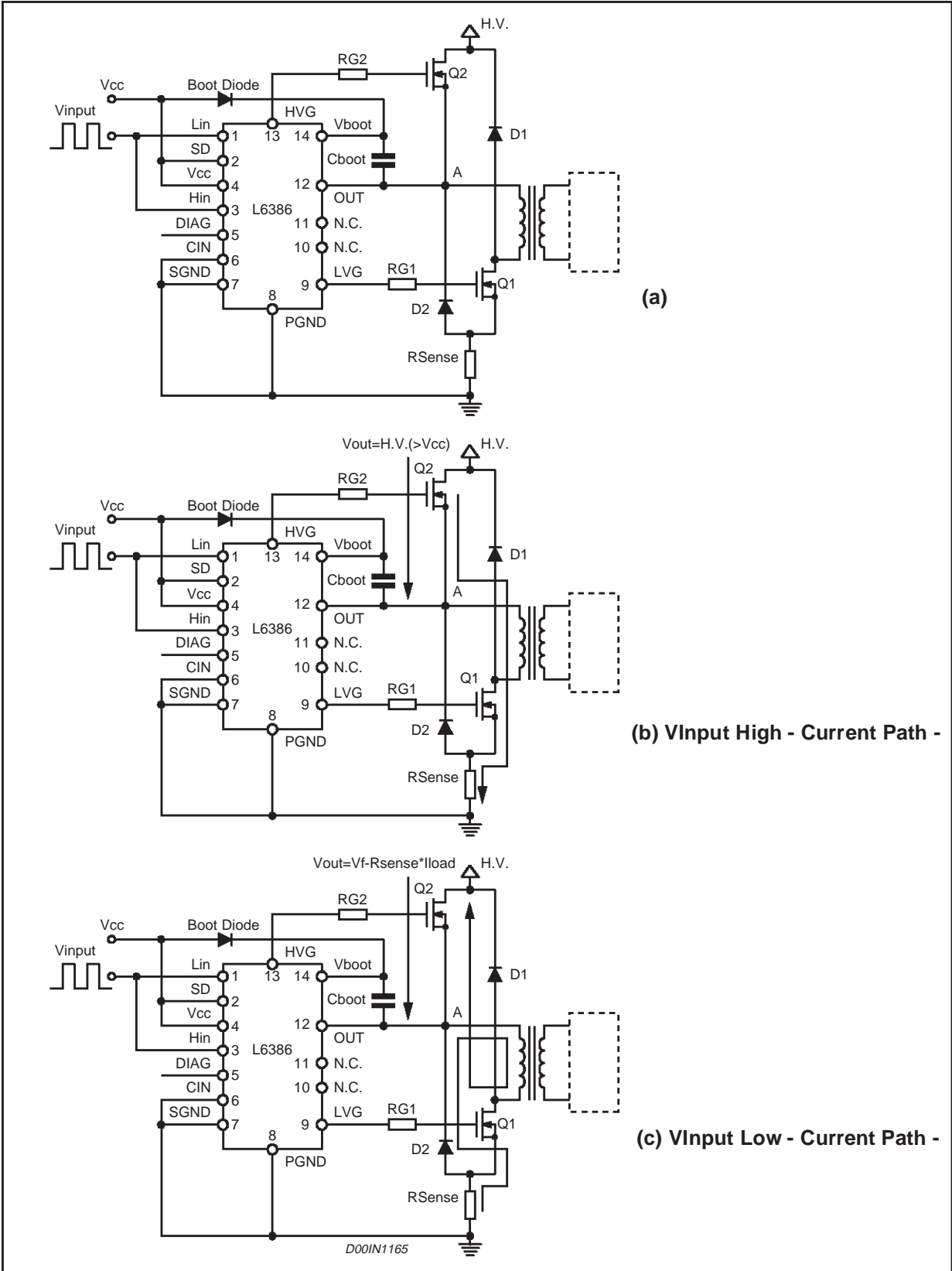
HOW TO SELECT C$_{BOOT}$

As already said, when the internal bootstrap diode is used, the bootstrap capacitor is charged every time the low side driver is on and the out pin is below the IC power supply. The capacitor is discharged only when the high side switch is turned on: this capacitor is the supply for the high voltage section.

Let us discuss how to select the right capacitor value. The dimensioning procedure that we are going to describe is valid for both cases: with or without the external diode.

The first parameter to take into account is the maximum voltage drop that we have to guarantee when the high side switch is in on state.

The maximum allowable voltage drop (ΔV_{Boot}), depends on the minimum gate drive voltage (for the high side switch) that we want to maintain. If V_{gs-min} is the minimum gate source voltage, the capacitor drop must be :

$$\Delta V_{boot} = V_{cc} - V_F - V_{gs\_min}$$

V_{cc} : IC voltage supply

V_F : Bootstrap diode forward voltage

The capacitor size is calculated by the formula :

$$C_{Boot} = \frac{Q_{tot}}{\Delta V_{boot}}$$

Q_{tot} : total amount of the charge supplied by the capacitor. This is evaluated taking into account the following factors:

I.	Q_{gate}:	High side switch total gate charge
II.	I_{lk_gs}:	High side switch gate-source leakage current
III.	I_{lk_cap}:	Bootstrap capacitor leakage current
IV.	I_{qbs}:	Bootstrapped section quiescent current
V.	I_{lk}:	Bootstrapped section leakage current
VI.	Q_{ls}:	Charge required by the internal level shifter (3nC for all L638x drivers)
VII.	T_{on}:	High side switch on time
VIII.	I_{lk_diode}:	External diode leakage current (if it is used).

The total charge supplied by the bootstrap capacitor will be:

$$Q_{tot} = Q_{gate} + (I_{lk\_cap} + I_{lk\_gs} + I_{qbs} + I_{lk} + I_{lk\_diode}) \cdot T_{on} + Q_{ls}$$

The capacitor leakage current is important only if an electrolytic capacitor is used, otherwise this term can be neglected (e.g. with ceramic capacitor).

When the internal diode is used, the Dmos Rdson introduces an additional voltage drop that can be low at low switching frequency. Increasing the frequency this drop can be evaluated as follow:

$$V_{drop} = I_{charge} \cdot R_{dson} = \frac{Q_{tot}}{T_{charge}} \cdot R_{dson}$$

I_{charge} : capacitor charging current.

R_{dson} : Dmos drain-source typical on resistance.

T_{charge} : capacitor charging time (It is the low side turn on time).

This drop must be taken into account when the maximum ΔV_{Boot} is calculated. If this drop is too high or the circuit topology does not allow a sufficient charging time, an external fast recovery diode can be used.

Example:

Let's evaluate the bootstrap capacitor size when (the internal diode is used) .

Data:

o Q_{gate} = 70nC   (STGW12NB60H)

o I_{lk_gs} = 100nA

o I_{qbs} = 200µA   (Datasheet L6386)

o I_{lk} = 10µA   (Datasheet L6386)

o Q_{ls} = 3nC

o T_{on} = 100µs

Capacitor leakage current is not considered because we assume we use a ceramic capacitor and not an electrolytic one.

If the maximum allowable voltage drop on the bootstrap capacitor is 1 V during the high side switch on state, the minimum capacitor size is:

$$C_{Boot} = \frac{Q_{tot}}{\Delta V_{Boot}} = \frac{94nC}{1V} = 94nF$$

The voltage drop due to the internal Dmos Rdson is nearly:

$$V_{drop} = \frac{Q_{tot}}{T_{charge}} \cdot R_{dson} = \frac{94nC}{100µs} \cdot 125\Omega = 117mV$$

and can be neglected. We have assumed the capacitor charging time equal to the high side on time (duty cycle 50%).

According to different bootstrap capacitor sizes we may have the following drops:

o 100nF --> $\Delta V_{Boot} = \frac{Q_{tot}}{C_{Boot}} = 0.93V$,

o 150nF --> $\Delta V_{Boot} = \frac{Q_{tot}}{C_{Boot}} = 0.62V$,

o 220nF --> $\Delta V_{Boot} = \frac{Q_{tot}}{C_{Boot}} = 0.42V$

Suggested values are within the range of 100nF-570nF but the right value must be selected according to the application in which the device is used, when the capacitor size is too big, the bootstrap charging time is slowed and the low side on time (i.e. the "internal diode" on time) might be not long enough to reach the right bootstrap voltage.

PARASITIC ELEMENTS IN THE HALF BRIDGE TOPOLOGY

Parasitic elements exist inside a half bridge driver circuit and they have to be considered because switching currents rapid changes induce voltage transients across all the parasitic components.

In the following paragraphs we are going to describe the use of L6386 in a typical half bridge application and the layout parasitic elements to minimize in order to improve the application behavior (see fig.4).

We take the L6386 device as example, but the considerations that we do can be used also for all L638X drivers.

Figure 4. Main parasitic elements that must be taken into account inside the half bridge topology.
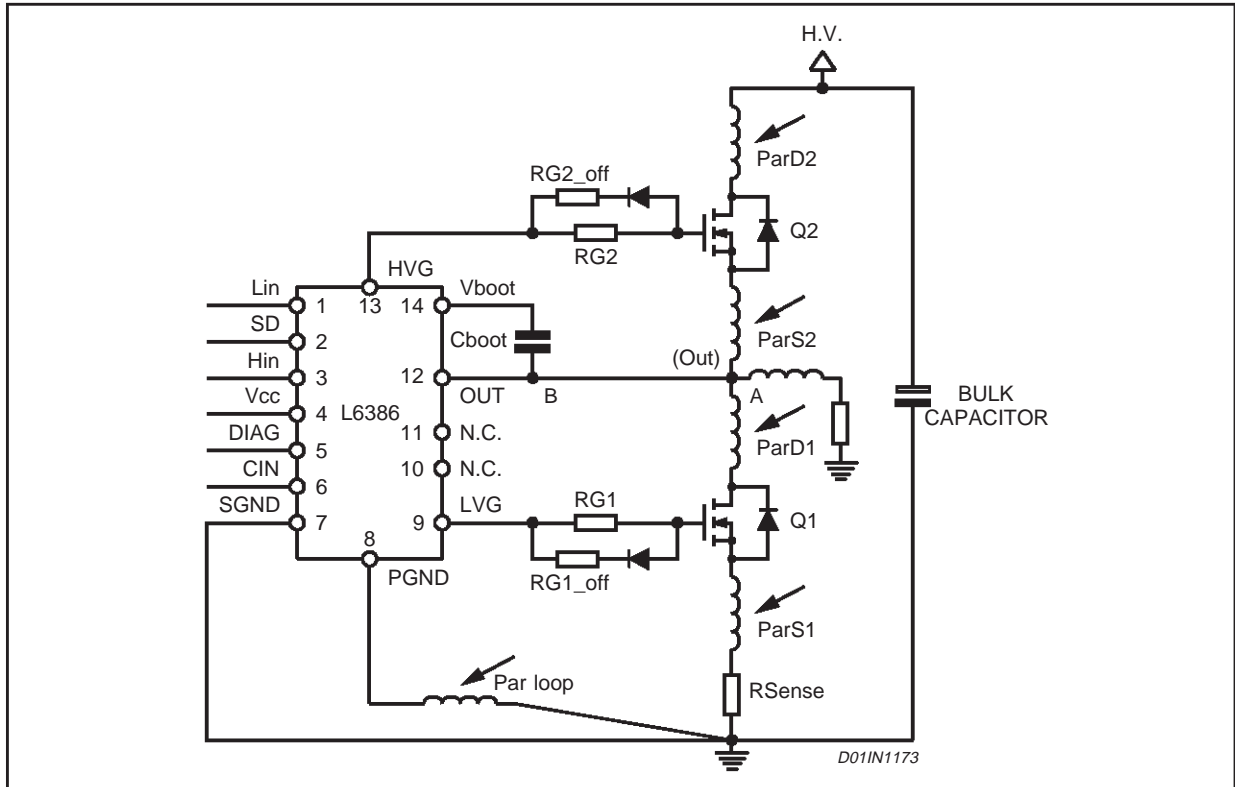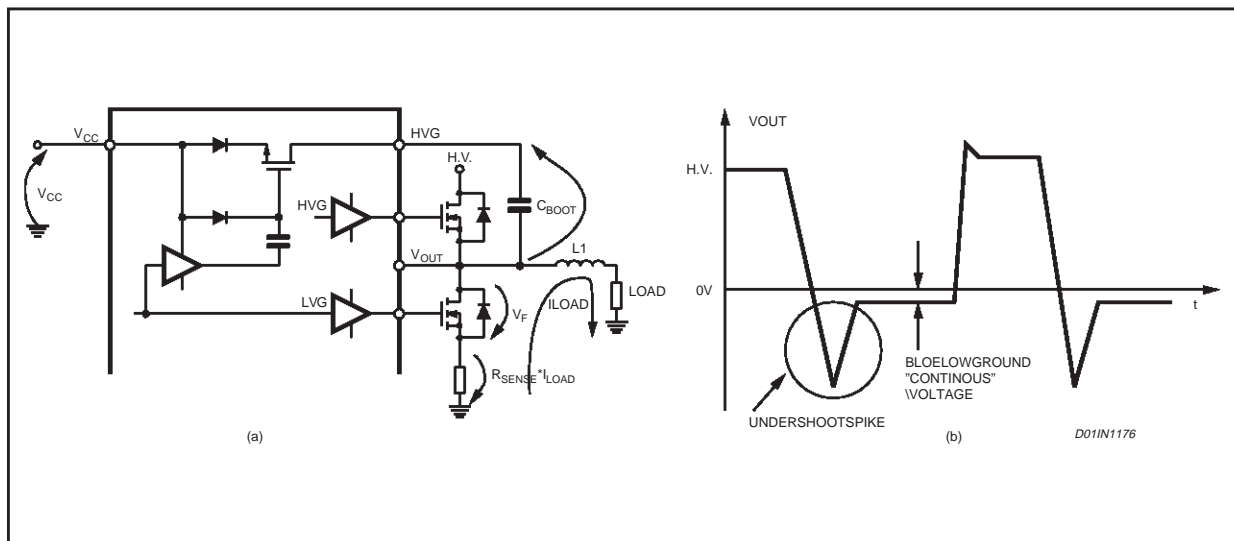
1 HOW TO MANAGE BELOW GROUND VOLTAGE ON THE OUT PIN

We have to take care of the below ground voltage on the out pin because they are really pernicious. There are two main issues:

1) Out pin voltage persists below the signal ground reference during all the time in which the low side freewheeling diode is in conduction state. **(Static condition)**

2) Undershoot spike on the out pin that appears during the commutation pattern. **(Dynamic condition)**

In the following sections let's analyze both the issues and what could happen to the IC.

1.1 Out Pin voltage that persists below the signal ground

Figure 5. Voltage across the bootstrap capacitor.

In static mode the out pin can sustain below ground voltages down to -3V (absolute maximum rating). Within this limit, a negative voltage on the out pin can cause the bootstrap capacitor overcharge. This condition happens when the load current flows in the direction shown in fig.5a: the high side is off and the low side freewheeling diode is on.

In this condition the voltage between the out pin and the ground is:

$$V_{out} = - (R_{sense} + R_{trace}) \cdot I_{load} - V_f$$

Where V_f is the freewheeling diode forward voltage, Rtrace is the parasitic trace resistance, Rsense the sense resistor and Iload is the load current. We have not mentioned the parasitic trace inductance because we are not dealing with dynamic undershoot voltage.

The voltage across the Cboot is:

$$V_{boot} = V_{cc} - V_{out} = V_{cc} + (R_{sense} + R_{trace}) \cdot I_{load} + V_f$$

It has to be: V_{boot} < 17V (Recommended operating condition for all the three L638x drivers). The bootstrap capacitor is the supplier of the internal High Voltage driver, and if this voltage goes above the recommended condition the device could fail.

In order to avoid this undesired phenomena we suggest the following "rules":

→ maintain a "safety margin" when the V_{cc} is selected: for example, if we use V_{cc} = 15V and we want to avoid that the bootstrap capacitor becomes overcharged (i.e. charged over 17V), the out pin must not go below ground more than -2V. The higher Vcc, the lower below ground voltage on the out pin.

→ Select the Rsense and minimize Rtrace in order to satisfy the the following relation:

$$Vboot = Vcc - Vout = Vcc + (R_{sense} + R_{trace}) \cdot I_{load} + V_f < 17V$$

1.2 Undershoot spike on the out pin:

If the out pin undershoot spike has a time length that is in order of tenths of nanoseconds the bootstrap capacitor can not become overcharge.

Figure 6. Equivalent internal bootstrap charging circuit.
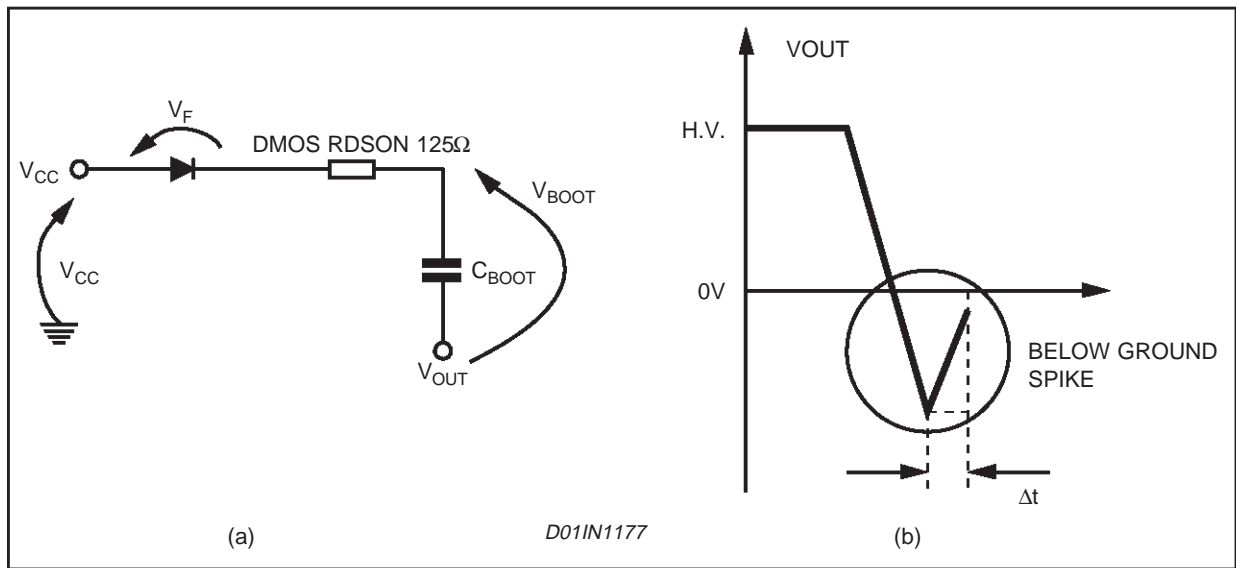
We can evaluate the maximum below ground duration that can lead to capacitor overcharge. Let us assume that the below ground spike has not a triangular shape but a square shape, like the dotted line in the fig. 6a (worst case).

If we have:

o V_{cc} = 15

o C_{boot} = 100nf

o V_f = 0.7V

o V_{out} = 18V (Below ground spike on the out pin)

o ΔV_{boot} =17V-15V=2V (Maximum allowable capacitor overcharge voltage)

the max below ground spike duration is :

$$\Delta t = R_{DSon} \cdot C_{Boot} \cdot Ln\left(\frac{V_{out} - V_f}{V_{out} - V_f - \Delta V_{boot}}\right) \cong 1.5\mu s$$

It is much more than some tenths of nanoseconds! Note that in this example we use the internal bootstrap diode. If an external diode is adopted, the situation may become more dangerous: infact in this case the internal Dmos Rdson resistance does not limit the bootstrap capacitor overcharge.

The example above demonstrates that short undershoot spikes on the out pin do not lead to bootstrap overcharge. They are dangerous for another reason: heavy below ground spikes can lead to a spurious logic commutation of the IC. It can happen that the high side or the low side buffer do not follow the input logic signals. A consequence of this situation is power switch cross-conduction and/or device damage.

This situation is caused by the parasitic inductance in the tracks between the out node and ground, we have called them ParD1 and ParS1 in the fig. 4.

Now we will analyze the following points:

1. How to measure the below ground spike on the out pin?
2. What are the root causes?
3. Dealing with the undershoot spikes - tricks and layout suggestions.

1.2.1 How to measure the below ground spike on the out pin?

The voltage difference between the out pin and the signal ground is one of the first signals that has to be analyzed with the oscilloscope when the driver outputs do not follow the logic inputs or when the device has a "general" failure.

It is very important to put the ground probe as close as possible to the IC signal ground pin and not to a generic ground.

 If the ground probe is not well connected to a point that is close to the IC pin, a lot of noise and strange spurious spikes could be seen, due to the high current that can flows into the ground tracks of the application.

Figure 7. Where to put the oscilloscope probe for the undershoot spike measurement.
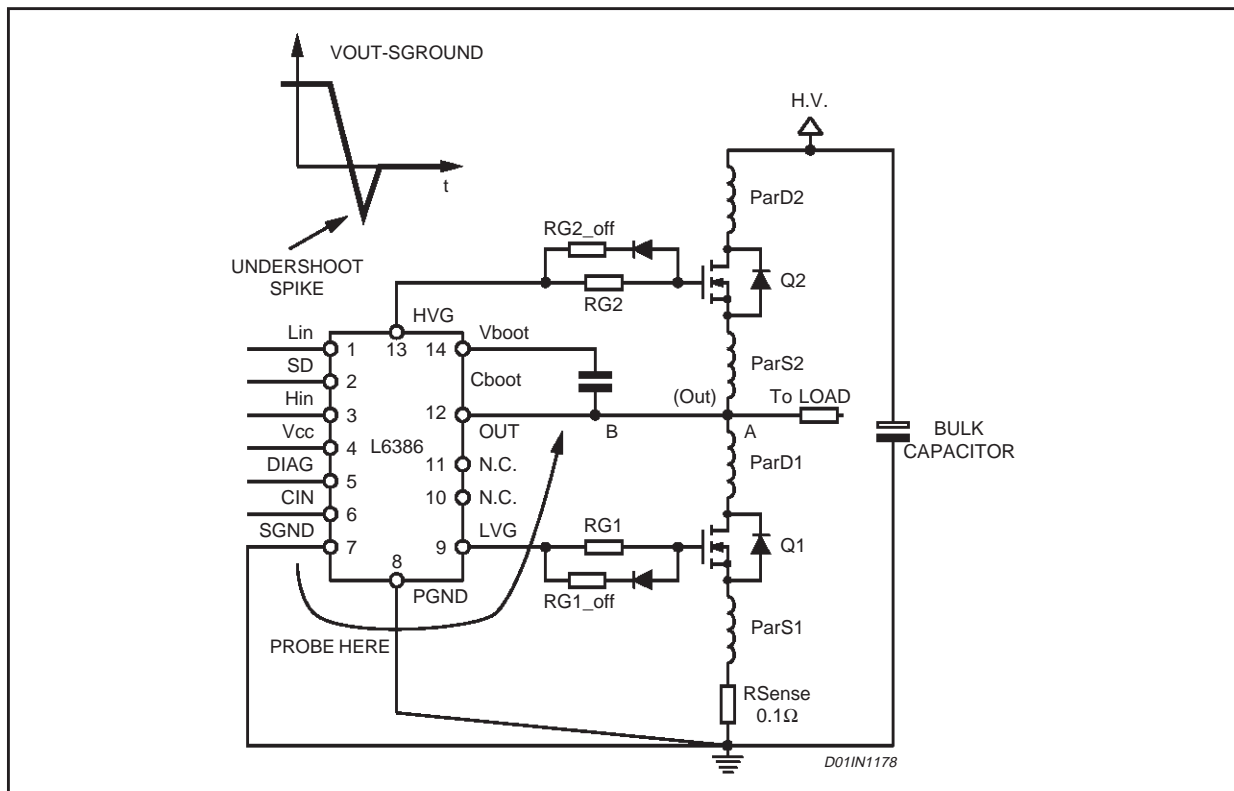
1.2.2 What are the root causes ?

Let's find the undershoot spike root causes. There are two main causes:

   I. Tracks parasitic inductance

    II. High di/dt values

We can use the well known formula:

$$\Delta V = L \cdot \frac{dI}{dt}$$

Where L = ParD1 + ParS1 (referring to fig. 4). Note that the parasitic inductance ParD2 and ParS2 are not involved in the path that can lead to the undershoot voltage on the out pin.

Let's analyze the current path during the high and low side commutation when the direction of the load current is positive or negative. (See fig. 8)

Figure 8. PCB Trace Parasitic inductance that must be minimized.
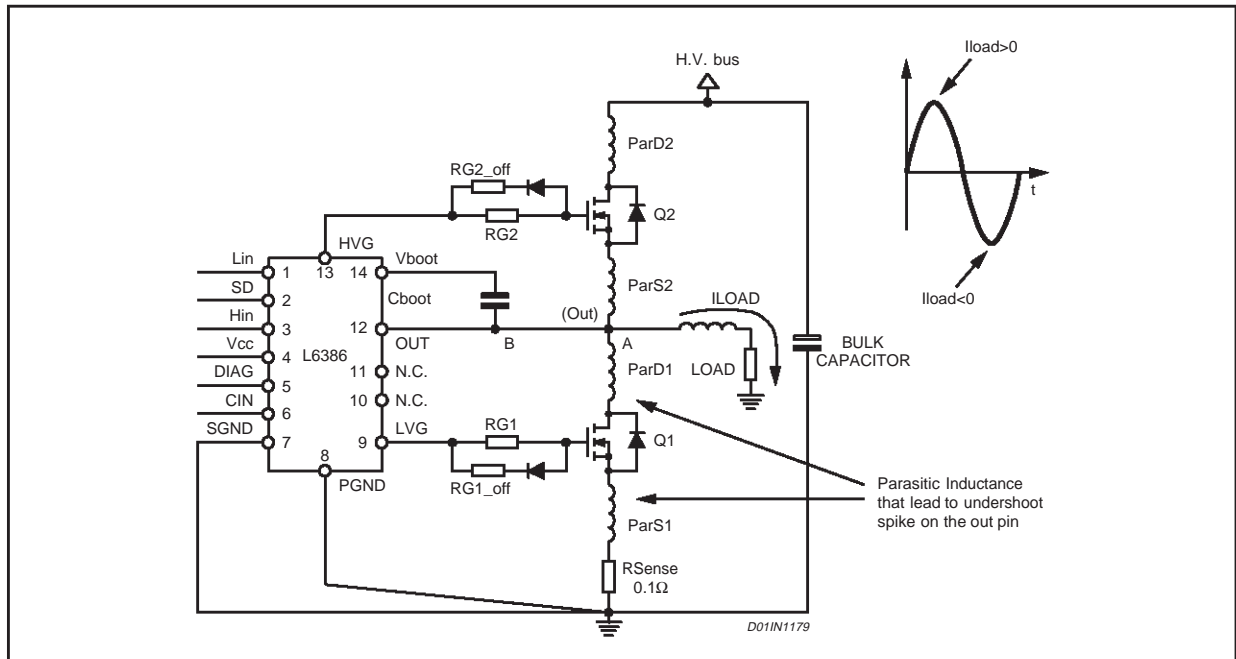
$I_{load} > 0$:

In this condition the undershoot spike at the out pin appears when the high side is switched off and the load current must flow through the low side freewheeling diode. The below ground spike in this condition is:

$$V_{peak} = V_{fpk} + L \cdot \frac{dI}{dt} + (R_{sense} + R_{trace}) \cdot I_{load}$$

The peak voltage is mainly composed by the L*dI/dt and Vfpk contribute, all other terms are negligible.

Vfpk: the diode usually has a forward voltage around 1V but shows a forward peak voltage that depends on the dI/dt current and on the diode technology. The higher dI/dt, the higher peak forward voltage across the diode(Fig.9).

Figure 9. Diode transient forward peak voltage versus dI/dt (STTA806).
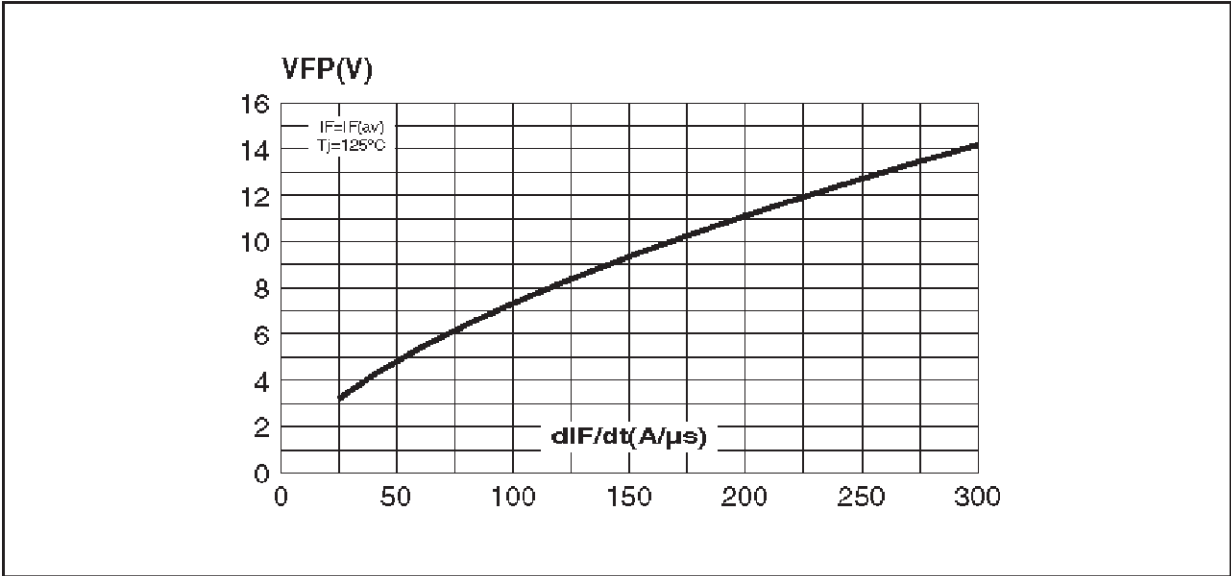
HIGH SIDE ON-LOW SIDE OFF

Figure 10. The low side device is off and the load current flows in the high side power switch (On)
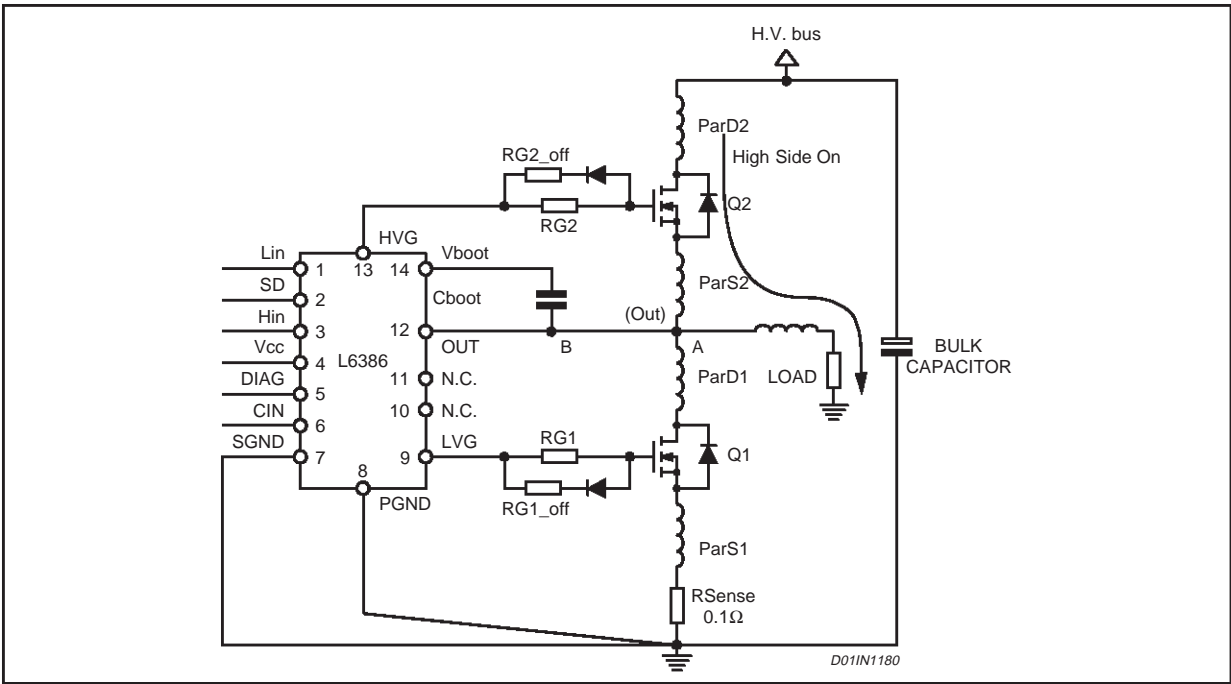
HIGH SIDE OFF -LOW SIDE OFF

Figure 11. The high side is turned off and the load current flows trough the low side freewheeling diode that is injected
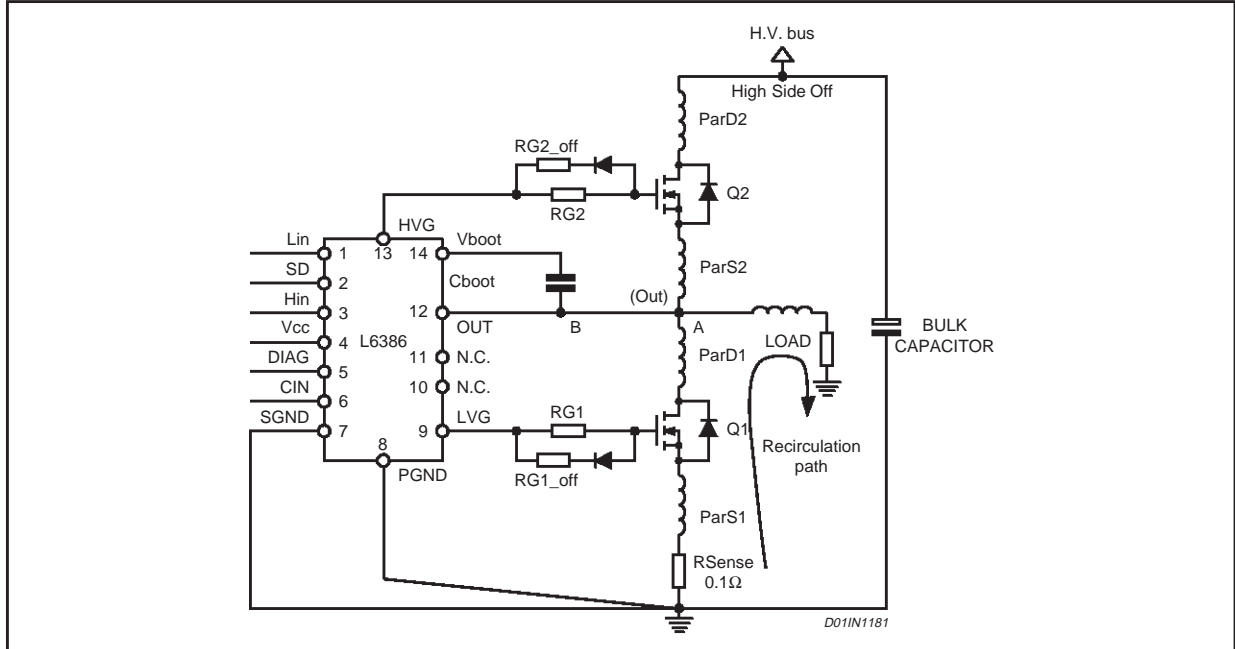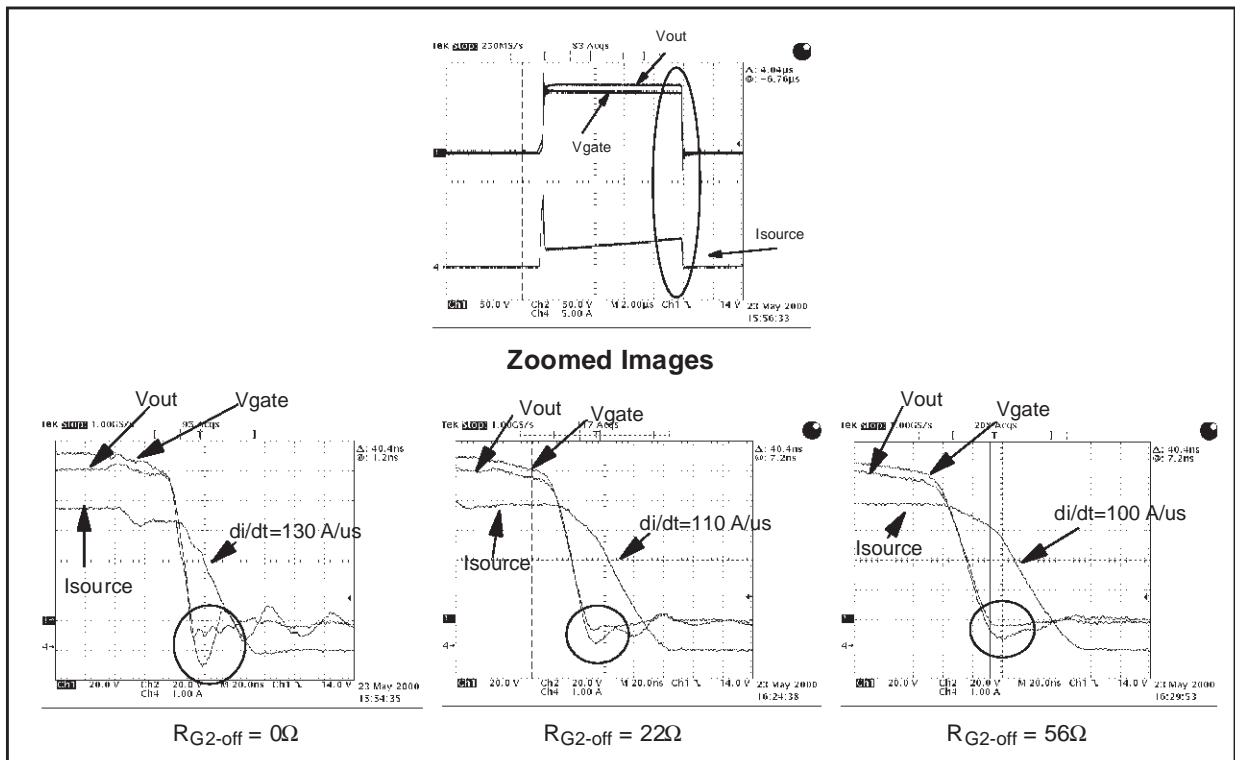

Figure 12. The oscilloscope image shows how the undershoot spike on the out pin is handled with the high side turn off resistor (Rg2_Off).Note that all the measurements shown are done with the low side always off.

Zoomed Images

$R_{G2-off} = 0\Omega$

$R_{G2-off} = 22\Omega$

$R_{G2-off} = 56\Omega$

In order to reduce this undershoot voltage we can act on:

→ reducing the parasitic L between the out and the ground connection.

→ reducing the dI/dt: this is accomplished by increasing the high side turn off resistor. This has the double effect to reduce the low side diode forward peak voltage and the parasitic inductance contribution .Disadvantage: the switching power losses increase.

During the high side turn-on, on the out pin we can see only an overshoot spike but in most of cases this is not dangerous for the IC due to the high voltage capability of these L638x drivers (600V is the absolute maximum on the out pin).

■ $I_{load} < 0$:

In this load condition the bigger undershoot spike on the out pin occurs when the low side switch is turned on during the high side freewheeling diode conduction state. The spike is mainly related to the freewheeling diode behavior.
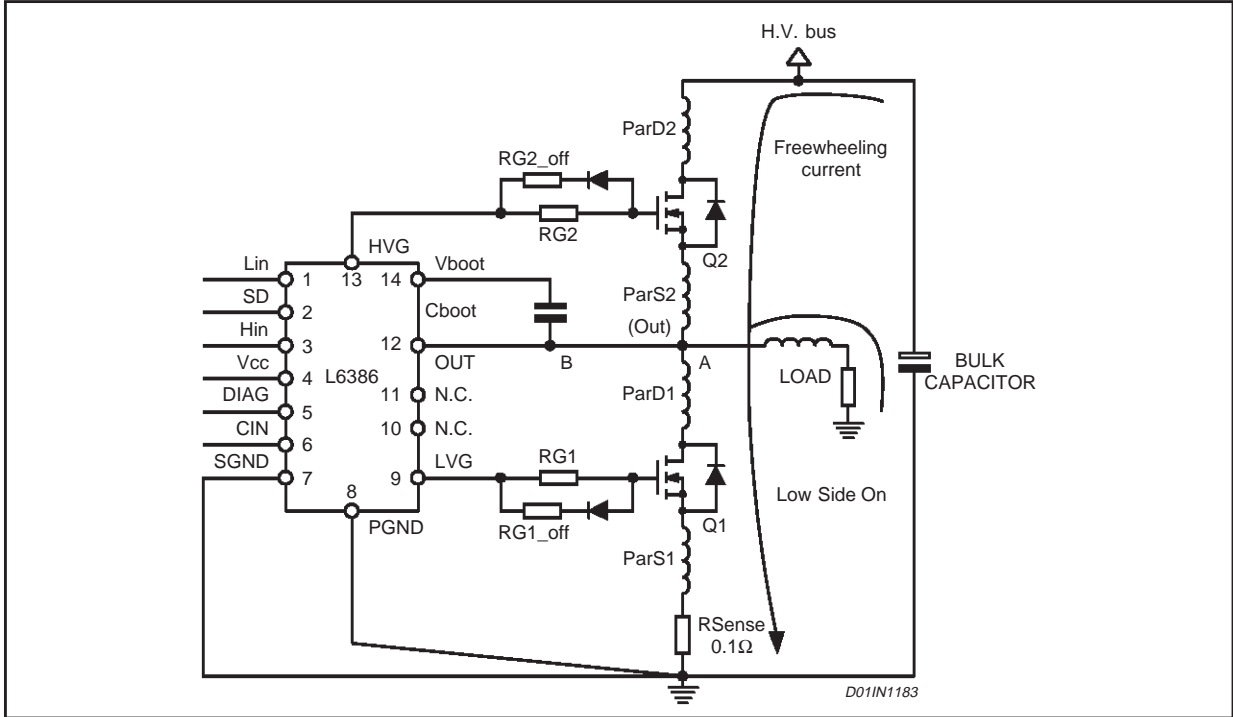
HIGH SIDE OFF - LOW SIDE OFF

Figure 13. The low side Mos is off and the load current flows inside the high side freewheeling diode
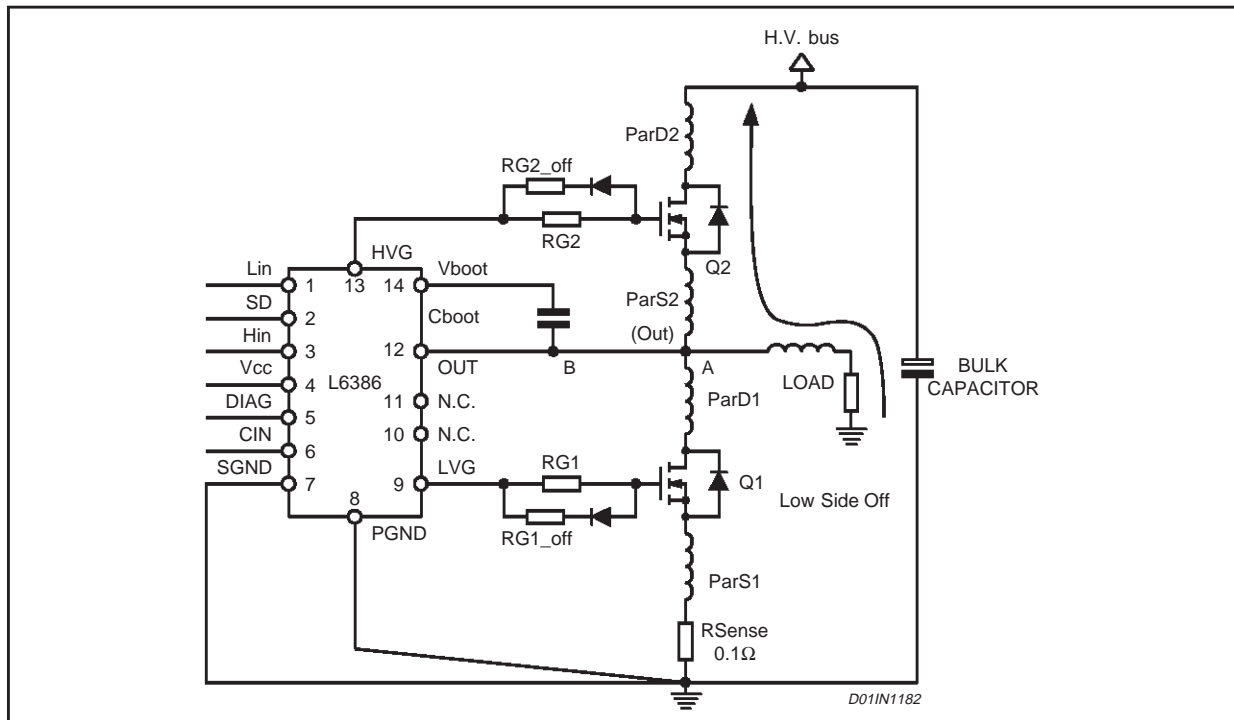
HIGH SIDE OFF-LOW SIDE TURNED ON

Figure 14. The Low side is turned On, the current that flows through the low side switch is the sum of the charge recovered by the diode (Qrr) and the load current

HIGH SIDE OFF - LOW SIDE ON

Figure 15. Now The high side freewheeling diode is reverse biased and the current that flows through the low side switch is only the load current
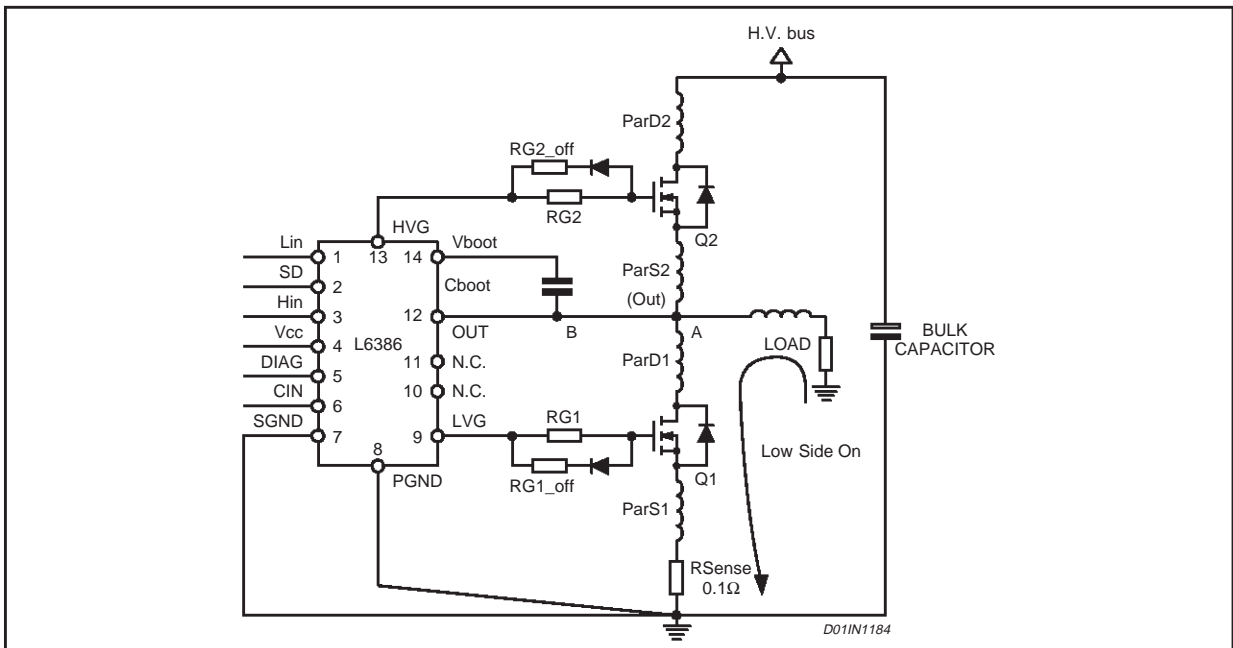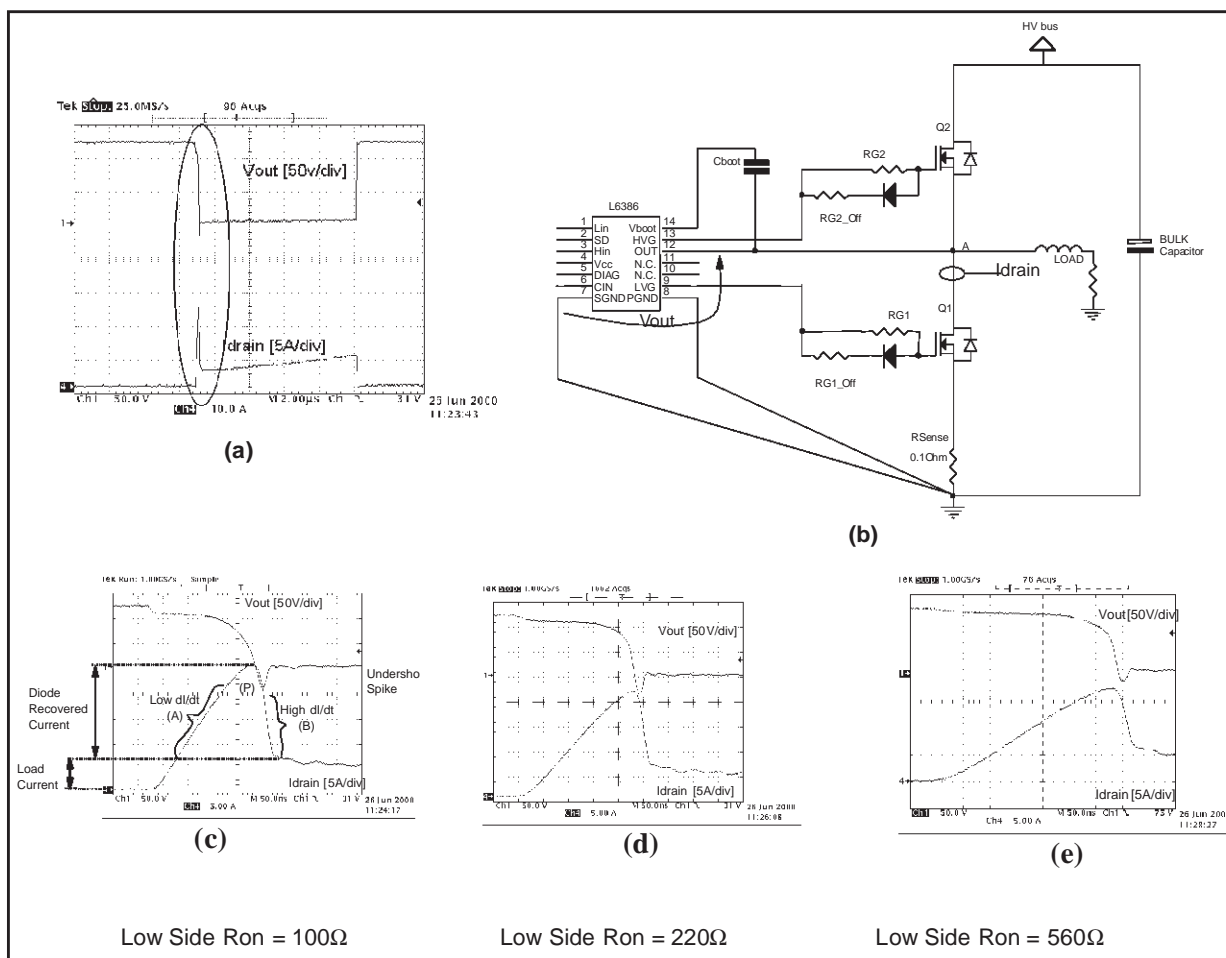
Figure 16. Undershoot caused by the freewheeling diode. The high side freewheeling diode is forward biased by the load current and the low side switch is turned On, so the current shown in the picture is the sum of the load current and the diode recovered charge.

Low Side Ron = 100Ω Low Side Ron = 220Ω Low Side Ron = 560Ω

The picture above(fig.16) shows how the high di/dt diode recovery current leads to a heavy spike below ground on the out pin. All the charge recovered by the high side diode goes through the low side switch when it turns on .The current in the low side drain ramps up with a controlled slope (slope A) that is related only to the low side turn-on speed. On the other side the slope (Slope B) is not well "limited": the high di/dt value (B) depends mainly on the diodes physical structure.

In this case the peak voltage could be reduced by acting on the PCB traces, reducing the parasitic inductance, designing wider and shorter traces. But, attention must be paid also to the diode selection. A very high value of diode recovered current slope is very difficult to manage anyway and forces to use higher values of low side turn on resistance: this for sure helps to reduce the below ground spikes, but increases the turn on speed and the switching losses. The turn on resistor value should be as low as the layout allows.

For example, referring to fig16c, if we want to limit the undershoot spike under 10V, with the same low side turn on resistance, and we have 700A/µs of dI/dt (we are talking about the second slope (B) of the current shown in the picture 16c) we need a maximum parasitic inductance of 15nH: difficult to reach. So in this case we must increase the low side turn on resistance increasing the switching losses.

The message is to reduce as much as possible the trace parasitic inductance, but also to take into account the amount of the total freewheeling diode recovered charge and the diode softness factor.

TRICKS AND LAYOUT SUGGESTIONS

Layout suggestions:

The driver can easily deal with an undershoot spike in order of -18V (measured between the IC out pin and his signal ground) for a time that must not be longer than 100ns. The guidelines to follow in order to avoid device failure related to heavy below ground spikes are:

■ Remember that the total amount of inductance and resistance exhibited is directly proportional to the trace's length and inversely proportional to its width.

■ To put both power switches of each half bridge as close as possible in order to make shortest and widest trace possible between the low side drain and the high side source. (This solution is in order to minimize the stray inductance ParD1 and ParS2 shown in fig.17)

■ Take care of the trace between the low side source, the sense resistor and the power ground reference, making it shorter and wider.(To reduce ParS1, fig.17). Remember: all the load current flows in this path!

Figure 17. Path to be optimized
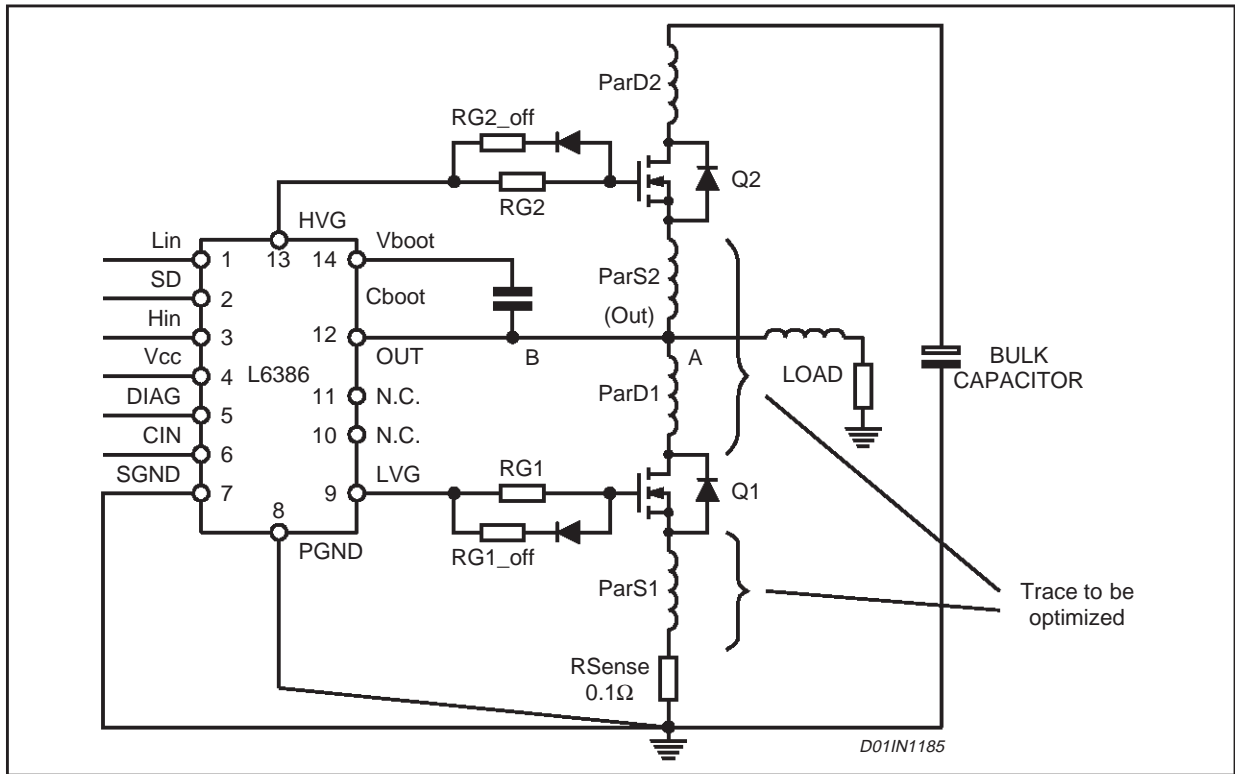
■ Use "inductance free" sense resistors.

■ Shorten the power switch lead length.

TRICKS:

■ If we are not able to reduce the below ground spikes acting only on the layout a resistor in series to the out pin as indicated in (fig. 18) is a good trick that improves the device immunity. The resistor is not additional, the part count does not change , but it is the high side turn-off resistor that is moved on the out pin. In this way we can deal with undershoot spike above -18V.

Figure 18. Placing resistance on the out pin
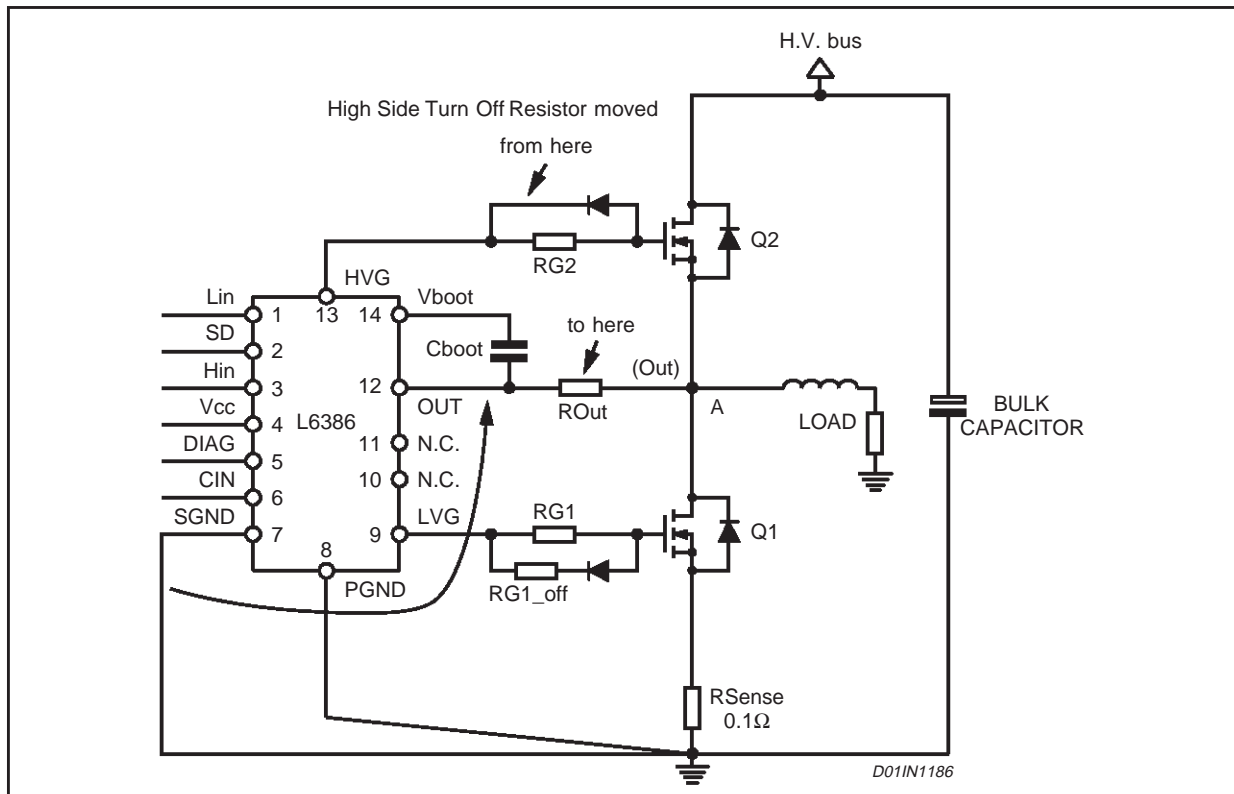
This resistor, with values between 10-220 Ohms, is not mandatory for the application, but helps to manage heavy below ground spikes. This limits the current absorbed from the IC substrate when the out pin voltage goes below the ground reference and improves the spike device immunity.
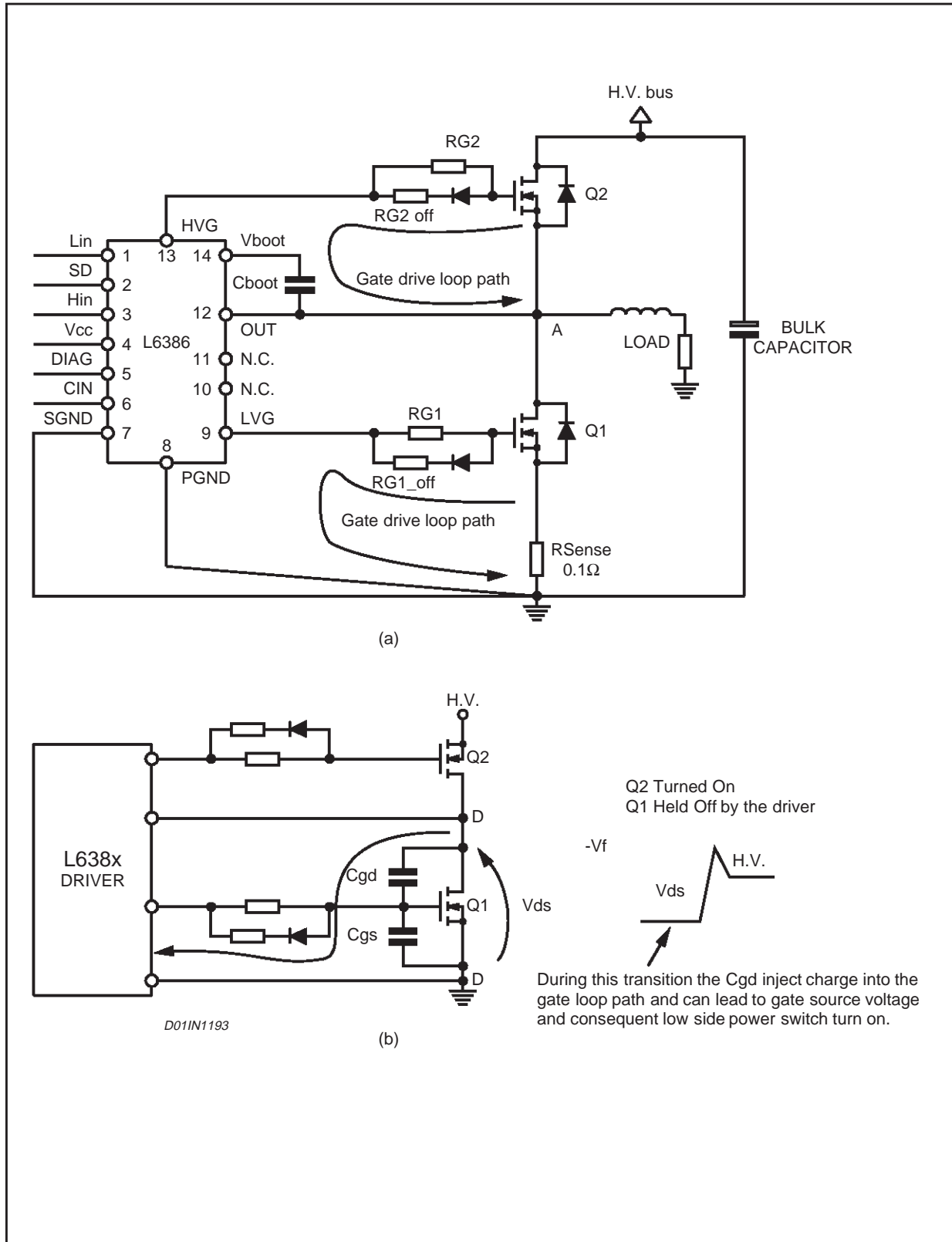
We strictly suggest avoiding high resistor values, because it is in series with the bootstrap capacitor charging path.

■ Another way to reduce the below ground spike is slowing down the switching speed by means of the gate resistor. When increasing the high side turn off series resistor the negative spikes amplitude decrease, like shown in fig. 12.

■ Pay attention selecting the freewheeling diodes, high values in terms of recovered charge can lead to high value of di/dt and then to spikes below ground on the out pin (fig.16).The only way to control this di/dt is increasing the low side turn on time by means of the turn on resistor, but this leads also to increasing in terms of switching losses.

Further suggestion:

■ The layout must also optimize the gate drive loops in order to improve mainly the power switch turn on immunity. High dV/dt values between power switch drain-source, inject current inside the gate drive path via the drain-gate capacitance. This impulsive current must be absorbed by the driver. But if the gate drive loop is not well optimized and has long and thin trace, the parasitic inductance can lead to the power switch turn on. This is called "induced turn on ".

Figure 19. (a) Gate drive loops to be optimize and (b) current injected inside the Low side gate drive loop.(the same concept is also valid for the high side gate drive loop)


(a)

(b)

Q2 Turned On
Q1 Held Off by the driver

-Vf

Vds

H.V.

During this transition the Cgd inject charge into the gate loop path and can lead to gate source voltage and consequent low side power switch turn on.

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HOW TO DEAL WITH SIGNAL GROUND AND POWER GROUND

Inside the L638x family the L6386 has two ground connections:

■ **power ground:** reference for internal low side power driver. On this ground circulate the low side gate loops current.

■ **signal ground:** reference for all the internal logic. On this reference flows only the logic supply current .

Figure 20. Internal signal ground and power ground: simplified schematic
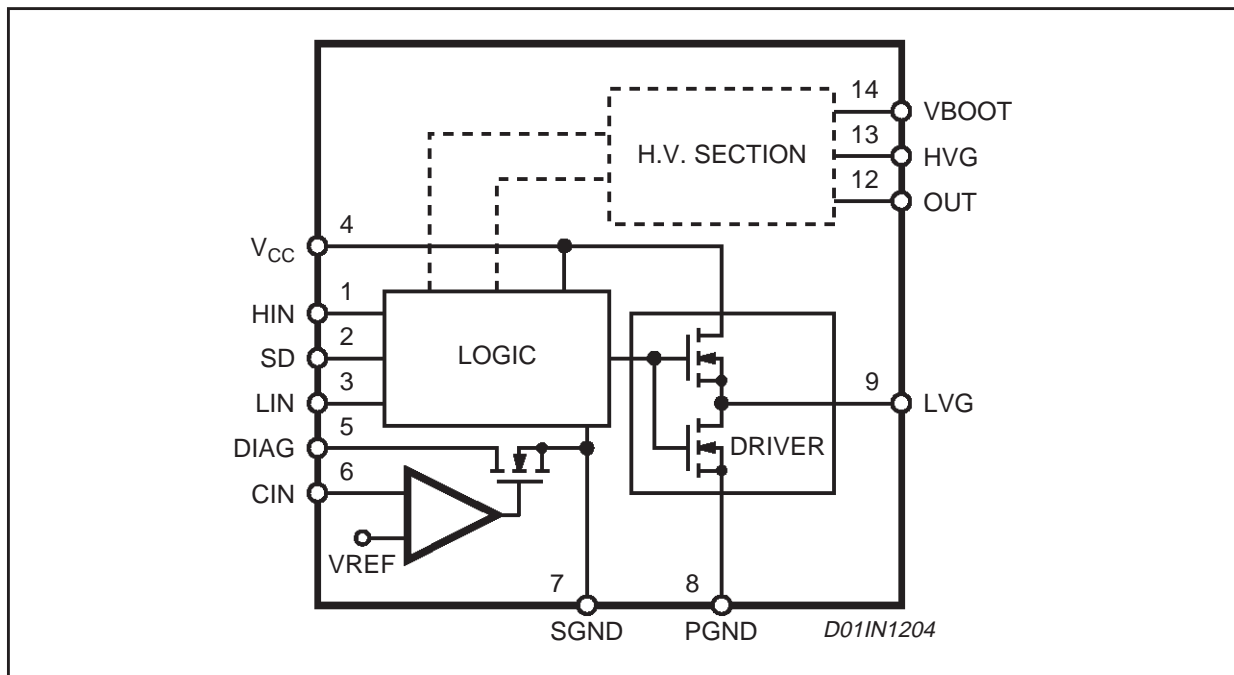
Two different grounds avoid that gate drive current flows on signal ground, leading to internal ground noise. Control ground is extremely sensitive and separated grounds help to avoid that noise generated from the low side turn-offgate drive current reaches the internal logic section: noise generated on this signal grounds will keep inside the device and affecting the IC functioning.

We can suggest two different ways to connect this ground references:

1. Signal and power ground connected together (suggested solution);
2. Signal and power ground separated.

Let's analyze both solutions:

SIGNAL AND POWER GROUND CONNECTED TOGETHER

Connection between the two grounds is done in a specific point: common end of the current sense resistor. This point must be filtered with an electrolytic capacitor connected between ground and the high voltage bus. An high voltage ceramic capacitor connected in parallel with the electrolytic one is also advisable: this help to reduce the equivalent ESR, and to smooth the high frequency voltage transient.

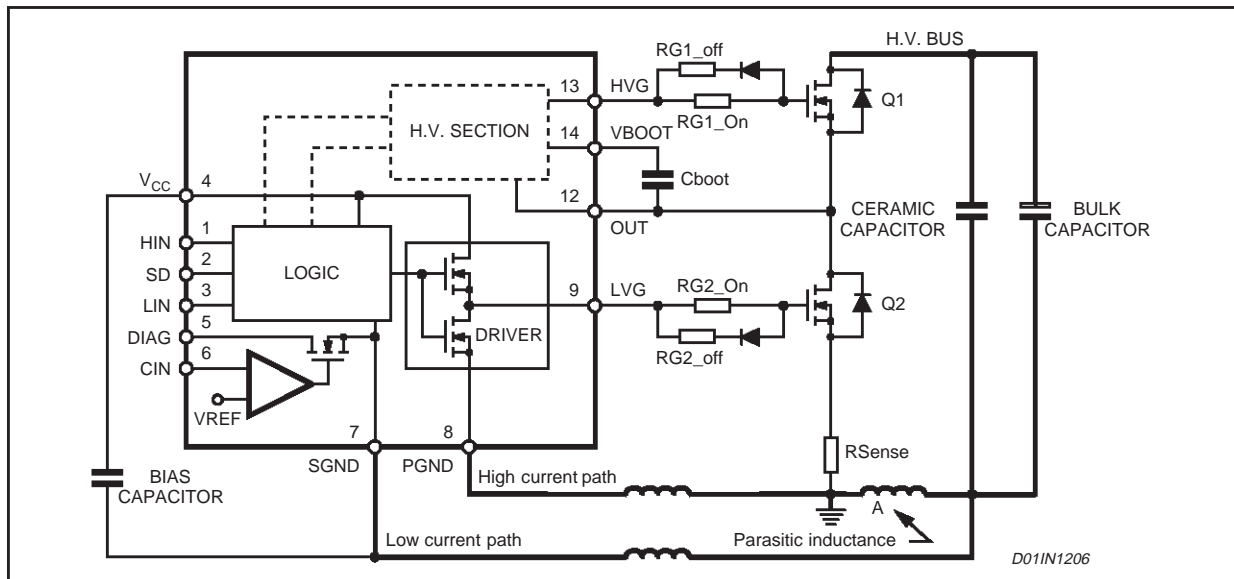**Figure 21. Signal ground and power ground connected together**
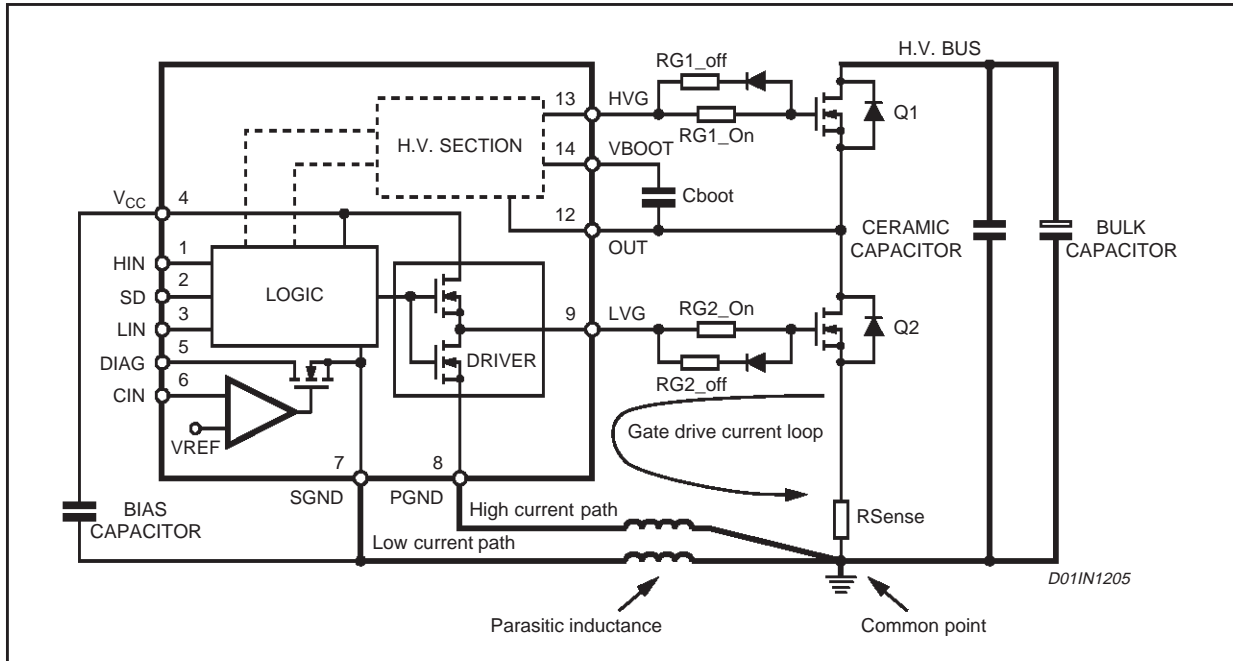
Advantages:

   o The solution proposed helps to limit the noise seen by the signal ground due the low side turn off gate current. This current flows on the path highlighted in fig. 21. Voltage transient on power ground pin due to parasitic inductance is not seen on signal ground. Remember that turn-off gate current can be up to 600mA and can lead to heavy spikes on the IC power ground.

   o Differential voltage between signal and power ground is minimized and due only to the low side gate drive current. There is no DC voltage between the two grounds but only transient voltage during the low side switch turn off. It is important to limit the transient voltage below ground on the PGND to avoid internal power drive damages.

Disadvantage:

   o PCB layout of the low side gate drive loop could be to "long". If it is not well realized, his parasitic inductance and resistance could be not negligible. This means that we need to realize shorter and wider traces in order to minimize all the parasitic elements and improve the power switch "induced turn on"immunity.

Figure 22 show a bad way to connect signal and power ground, because all the load current flows on the parasitic inductance inside the trace A, and can lead to high differential voltage between the two grounds.

Figure 22. Bad way to connect power and signal ground

In a three phase motor control, three half bridges must be used: the ground's common point for all the three sections is highlighted in the figure 21. Signal and power grounds must be connected at this point with a low inductive path (especially for the power ground connection).

Signal and power ground separated

In this solution (fig.23), power ground is connected to the low side source and the sense resistor is outside the gate drive loop. The turn off resistor is moved from the low side gate to the " power ground-source path" like shown in figure 23: the resistor limits the current absorbed from the power ground when the voltage goes below the signal one.

Values suggested are the same that are also used for the turn off resistor: in the range of 10-100 Ohms, or anyway more then 10 Ohms.

Advantages:

o noise seen by signal ground due the low side turn off gate current is limited.(As already said for the first solution)

o Low side gate drive loop is shorter if compared to the first solution (Because the sense resistor is outside of this loop).

Disadvantages:

o differential voltage between the two grounds is proportional to the load current(see fig. 24 a,b). Transient and DC voltage difference could be high and leads to device damaging. In order to avoid IC failure is mandatory put the low side turn off resistor on the path shown in fig.23: this limits the current absorbed from the power ground when his voltage goes below the signal one.

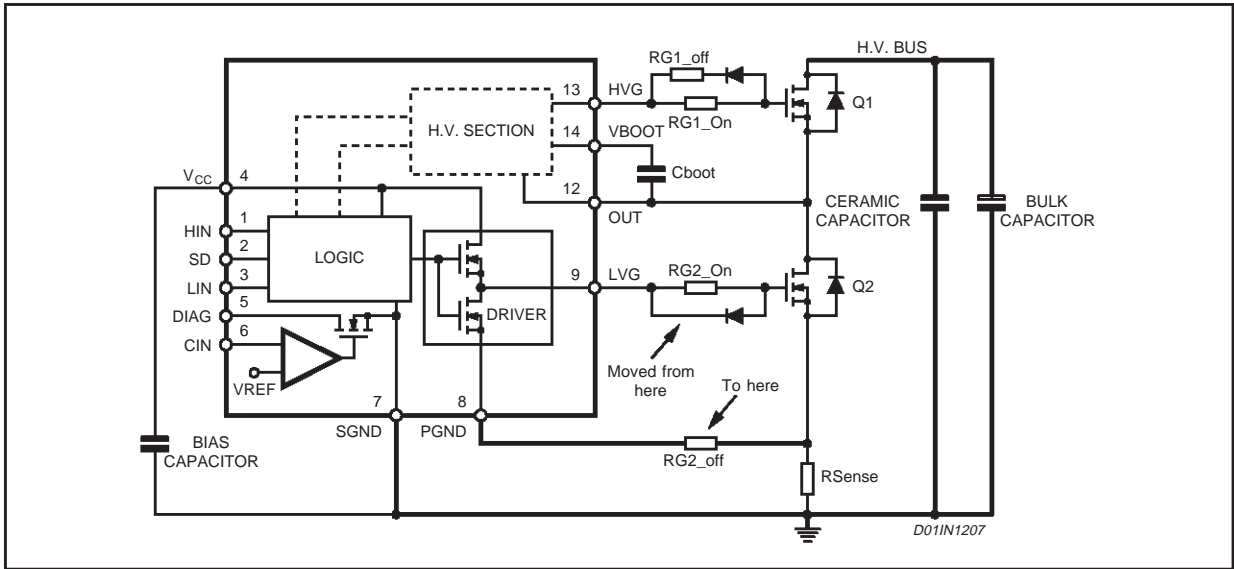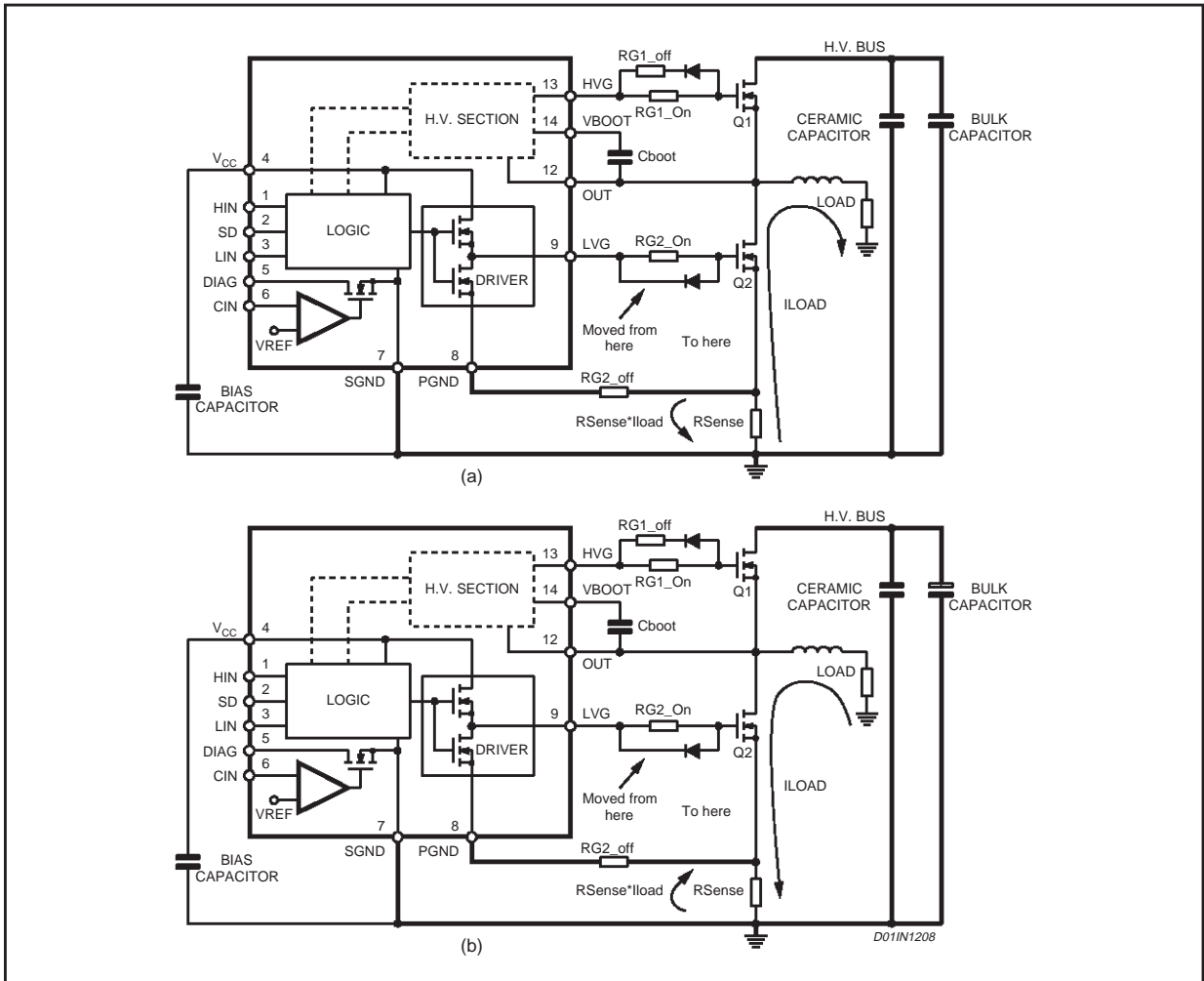**Figure 23. Power ground connected to the low side source**

Figure 24. Voltage between power and signal ground for opposite load current directions