= Preliminary =

AK4710

Low Power Single SCART Driver

FEATURES

Audio section
- ☐ THD+N: –92dB (@2Vrms)
- ☐ Dynamic Range: 96dB (@2Vrms, A-weighted)
- ☐ Full Differential or Single-ended input for Decoder DAC
- ☐ Stereo Output for TV SCART and CINCH (2Vrms)
- ☐ Ground-Referenced Output Eliminates DC-Blocking Capacitor and Mute Circuit

Video section
- ☐ Integrated LPF: –40dB@27MHz
- ☐ 6dB Gain for Outputs
- ☐ 5ch 75ohm driver
  - 4ch for SCART: CVBS/Y, R/C, G, B
  - 1ch for CINCH: CVBS
- ☐ Y/Pb/Pr Option (to 6MHz)

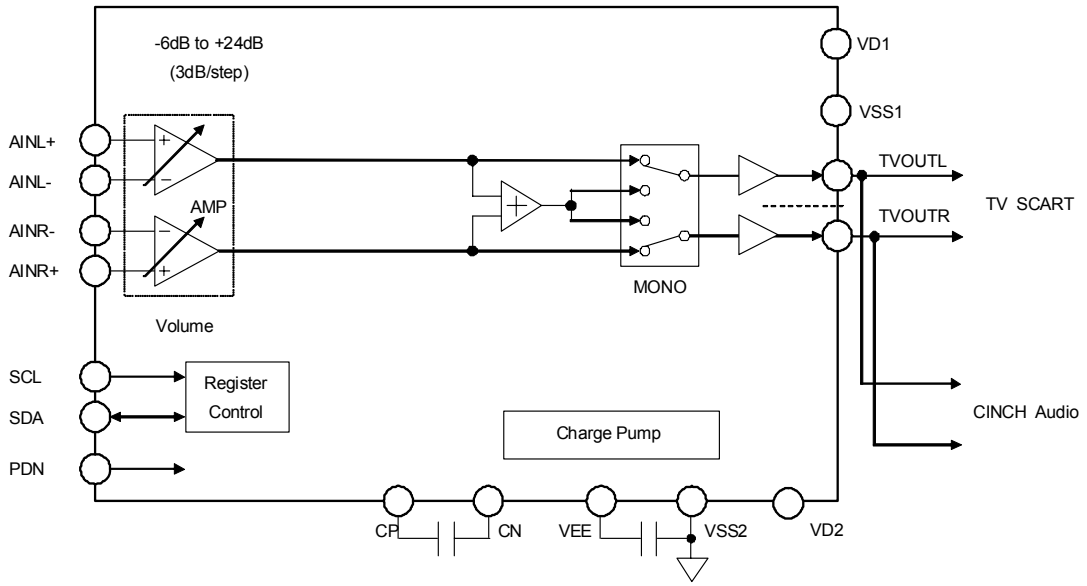
Low-power Standby

SCART pin#16(Fast Blanking), pin#8(Slow Blanking) Output Control

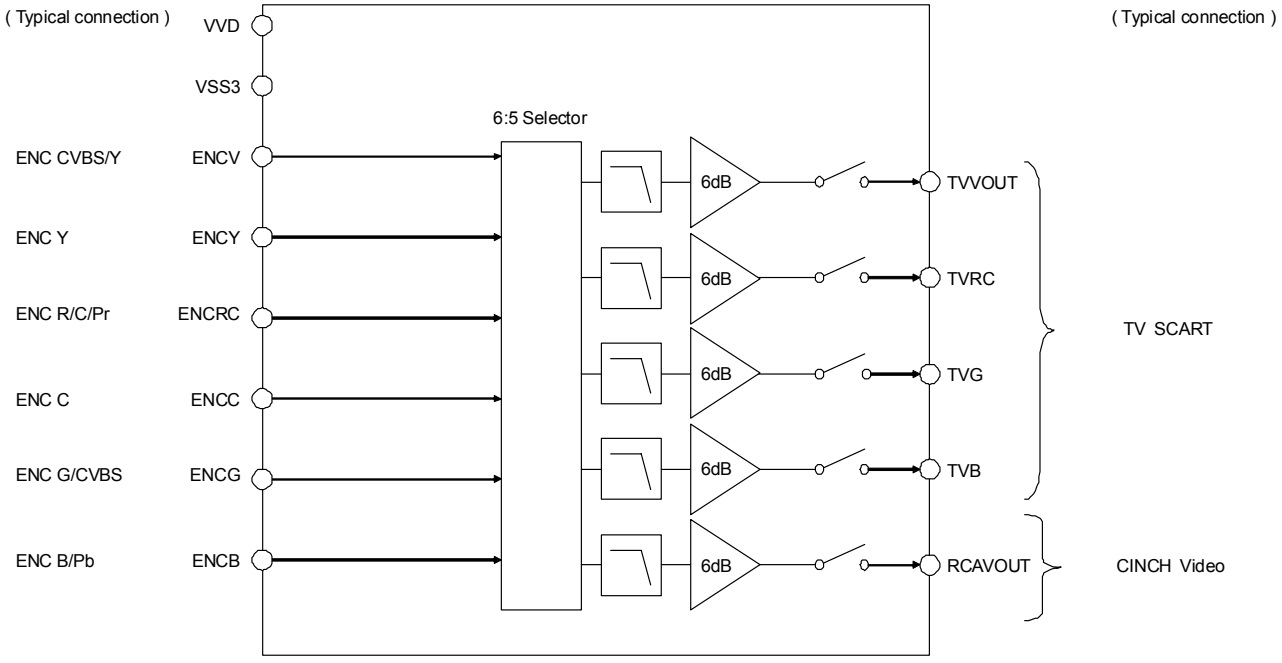
Power supply
- ☐ 3.3V+/–5% and 12V+/–5%
- ☐ Low Power Dissipation / Low Power Standby Mode

Package
- ☐ 32pin QFN (0.4mm pitch)

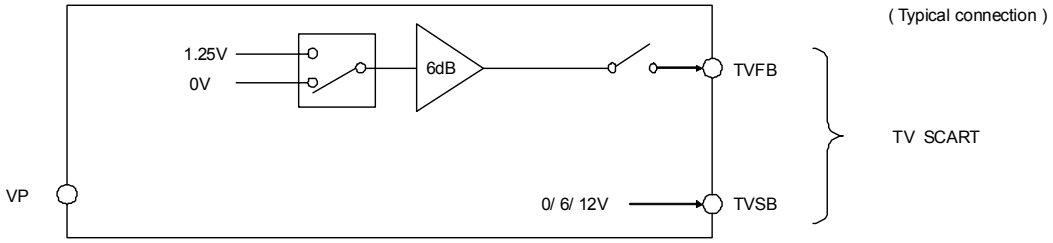
■ Block Diagram



Audio Block



Video Block



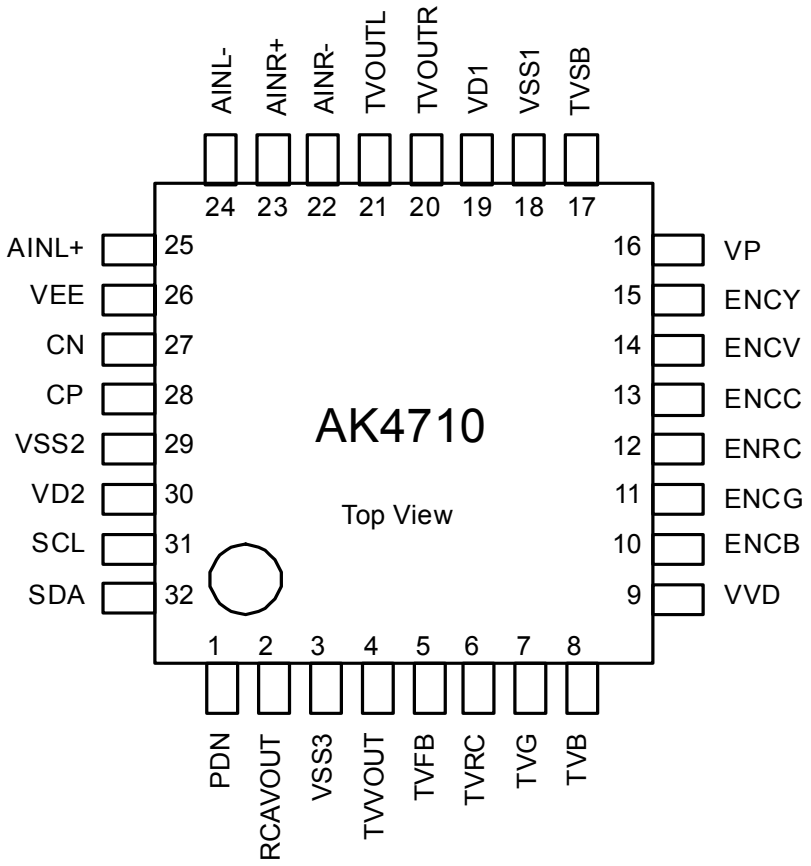
Video Blanking Block

■ Ordering Guide

AK4710EN	-10 ~ +70°C	32pin QFN (0.4mm pitch)
AKD4710	Evaluation board for AK4710	

■ Pin Layout

32pin QFN (0.4mm pitch)



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PDN	I	Power-Down Mode Pin When at "L", the AK4710 is in the power-down mode and is held in reset. The AK4710 should always be reset upon power-up.
2	RCAVOUT	O	Composite/Luminance Output Pin for RCA
3	VSS3	-	Video Ground Pin , 0V
4	TVVOUT	O	Composite/Luminance Output Pin for TV
5	TVFB	O	Fast Blanking Output Pin for TV
6	TVRC	O	Red/Chrominance Output Pin for TV
7	TVG	O	Green Output Pin for TV
8	TVB	O	Blue Output Pin for TV
9	VVD	-	Video Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS3 with a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic capacitor.
10	ENCB	I	Blue Input Pin for Encoder
11	ENCG	I	Green Input Pin for Encoder
12	ENCRC	I	Red/Chrominance Input Pin #1 for Encoder
13	ENCC	I	Chrominance Input Pin #2 for Encoder
14	ENCV	I	Composite/Luminance Input Pin #1 for Encoder
15	ENCY	I	Composite/Luminance Input Pin #2 for Encoder
16	VP	-	Blanking Power Supply Pin, 10.8V ~ 13.2V The VP pin must connect to power supply through 10ohm resistor with 0.1μF ceramic capacitor in parallel with a 1μF electrolytic capacitor to VSS1.
17	TVSB	O	Slow Blanking Output Pin for TV A 470ohm ±5% resistor must be connected between the TVSB pin and SCART connector.
18	VSS1	-	Audio Ground Pin , 0V
19	VD1	-	Audio Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS1 with a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic capacitor.
20	TVOUTR	O	Rch Analog Output Pin #2
21	TVOUTL	O	Lch Analog Output Pin #2
22	AINRN	I	Rch Negative Analog Input Pin
23	AINRP	I	Rch Positive Analog Input Pin
24	AINLN	I	Lch Negative Analog Input Pin
25	AINLP	I	Lch Positive Analog Input Pin

26	VEE	O	Negative Voltage Output Pin Connect to VSS2 with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the VSS2 pin. Non polarity capacitors can also be used.
27	CN	I	Negative Charge Pump Capacitor Terminal Pin Connect to CP with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
28	CP	I	Positive Charge Pump Capacitor Terminal Pin Connect to CN with a 1.0μF capacitor that should have the low ESR (Equivalent Series Resistance) over all temperature range. When this capacitor has the polarity, the positive polarity pin should be connected to the CP pin. Non polarity capacitors can also be used.
29	VSS2	-	Charge Pump Ground Pin , 0V
30	VD2	-	Charge Pump Power Supply Pin: 3.13V ~ 3.47V Normally connected to VSS2 with a 0.1μF ceramic capacitor in parallel with a 4.7μF electrolytic cap.
31	SCL	I	Control Data Clock Pin
32	SDA	I/O	Control Data Pin

Note: All digital input pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3= 0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply (Note 2)	VD1	–0.3	4.0	V
	VD2	-0.3	4.0	V
	VVD	–0.3	4.0	V
	VP	–0.3	14	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage(PDN pin)	VIND1	–0.3	VVD+0.3	V
Digital Input Voltage(SCL, SDA pins)	VIND2	–0.3	4.0	V
Video Input Voltage	VINV	–0.3	VVD+0.3	V
Audio Input Voltage (Note 3)	VINA	VEE-0.3	VD1+0.3	V
Ambient Operating Temperature	Ta	–10	70	°C
Storage Temperature	Tstg	–65	150	°C

Note 1. All voltages with respect to ground.

Note 2. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 3. VEE: VEE pin voltage.

The internal negative power supply generating circuit provides negative power supply(VEE).

The PDN pin, MUTE bit, control operation mode as shown in Table 2 and Table 3.

Mode			VEE pin Voltage
0	Full Power-down		0V
1	Mute		0V
2	Normal operation	No video input	0V
		Video input	-VD2+0.2V

Table 1. VEE pin voltage

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3= 0V; Note 1)

Parameter	Symbol	Min	typ	max	Units
Power Supply (Note 4)	VD1	3.13	3.3	3.47	V
	VD2	3.13	3.3	3.47	V
	VVD	3.13	3.3	3.47	V
	VP	10.8	12	13.2	V

Note 1. All voltages with respect to ground.
Note 4. VVD must be connected to the same voltage.

*AKM assumes no responsibility for the usage beyond recommended operating conditions in this datasheet.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C; VP=12V, VD1=VD2=VVD= 3.3V)

Power Supplies	min	typ	max	Units
Power Supply Current				
Normal Operation (PDN = "H") (Note 5)				
VD1+VD2+VVD		386	TBD	μA
VP		48	TBD	μA
Power-Down Mode (PDN = "L") (Note 6)				
VD1+VD2		0	TBD	μA
VVD		0	TBD	μA
VP		48	TBD	μA

Note 5. All video outputs active. No signal, no load for A/V switches, refer to the Table 3.
Note 6. All digital inputs are held at VVD or VSS3. No signal, no load for A/V switches.

DIGITAL CHARACTERISTICS

(Ta = 25°C; VD1=VD2=VVD= 3.13 ~ 3.47V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VVD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VVD	V
Low-Level Output Voltage (SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

ANALOG CHARACTERISTICS (AUDIO)

(Ta=25°C; VP=12V, VD1=VD2=VVD =3.3V; Signal Frequency=1kHz; Measurement frequency=20Hz ~ 20kHz; R_L ≥4.5kΩ; 0dB=2Vrms output; Volume=0dB, unless otherwise specified)

Parameter	min	typ	max	Units
Analog Input: (AINL+/AINL-/AINR-/AINR+ pins)				
Analog Input Characteristics				
Input Voltage (AIN+) – (AIN–), (Note 7)			2.0	Vrms
Input Resistance (AINL+, AINR+ pins)	85	120		kΩ
Input Resistance (AINL-, AINR- pins)	85	120	-	kΩ
Stereo/Mono Output: (TVOUTL/TVOUTR pins) (Note 8)				
Analog Output Characteristics				
Volume Step Width	2.3	3.0	3.7	dB
THD+N (at 2Vrms output, Note 10, Note 12)		–92	-80	dB
Dynamic Rang (–60dB Output, A-weighted, Note 10)	92	96		dB
S/N (A-weighted, Note 10, Note 14)	92	96		dB
Interchannel Isolation (Note 10, Note 11)	80	90		dB
Interchannel Gain Mismatch (Note 10, Note 11)	-0.5	0	+0.5	dB
DC offset (Note 13)	-5	0	+5	mV
Gain Drift	-	200	-	ppm/°C
Load Resistance TVOUTL/R	4.5			kΩ
Load Capacitance TVOUTL/R			20	pF
Output Voltage (Note 9)	1.8	2	2.2	Vrms
Power Supply Rejection (PSR) (Note 15)	-	50		dB

Note 7. f = 1kHz, THD+N < -80dB, gain = 0dB(Volume=0dB)

Note 8. Measured by Audio Precision System Two Cascade.

Note 9. The output level of the internal AMP with volume should be less than 2Vrms.

Note 10. Analog In to TVOUT. Path : AINL+/– → TVOUTL, AINR+/– → TVOUTR,Volume0dB.
At 2Vrms single input, TDH+N is -91dB (typ), on path AINL+ → TVOUTL, AINR+ → TVOUTR, Volume=0dB

Note 11. Between TVOUTL and TVOUTR with analog inputs AINL+/–, AINL/R+/–, 1kHz/0dB.
Inter-channel crosstalk is -80dB (typ), at 20Hz~20kHz other than 1kHz.

Note 12. -79dB (typ) referred to 0.5Vrms output level at Volume=+24dB
: path = AIN+/- → TVOUT.

Note 13. Analog In to TVOUT. Volume=0dB
Path : AINL+/– → TVOUTL, AINR+/– → TVOUTR

Note 14. 82dB (typ) referred to 0.5Vrms output level at Volume=+24dB
: path = AIN+/- → TVOUT.
84dB (typ), referred to 0.5Vrm output level at Volume = +21dB.

Note 15. The PSR is applied to VD1 and VD2 with 1kHz, 100mV.

ANALOG CHARACTERISTICS (VIDEO)

(Ta = 25°C; VP = 12V, VD1=VD2= VVD = 3.3V; unless otherwise specified.)

Parameter	Conditions	min	typ	max	Units
Sync Tip Clamp Voltage	at output pin.		0.20		V
R/G/B Clamp Voltage	at output pin.		0.20		V
Pb/Pr Clamp Voltage	at output pin.		1.44		V
Chrominance Bias Voltage	at output pin.		1.44		V
Gain	Input = 0.3Vp-p, 100kHz	5.5	6	6.5	dB
Interchannel Gain Mismatch	TVRC, TVG, TVB. Input = 0.3Vp-p, 100kHz.	-0.5	-	0.5	dB
Frequency Response	Input=0.3Vp-p, C1=C2=0pF. 100kHz to 6MHz. at 10MHz. at 27MHz.	-1.0	 -3 -40	0.5 -20	dB dB dB
Group Delay Distortion	At 4.43MHz with respect to 1MHz.			20	ns
Input Impedance	Chrominance input (internally biased)	80	100	-	kΩ
Input Signal	f = 100kHz, maximum with distortion < 1.0%, gain = 6dB.	-	-	1.25	Vpp
Load Resistance	(Figure 1)	150	-	-	Ω
Load Capacitance	C1 (Figure 1) C2 (Figure 1)			400 15	pF pF
Dynamic Output Signal	f = 100kHz, maximum with distortion < 1.0%	-	-	2.5	Vpp
Y/C Crosstalk	f = 4.43MHz, 1Vp-p input. Among TVVOUT, TVRC and RCAVOUT outputs.	-	–50	-	dB
S/N	Reference Level = 0.7Vp-p, CCIR 567 weighting. BW = 15kHz to 5MHz.	-	74	-	dB
Differential Gain	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	0.6	-	%
Differential Phase	0.7Vpp 5steps modulated staircase. chrominance &burst are 280mVpp, 4.43MHz.	-	1.4	-	Degree

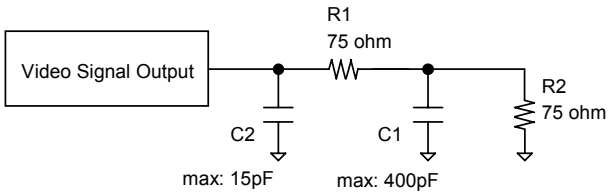


Figure 1. Load Resistance R1+R2 and Load Capacitance C1/C2.

SWITCHING CHARACTERISTICS

(Ta = 25°C; VP = 10.8 ~ 13.2V, VD1=VD2= VVD = 3.13 ~ 3.47V)

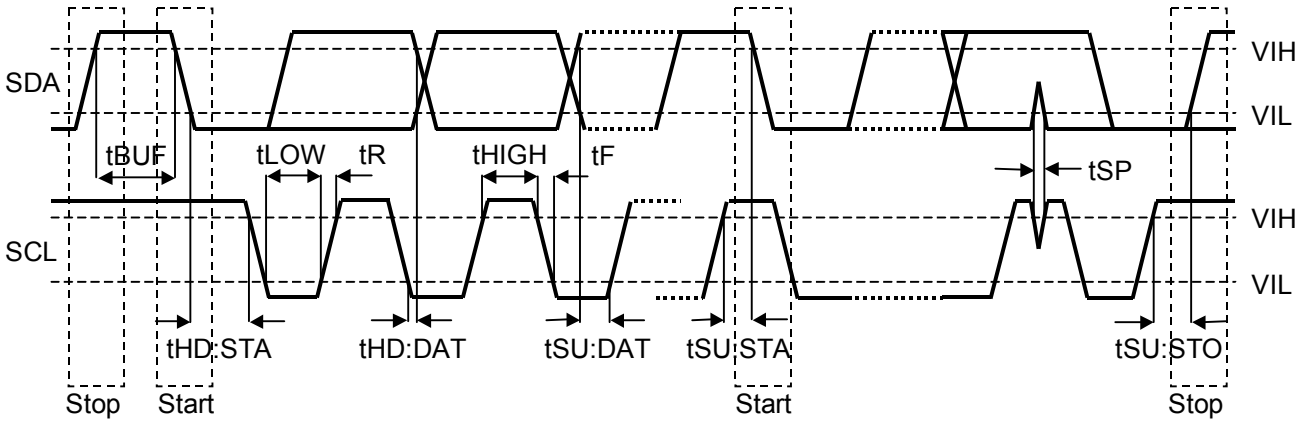
Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 16)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF
Reset Timing					
PDN Pulse Width (Note 17)	tPD	150			ns

Note 16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

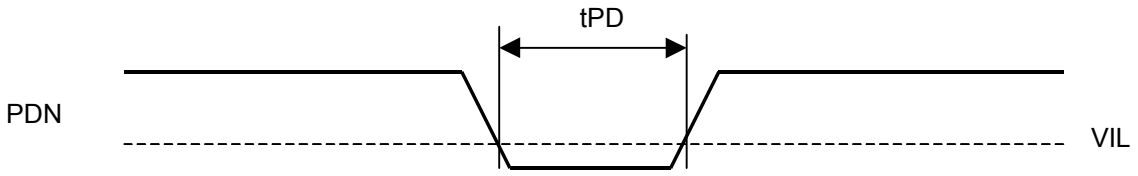
Note 17. The AK4710 should be reset once by bringing the PDN pin = “L” after all power supplies are supplied.

Note 18. I^2C-bus is a trademark of NXP B.V.

■ **Timing Diagram**



I^2C Bus mode Timing



Power-down Timing

OPERATION OVERVIEW

1. System Reset and Power-down Options

The AK4710 should be reset once by bringing the PDN pin = "L" after all power supplies are supplied. The AK4710 has several operation modes. The PDN pin and MUTE bit, control operation mode as shown in Table 2and Table 3.

■ System Reset and Full Power-down Mode

The AK4710 should be reset once by bringing the PDN pin = "L" after all power supplies are supplied.

PDN pin: Power down pin
L: Full Power-down Mode. Power-down, reset and initializes control registers.
H: Device active.

■ Mute Mode

When the MUTE bit = "1", the audio outputs settle to VSS (0V, typ) and the charge pump circuit is in power down mode.

MUTE bit (00H D1): Audio output control
0: Normal operation.
1: All audio outputs to GND (default)

Mode	PDN pin	MUTE bit	Mode
0	L	x	Full Power-down
1	H	1	Mute (Note 19) (AMP power down)
2	H	0	Normal operation (AMP operation)

Note 19. TVOUTL/R are muted by Mute bit in the default state.

Table 2. Operation Mode Settings (x: Don't Care)

Mode			Register Control	Audio Charge pump	Video Output	TVFB	TVSB	Power Consumption (typ.) (Note 20)
0	Full Power-down		NOT available	Power down	Hi-Z	Hi-Z	Pull -down (Note 21)	0.6mW
1	Mute (AMP power down)	No Video Input	Available			Active	Active	1.86mW
		Video Input			Hi-Z/ Active			228mW
2	Normal operation (AMP operation)	No video input			Hi-Z			1.86mW
		Video input		Active	Hi-Z/ Active			250mW

Note 20. 1kHz 2Vrms output with 4.5kΩ load at all audio output pins.
47.46 IRE at all video inputs corresponding to all video output pins with 150Ω load.
Note 21. Internally pulled down by 120kΩ (typ) resistor.

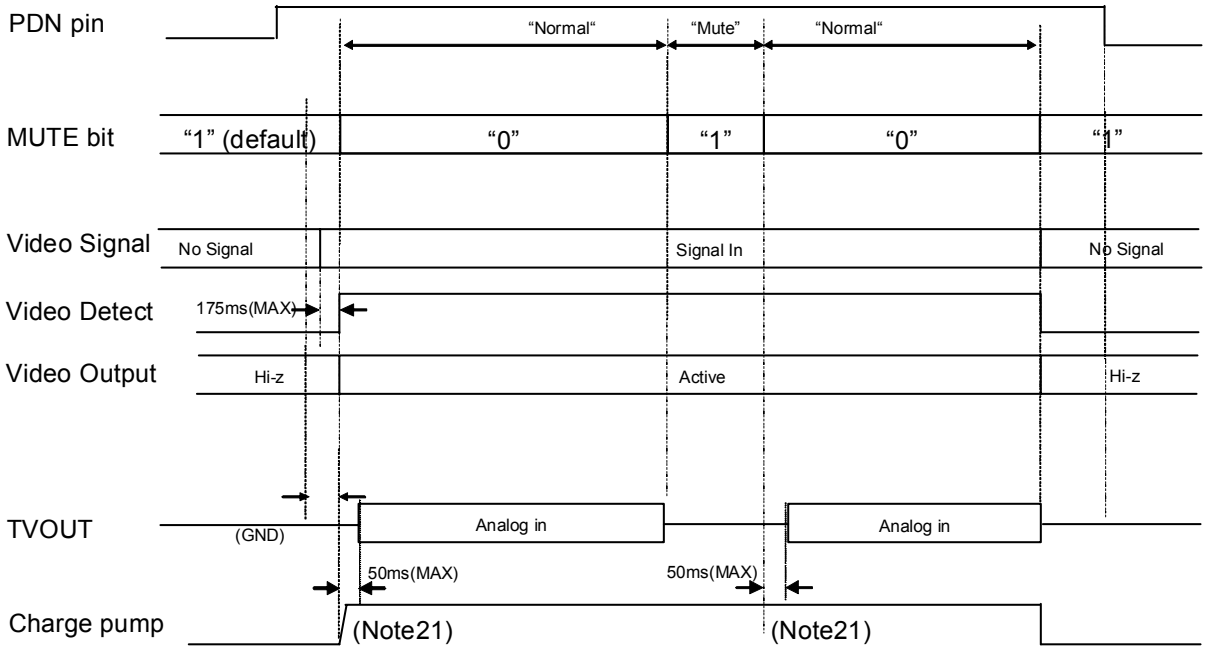
Table 3. Status of Each Operation Modes

■ Normal Operation Mode

To change analog switches, set the MUTE bit to “0”. The AK4710/11 is in power-down mode until the PDN pin = “H”. The Figure X shows an example of the system timing at the power-down and power-up by the PDN pin.

■ Typical Operation Sequence

Figure 2 shows an example of the system timing at normal operation mode.



Note 22. Mute the analog outputs externally if click noise affects the system.

Figure 2. Typical Operating Sequence

2. Audio Block

■ Volume Control (11-Level Volume)

The AK4710 has an 11-level volume control as shown in Table 4. The volume reflects the change of register value immediately.

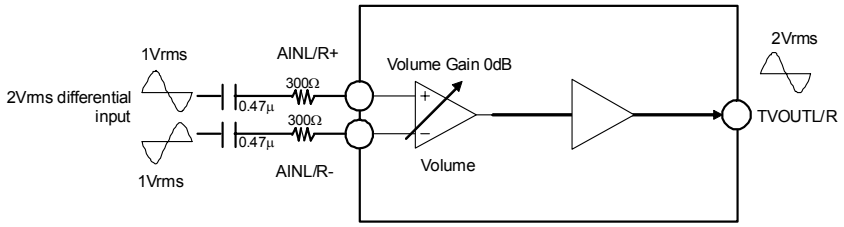


Figure 3. Volume (Volume Gain=0dB: default), Full Differential Stereo Input

(0DH: D6-D3)

VOL3	VOL2	VOL1	VOL0	Volume Gain	Output Level (Typ)
1	1	x	x	--	Reserved
1	0	1	1	+24dB	2Vrms (with 0.13Vrms differential input)
1	0	1	0	+21dB	-
1	0	0	1	+18dB	2Vrms (with 0.25Vrms differential input)
1	0	0	0	+15dB	-
0	1	1	1	+12dB	2Vrms (with 0.5Vrms differential input)
0	1	1	0	+9dB	-
0	1	0	1	+6dB	2Vrms (with 1Vrms differential input)
0	1	0	0	+3dB	-
0	0	1	1	0dB	2Vrms (with 2Vrms differential input: default)
0	0	1	0	-3dB	-
0	0	0	1	-6dB	1Vrms (with 2Vrms differential input)
0	0	0	0	Mute	-

(x: Don't care)

Table 4. Volume, Full Differential Stereo Input

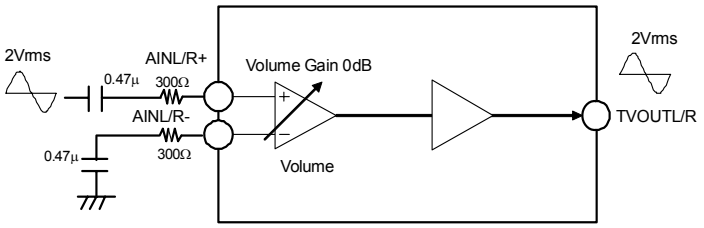


Figure 4. Volume (Volume Gain=0dB:default), Single-ended Input

(0DH: D6-D3)

VOL3	VOL2	VOL1	VOL0	Volume Gain	Output Level (Typ)
1	1	x	x	--	Reserved
1	0	1	1	+24dB	2Vrms (with 0.13Vrms input)
1	0	1	0	+21dB	-
1	0	0	1	+18dB	2Vrms (with 0.25Vrms input)
1	0	0	0	+15dB	-
0	1	1	1	+12dB	2Vrms (with 0.5Vrms input)
0	1	1	0	+9dB	-
0	1	0	1	+6dB	2Vrms (with 1Vrms input)
0	1	0	0	+3dB	-
0	0	1	1	0dB	2Vrms (with 2Vrms input: default)
0	0	1	0	-3dB	-
0	0	0	1	-6dB	1Vrms (with 2Vrms input)
0	0	0	0	Mute	-

(x: Don't care)

Table 5. Volume, Single-ended Input

■ Analog output block

The AK4710 has a charge pump circuit generating negative power supply rail from a 3.3V(typ) power supply. (Figure 5) It allows the AK4710 to output audio signal centered at VSS (0V, typ) as shown in Figure 6. The negative power generating circuit (Figure 5) needs 1.0uF capacitors (Ca, Cb) with low ESR (Equivalent Series Resistance). When using capacitors with a polarity, the positive side should be connected to CP and VSS2 for capacitor Ca and Cb, respectively. When the MUTE bit = "1", the charge pump circuit is in power down mode and its analog outputs become VSS (0V, typ).

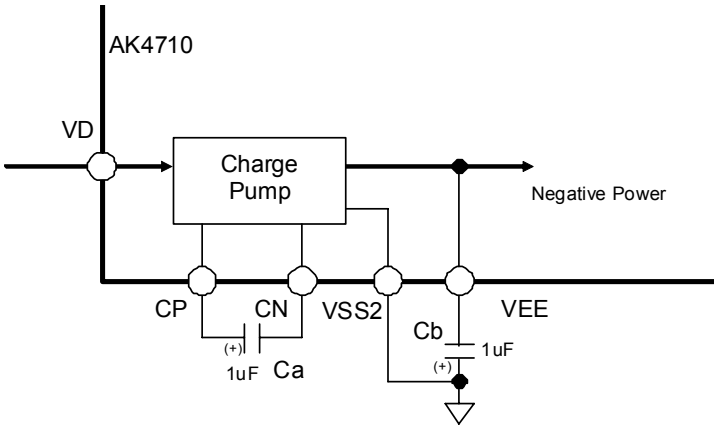


Figure 5. Negative Power Generate Circuit

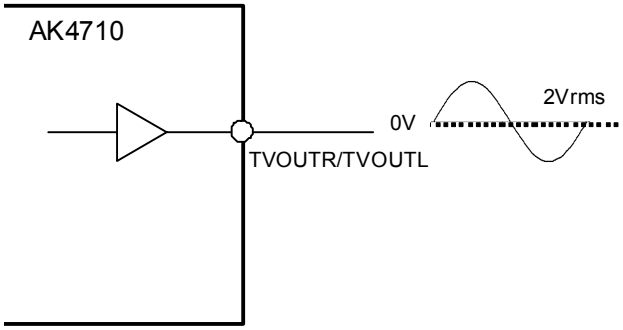


Figure 6. Audio Signal Output

3. Video Block

■ Video Switch Control

The AK4710 has switches for TV. Each switch can be controlled via the registers independently.

(04H: D1-D0)

Mode	VTV1-0 bit	Source of TVVOUT pin	Source of TVRC pin	Source of TVG pin	Source of TVB pin
Shutdown (default)	00	(Hi-Z)	(Hi-Z)	(Hi-Z)	(Hi-Z)
Encoder CVBS+RGB or Encoder YPbPr	01	ENCV pin (Encoder CVBS or Y)	ENCRC pin (Encoder Red,C or Pb)	ENCG pin (Encoder Green or Y)	ENCB pin (Encoder Blue or Pr)
Encoder Y/C 1	10	ENCV pin (Encoder Y)	ENCRC pin (Encoder C)	(Hi-Z)	(Hi-Z)
Encoder Y/C 2	11	ENCY pin (Encoder Y)	ENCC pin (Encoder C)	(Hi-Z)	(Hi-Z)

Table 6. TV Video Output (Note 23)

(04H: D4-D3)

Mode	RCA1-0 bit	Source of RCAVOUT pin
Shutdown (default)	00	(Hi-Z)
Encoder CVBS	01	ENCV pin
Encoder CVBS	10	ENCY pin
(Reserved)	11	-

Table 7. RCA Video Output (Note 23)

Note 23. When input the video signals via the ENCRC pin, set CLAMP1-0 bits respectively.

■ Video Output Control (05H: D6-D0,)

Each video output can be set to Hi-Z individually via the control registers.

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
RCAV: RCAVOUT output control
TVFB: TVFB output control
0: Hi-Z. (default)
1: Active.

■ Clamp and DC-restore Circuit Control (06H: D7-D3)

Each CVBS and Y input has a sync tip clamp circuit. The DC-restore circuit has two clamp voltages; 0.20V(typ) and 1.44V(typ) to support both RGB and YPbPr signal. They correspond to 0.10V(typ) and 0.72V(typ) at the SCART connector when matched by 75Ω resistors. CLAMP1 and CLAMPB bits select the input circuit for both the ENCRC pin (Encoder Red/Chroma) and the ENCB pin (Encoder Blue), and CLAMP2 bit selects the input circuit for the ENCG pin. VCLP1-0 bits select the sync source of DC- restore circuit.

CLAMPB	CLAMP1	ENCRC Input Circuit	ENCB Input Circuit	note	
0	0	DC restore clamp active (0.20V at sync timing/output pin)	DC restore clamp active (0.20V at sync timing/output pin)	for RGB	(default)
0	1	Biased (1.44V at sync timing/output pin)	DC restore clamp active (0.20V at sync timing output pin)	for Y/C	
1	0	DC restore clamp active (1.44V at sync timing/output pin)	DC restore clamp active (1.44V at sync timing/output pin)	for Y/Pb/Pr	
1	1	(reserved)	(reserved)		

Table 8. DC-restore Control for Encoder Input

CLAMP2	ENCG Input Circuit	note	
0	DC restore clamp active (0.20V at sync timing/output pin)	for RGB	(default)
1	Sync tip clamp active (0.20V at sync timing/output pin)	for Y/Pb/Pr	

Note: When the VTV1-0 bits = “01” (source for TV = Encoder CVBS /RGB), TVG bit = “1” (TVG = active) and VCLP1-0 bits = “11” (DC restore source = ENCG), the sync tip is selected even if the CLAMP2 bit = “0”.

Table 9. DC-restore Control for Encoder Green/Y Input

VCLP1-0: DC restore source control

VCLP1	VCLP0	Sync Source of DC Restore	
0	0	ENCV	(default)
0	1	ENCY	
1	0	(Reserved)	
1	1	ENCG	

Table 10. DC-restore Source Control

4. Blanking Control

The AK4710 supports Fast Blanking signals and Slow Blanking (Function Switching) signals for TV SCART.

■ Input/Output Control for Fast/Slow Blanking

FB: TV Fast Blanking output control (07H: D1-D0)

Input		Output
FB1 bit	FB0 bit	TVFB pin Output Level
0	0	0V (default)
0	1	2V<, 2.5V(typ) at 150Ω load
1	0	(Reserved)
1	1	(Reserved)

Table 11. TV Fast Blanking Output (Note: minimum load is 150Ω)

SBT1-0: TV Slow Blanking output control (07H: D3-D2)

Input		Output
SBT1 bit	SBT0 bit	TVSB pin Output Level
0	0	<2V (default)
0	1	4.73V <, < 7V
1	0	(Reserved)
1	1	10V<

Table 12. TV Slow Blanking Output (Note: minimum load is 10kΩ)

5. Control Interface (I^2C-bus Control)

1. WRITE Operations

Figure 7 shows the data transfer sequence in I^2C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 13). After the START condition, a slave address is sent. This address is 7bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010001". If the slave address match that of the AK4710, the AK4710 generates the acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 15). A "1" for R/W bit indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed. The second byte consists of the address for control registers of the AK4710. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 9). The data after the second byte contain control data. The format is MSB first, 8bits (Figure 10). The AK4710 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 13).
The AK4710 can execute multiple one byte write operations in a sequence. After receipt of the third byte, the AK4710 generates an acknowledge, and awaits the next data again. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 0DH prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 15) except for the START and the STOP condition.

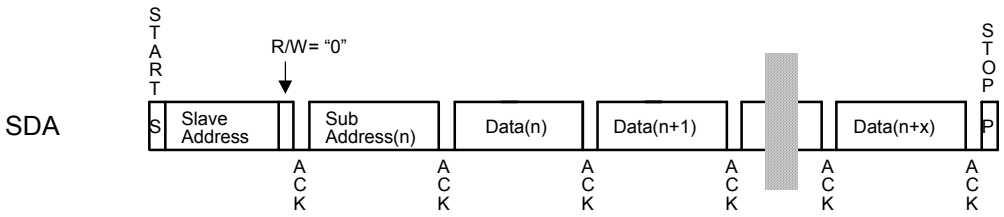


Figure 7. Data transfer sequence at the I^2C-bus mode

0	0	1	0	0	0	1	R/W

Figure 8. The first byte

0	0	0	A4	A3	A2	A1	A0

Figure 9. The second byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 10. Byte structure after the second byte

2. READ Operations

Set R/W bit = "1" for READ operations. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt the first data word. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4710 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

2-1. CURRENT ADDRESS READ

The AK4710 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4710 generates an acknowledge, transmits 1byte data which address is set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4710 discontinues transmission.

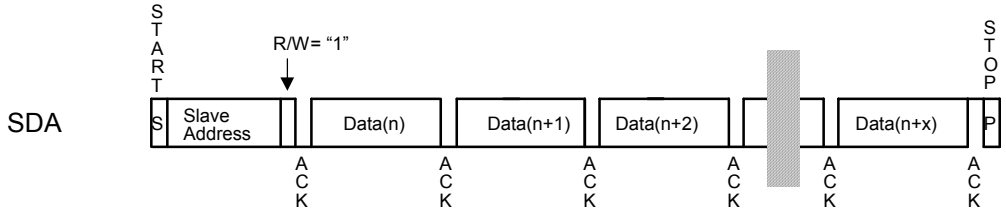


Figure 11. CURRENT ADDRESS READ

2-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4710 generates an acknowledge, 1-byte data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generate the stop condition, the AK4710 discontinues transmission.

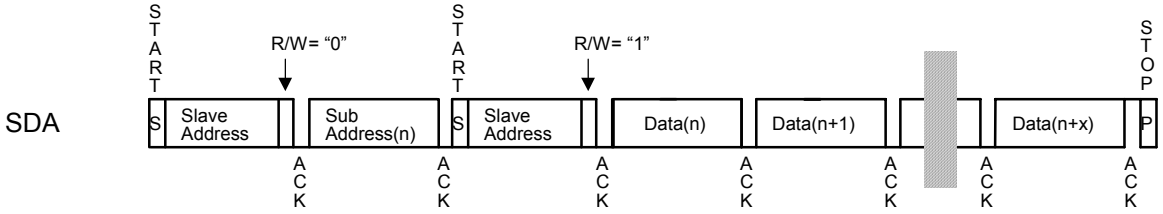


Figure 12. RANDOM ADDRESS READ

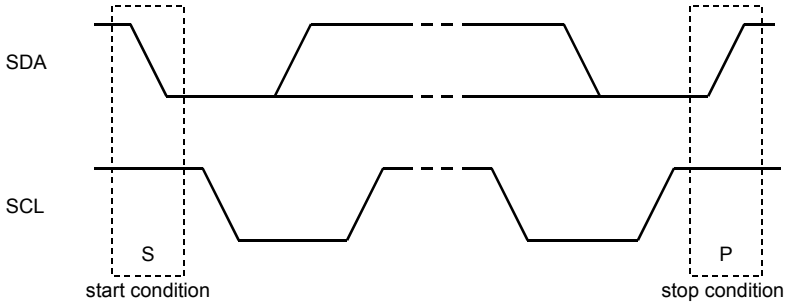


Figure 13. START and STOP Conditions

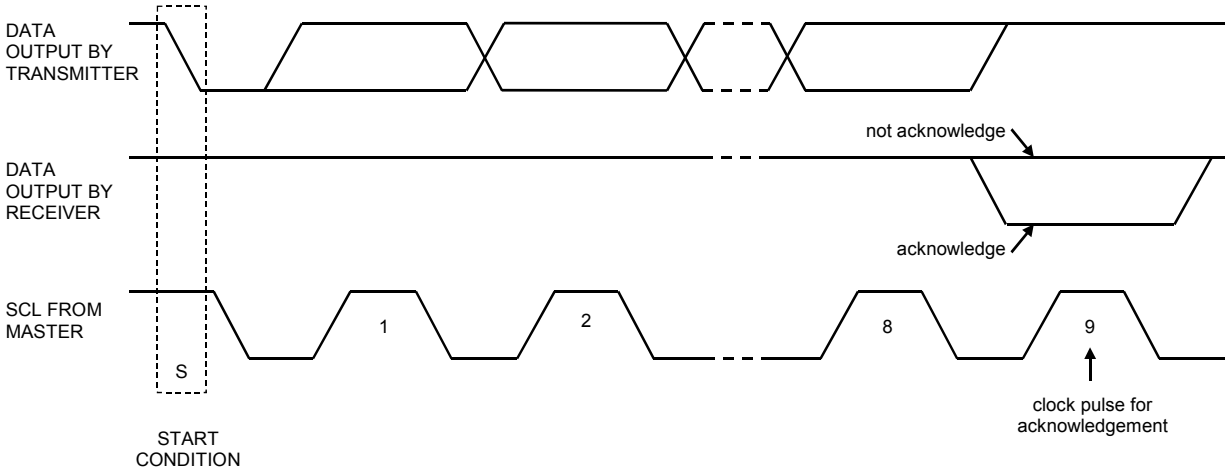


Figure 14. Acknowledge on the I^2C-bus

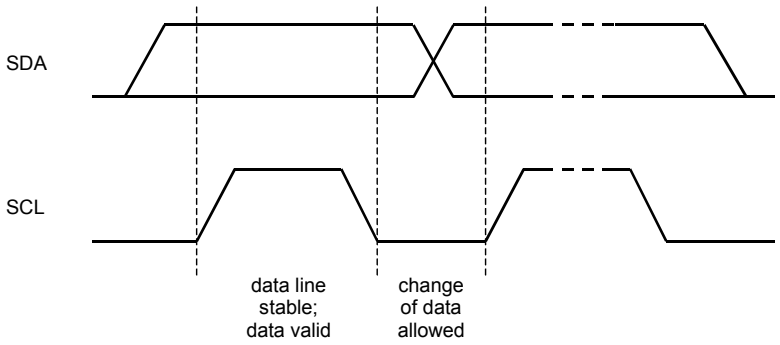


Figure 15. Bit transfer on the I^2C-bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	1	0	MUTE	1
01H	Switch	1	0	0	1	MONO	1	0	1
02H	Reserve	0	0	0	0	0	0	0	0
03H	Zerocross	0	0	CAL	0	0	1	1	1
04H	Video switch	0	0	0	RCA1	RCA0	1	VTV1	VTV0
05H	Video output enable	0	TVFB	0	RCAV	TVB	TVG	TVR	TVV
06H	Video volume/clamp	CLAMPB	VCLP1	VCLP0	CLAMP2	CLAMP1	1	0	0
07H	S/F Blanking control	0	0	0	0	SBT1	SBT0	FB1	FB0
08H	Reserve	0	0	0	0	0	0	0	0
09H	Reserve	0	0	0	0	0	0	0	0
0AH	Reserve	0	0	0	0	0	0	1	1
0BH	Reserve	0	0	0	0	0	0	0	0
0CH	Reserve	0	0	0	0	0	0	0	0
0DH	Volume	0	VOL3	VOL2	VOL1	VOL0	1	1	1

When the PDN pin goes “L”, the registers are initialized to their default values.
While the PDN pin = “H”, all registers can be accessed.
Do not write any data to the register over 0DH.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control	0	0	0	0	1	0	MUTE	1
R/W		R/W							
Default		0	0	0	0	1	0	1	1

MUTE: Audio output control
0: Normal operation
1: ALL Audio outputs to GND (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Switch	1	0	0	1	MONO	1	0	1
R/W		R/W							
Default		1	0	0	1	0	1	0	1

MONO: Mono select for TVOUTL/R pins
0: Stereo. (default)
1: Mono. (L+R)/2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Volume Control	0	0	CAL	0	0	1	1	1
R/W		R/W							
Default		0	0	1	0	0	1	1	1

CAL: Offset calibration Enable
0: Offset calibration disable.
1: Offset calibration enable (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Video switch	0	0	0	RCA1	RCA0	1	VTV1	VTV0
R/W		R/W							
Default		0	0	0	1	1	1	0	0

VTV1-0: Selector for TV video output
Refer to Table 6.

RCA1-0: Selector for RCA video output
Refer to Table 7.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Output Enable	0	TVFB	0	RCAV	TVB	TVG	TVR	TVV
R/W		R/W							
Default		0	0	0	0	0	0	0	0

TVV: TVVOUT output control
TVR: TVRCOUT output control
TVG: TVGOUT output control
TVB: TVBOUT output control
RCAV: RCAVOUT output control
TVFB: TVFB output control
0: Hi-Z (default)
1: Active.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Video volume	CLAMPB	VCLP1	VCLP0	CLAMP2	CLAMP1	1	0	0
R/W		R/W							
Default		0	0	0	0	0	1	0	0

CLAMPB, CLAMP2-1: Clamp control.
Refer to Table 8 and Table 9.

VCLP1-0: DC restore source control
00: ENCV pin (default)
01: ENCY pin
10: (Reserved)
11: ENCG pin

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	S/F Blanking	0	0	0	0	SBT1	SBT0	FB1	FB0
R/W		R/W							
Default		0	0	0	0	0	0	0	0

FB1-0: TV Fast Blanking output control (for TVFB pin)
- 00: 0V (default)
- 01: 2V<, 2.5V(typ) at 150Ω load
- 10: (Reserved)
- 11: (Reserved)

SBT1-0: TV Slow Blanking output control (for TVSB pin. minimum load is 10kΩ.)
- 00: < 2V (default)
- 01: 4.73V <, < 7V
- 10: (Reserved)
- 11: 10V <

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Main volume	0	VOL3	VOL2	VOL1	VOL0	1	1	1
R/W		R/W							
Default		0	0	0	1	1	1	1	1

VOL3-0: Volume control

Those registers control both Lch and Rch of Volume.
- 1011: Volume gain = +24dB
- 1010: Volume gain = +21dB
- 1001: Volume gain = +18dB
- 1000: Volume gain = +15dB
- 0111: Volume gain = +12dB
- 0110: Volume gain = +9dB
- 0101: Volume gain = +6dB
- 0100: Volume gain = +3dB
- 0011: Volume gain = +0dB (default)
- 0010: Volume gain = -3dB
- 0001: Volume gain = -6dB
- 0000: MUTE

SYSTEM DESIGN

Figure 16 shows the system connection diagram example. An evaluation board (AKD4710) demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

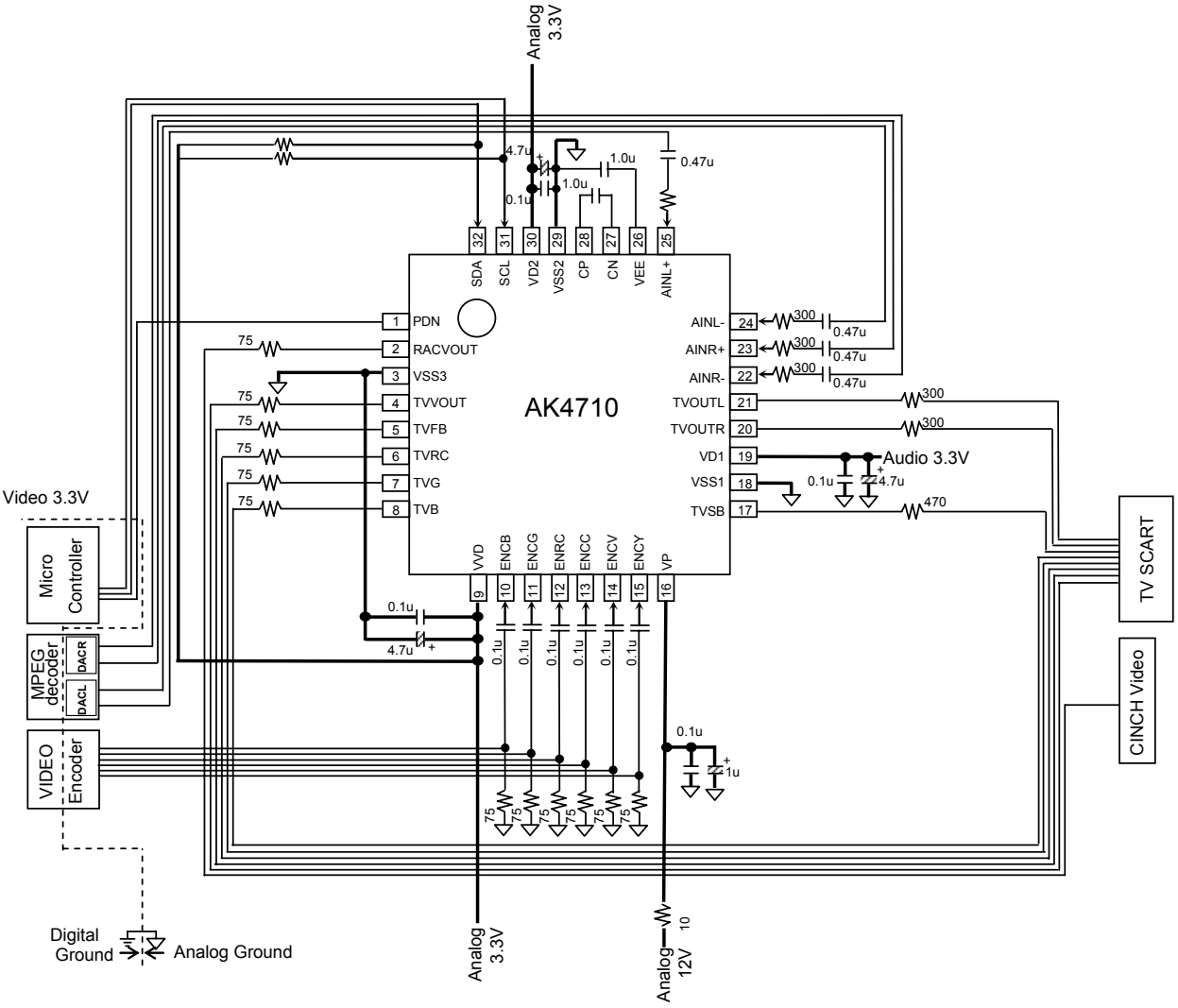


Figure 16. Typical Connection Diagram

■ Grounding and Power Supply Decoupling

VD1, VD2, VP, VVD, VSS1, VSS2 and VSS3 should be supplied from analog supply unit with low impedance and be separated from system digital supply. An electrolytic capacitor 4.7μF parallel with a 0.1μF ceramic capacitor should be attached to VD1, VD2, VVD, VSS1, VSS2 and VSS3 pin to eliminate the effects of high frequency noise. The 0.1μF ceramic capacitor should be placed as near to VD1 (VD2, VVD) as possible.

The VP pin must be connected to the Analogue 12V power supply via a 10ohm resistor and with a 0.1μF ceramic capacitor in parallel with a 1μF electrolytic capacitor to VSS1, as shown in Figure 16.

■ Analog Audio Outputs

The analog outputs are also single-ended and centered on 0V(typ.). The output signal range is typically 2Vrms .

■ Slow Blanking pins

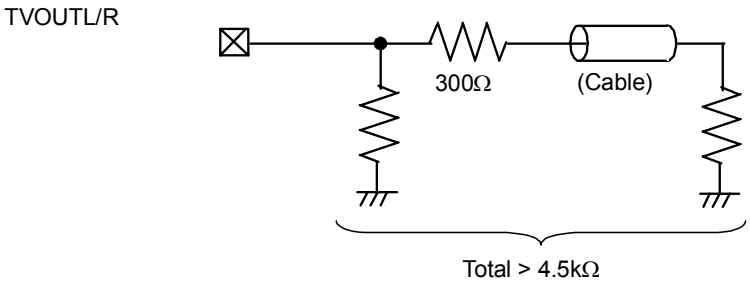
The Slow Blanking Pin must have a 470ohm ±5% series resistor.

■ External Circuit Example

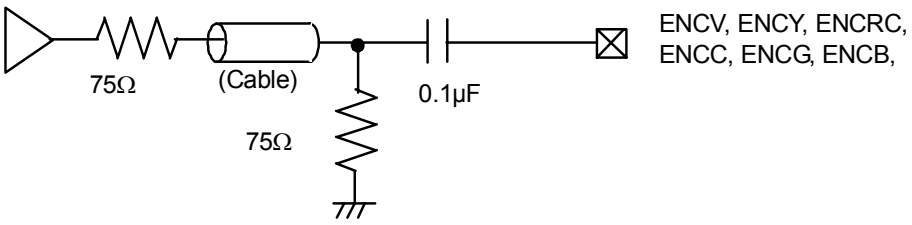
The analog audio input pin must have 300ohm series resistor and 0.47uF capacitor.

Analog Audio Input pin

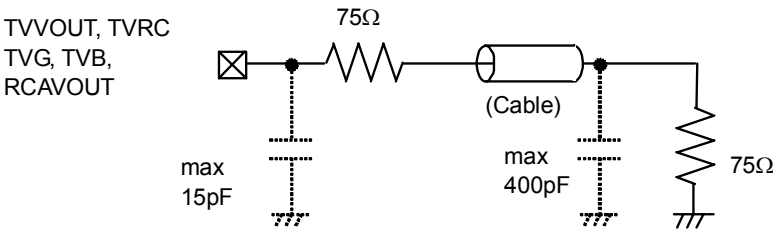
Analog Audio Output pin



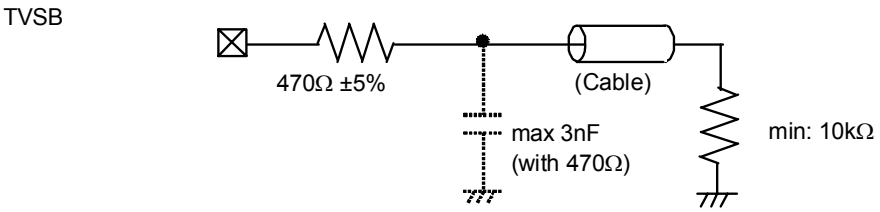
Analog Video Input pin



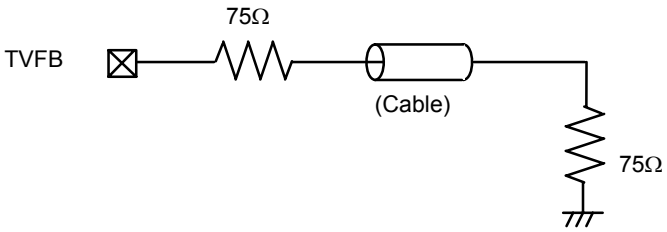
Analog Video Output pin



Slow Blanking pin

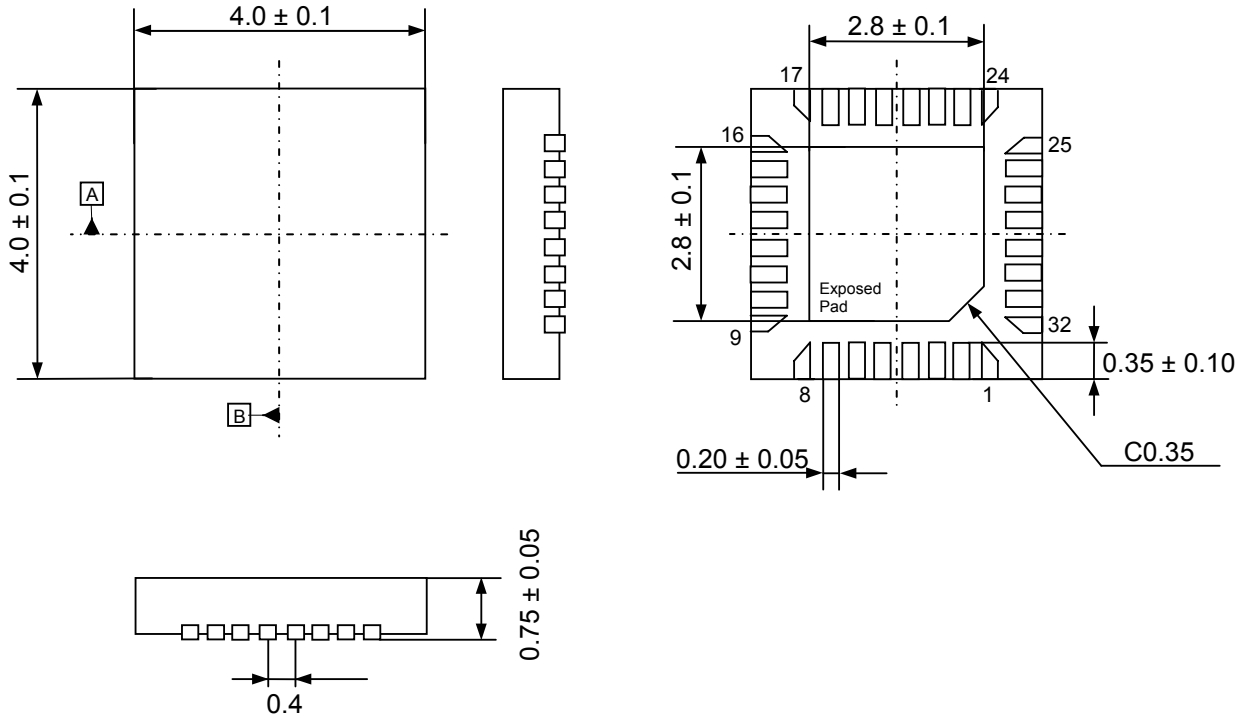


Fast Blanking Output pin



PACKAGE

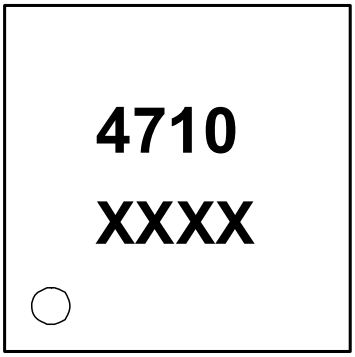
32pin QFN (Unit: mm)



■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



1

XXXX : Date code (4 digit)
Pin #1 indication

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