


**SANYO Semiconductors**
**DATA SHEET**

**LC75412WS**

CMOS IC

**Electronic Volume Controller  
for Car Audio Systems**
**Overview**

The LC75412WS are electronic volume controllers that enable control of volume, balance, fader, bass/treble, loudness, input switching, and input gain using only a small number of external components.

**Functions**

- Volume : 0dB to -79dB in 1dB steps, and  $-\infty$  (81 positions) Balance function with separate L/R control
- Fader : Rear output or front output can be attenuated across 16 positions (in 1dB steps from 0dB to -2dB, 2dB steps from -2dB to -20dB, 10dB steps from -20dB to -30dB, and -45dB, -60dB,  $-\infty$ )
- Bass/treble : Each band can be controlled in 2dB steps from  $\pm 0$ dB to  $\pm 18$ dB.
- Input gain : 0dB to +18.75dB (1.25dB steps) amplification is possible for the input signal.
- Input switching : Six input signals can be selected for Left and for Right (five are singleended inputs and one is a differential input.)
- Loudness : A tap is output from the -32dB position of a volume control resistor ladder. A loudness function can be implemented by connecting an external RC circuit.

**Specifications**
**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\ max}$	$V_{DD}$	11	V
Maximum input voltage	$V_{IN\ max}$	All input pins	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$

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## Allowable Operating Ranges at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}$	$V_{DD}$	6.0		10	V
Input high-level voltage	$V_{IH}$	CL, DI, CE	4.0		10	V
Input low-level voltage	$V_{IL}$	CL, DI, CE	$V_{SS}$		1.0	V
Input amplitude voltage	$V_{IN}$		$V_{SS}$		$V_{DD}$	Vp-p
Input pulse width	$T_{\phi W}$	CL	1			$\mu\text{s}$
Setup time	$T_{setup}$	CL, DI, CE	1			$\mu\text{s}$
Hold time	$T_{hold}$	CL, DI, CE	1			$\mu\text{s}$
Operating frequency	fopg	CL			500	kHz

## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 9\text{V}$ , $V_{SS} = 0\text{V}$

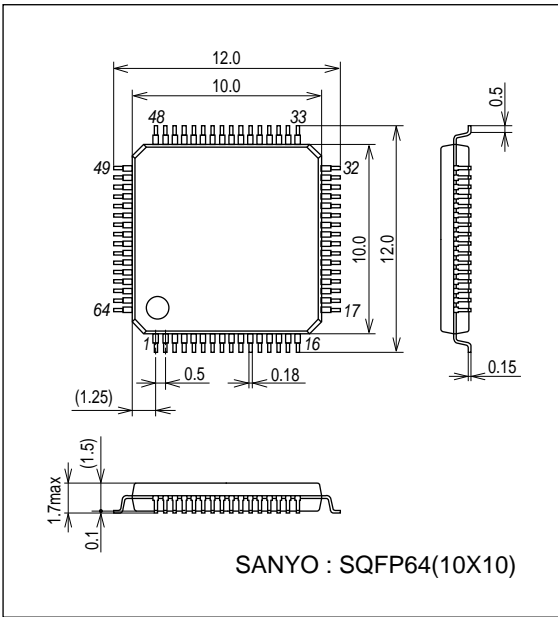
Parameter	Symbol	Pin Name	Conditions	Ratings			Unit
				min	typ	max	
[Input block]							
Input resistance	$R_{in}$	L1 to L4, L6, R1 to R4, R6		30	50	70	$\text{k}\Omega$
Minimum input gain	$G_{inmin}$	L1 to L4, L6, R1 to R4, R6		-1	0	+1	dB
Maximum input gain	$G_{inmax}$			+16.5	+18.75	+21	dB
Step setting error	$A_{Terr}$					$\pm 0.6$	dB
L/R balance	BAL					$\pm 0.5$	dB
[Volume block]							
Input resistance	$R_{vr}$	LVRIN, RVRIN	loudness off	25	50	100	$\text{k}\Omega$
Step setting error	$A_{Terr}$		0dB to -40dB			$\pm 0.5$	dB
L/R balance	BAL		0dB to -40dB			$\pm 0.5$	dB
[Tone block]							
Step setting error	$A_{Terr}$		-8dB to +8dB			$\pm 1.0$	dB
Bass control range	$G_{bass}$		max. boost/cut	$\pm 15$	$\pm 18$	$\pm 21$	dB
Treble control range	$G_{tre}$		max. boost/cut	$\pm 15$	$\pm 18$	$\pm 21$	dB
L/R balance	BAL					$\pm 0.5$	dB
[Fader block]							
Input resistance	$R_{fed}$	LFIN, RFIN		25	50	100	$\text{k}\Omega$
Step setting error	$A_{Terr}$		0dB to -2dB			$\pm 0.5$	dB
			-2dB to -20dB			$\pm 1$	dB
			-20dB to -30dB			$\pm 2$	dB
			-30dB to -60dB			$\pm 3$	dB
L/R balance	BAL		0dB to -60dB			$\pm 0.5$	dB
[General]							
Total harmonic distortion	THD (1)	$V_{IN} = 0\text{dBV}$ , $f = 1\text{kHz}$			0.004	0.01	%
	THD (2)	$V_{IN} = -10\text{dBV}$ , $f = 10\text{kHz}$			0.006	0.01	%
Input crosstalk	CT	$V_{IN} = 1\text{Vrms}$ , $f = 1\text{kHz}$		80	88		dB
L/R crosstalk	CT	$V_{IN} = 1\text{Vrms}$ , $f = 1\text{kHz}$		80	88		dB
Maximum attenuated output	Vomin (1)	$V_{IN} = 1\text{Vrms}$ , $f = 1\text{kHz}$		80	88		dB
	Vomin (2)	$V_{IN} = 1\text{Vrms}$ , $f = 1\text{kHz}$ INMUTE, fader $\infty$		90	95		dB
Output noise voltage	VN (1)	Flat overall, IHF-A filter			5	10	$\mu\text{V}$
	VN (2)	Flat overall, 20 to 20kHzBPF			7	15	$\mu\text{V}$
Current drain	$I_{DD}$				55	60	mA
Input high-level current	$I_{IH}$	CL, DI, CE, $V_{IN} = 9\text{V}$				10	$\mu\text{A}$
Input low-level current	$I_{IL}$	CL, DI, CE, $V_{IN} = 0\text{V}$		-10			$\mu\text{A}$
Maximum input voltage	VCL	THD = 1%, $R_L = 10\text{k}\Omega$ flat overall, $f_{IN} = 1\text{kHz}$		2.3	2.5		Vrms
Common-mode rejection ratio	CMRR	$V_{IN} = 0\text{dB}$ , $f = 1\text{kHz}$				70	dB

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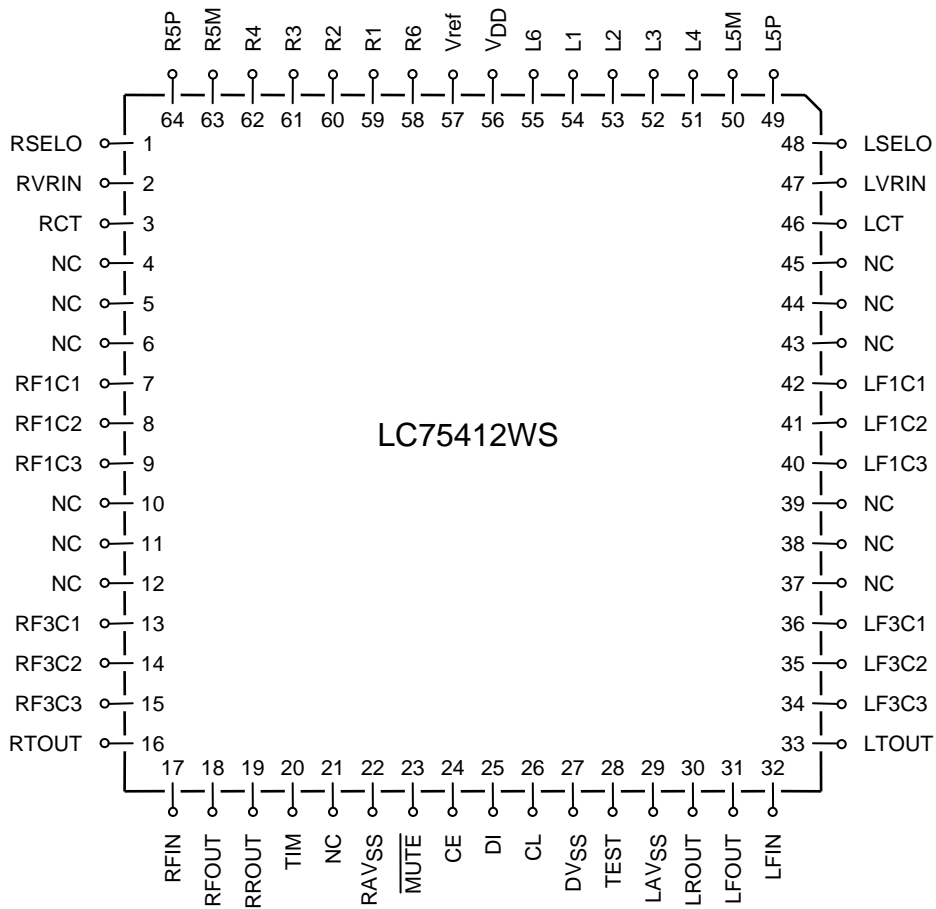
## Package Dimensions

unit : mm (typ)

3190A



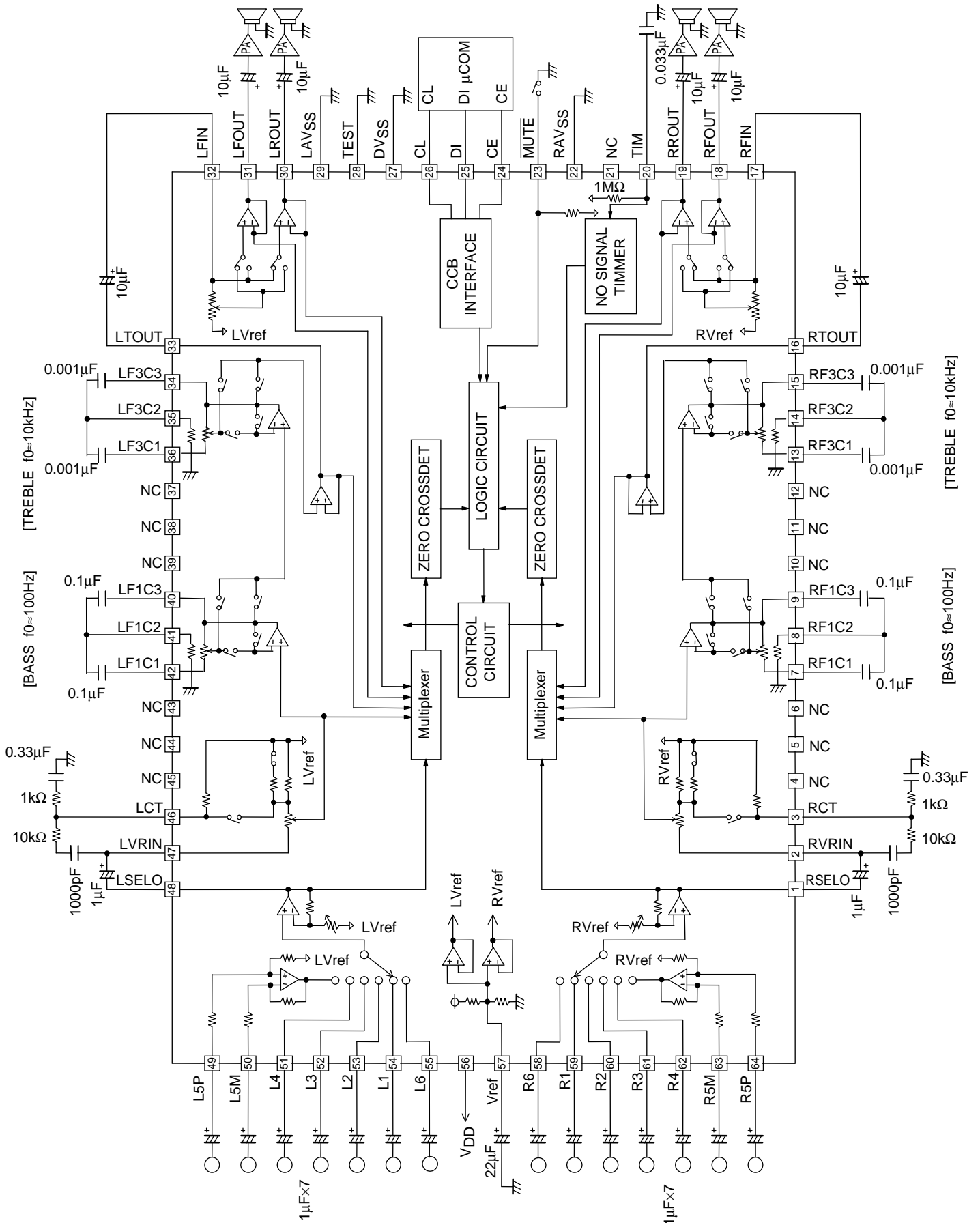
## Pin Assignment



Top view

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## Equivalent Circuit Block Diagram/Sample Application Circuit

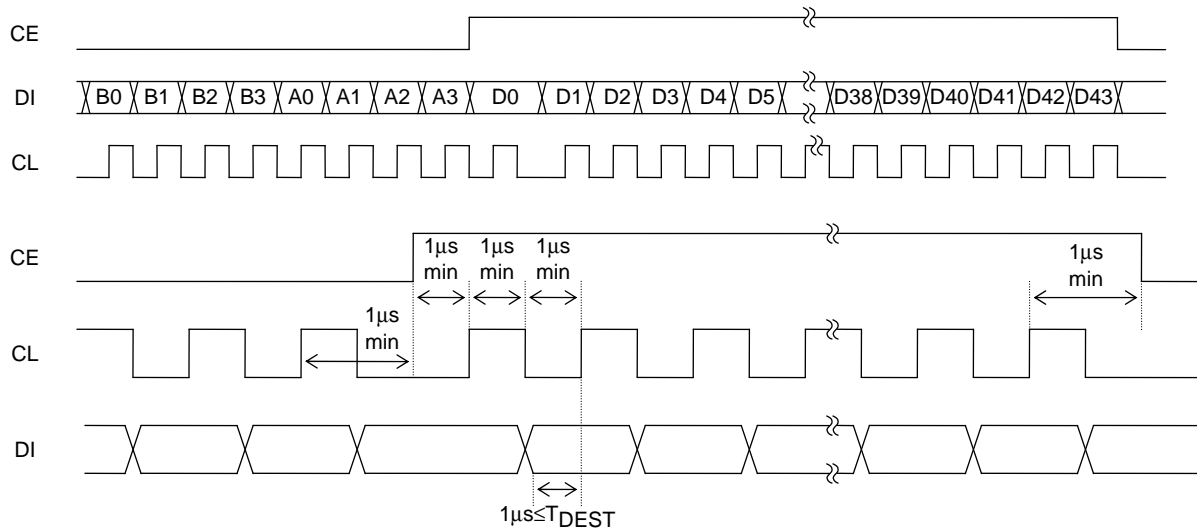


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## Control Timing and Data Format

To control the LC75412WS input specified serial data to the DI, CE, and CL pins.

The data configuration consists of a total of 52 bits broken down into 8 address bits and 44 data bits.



### 1) Address code (B0 to A3)

The LC75412WS use 8-bit address code and can be used in common with ICs that support SANYO's CCB serial bus.

Address Code

(LSB)	B0	B1	B2	B3	A0	A1	A2	A3	(81HEX)
	1	0	0	0	0	0	0	1	

### 2) Control code allocation

#### Input Switching Control

D0	D1	D2	Setting
0	0	0	L1 (R1)
1	0	0	L2 (R2)
0	1	0	L3 (R3)
1	1	0	L4 (R4)
0	0	1	L5 (R5)
1	0	1	L6 (R6)

D3	Bit for IC testing: Normally set to 0
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#### Input Gain Control

D4	D5	D6	D7	Operation
0	0	0	0	0dB
1	0	0	0	+1.25dB
0	1	0	0	+2.50dB
1	1	0	0	+3.75dB
0	0	1	0	+5.00dB
1	0	1	0	+6.25dB
0	1	1	0	+7.50dB
1	1	1	0	+8.75dB
0	0	0	1	+10.00dB
1	0	0	1	+11.25dB
0	1	0	1	+12.50dB
1	1	0	1	+13.75dB
0	0	1	1	+15.00dB
1	0	1	1	+16.25dB
0	1	1	1	+17.50dB
1	1	1	1	+18.75dB

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## Volume Control (0 to -50dB)

D8	D9	D10	D11	D12	D13	D14	D15	Operation
0	0	0	0	0	0	0	0	0dB
1	0	0	0	0	0	0	0	-1dB
0	1	0	0	0	0	0	0	-2dB
1	1	0	0	0	0	0	0	-3dB
0	0	1	0	0	0	0	0	-4dB
1	0	1	0	0	0	0	0	-5dB
0	1	1	0	0	0	0	0	-6dB
1	1	1	0	0	0	0	0	-7dB
0	0	0	1	0	0	0	0	-8dB
1	0	0	1	0	0	0	0	-9dB
0	1	0	1	0	0	0	0	-10dB
1	1	0	1	0	0	0	0	-11dB
0	0	1	1	0	0	0	0	-12dB
1	0	1	1	0	0	0	0	-13dB
0	1	1	1	0	0	0	0	-14dB
1	1	1	1	0	0	0	0	-15dB
0	0	0	0	1	0	0	0	-16dB
1	0	0	0	1	0	0	0	-17dB
0	1	0	0	1	0	0	0	-18dB
1	1	0	0	1	0	0	0	-19dB
0	0	1	0	1	0	0	0	-20dB
1	0	1	0	1	0	0	0	-21dB
0	1	1	0	1	0	0	0	-22dB
1	1	1	0	1	0	0	0	-23dB
0	0	0	1	1	0	0	0	-24dB
1	0	0	1	1	0	0	0	-25dB
0	1	0	1	1	0	0	0	-26dB
1	1	0	1	1	0	0	0	-27dB
0	0	1	1	1	0	0	0	-28dB
1	0	1	1	1	0	0	0	-29dB
0	1	1	1	1	0	0	0	-30dB
1	1	1	1	1	0	0	0	-31dB
0	0	0	0	0	1	0	0	-32dB
1	0	0	0	0	1	0	0	-33dB
0	1	0	0	0	1	0	0	-34dB
1	1	0	0	0	1	0	0	-35dB
0	0	1	0	0	1	0	0	-36dB
1	0	1	0	0	1	0	0	-37dB
0	1	1	0	0	1	0	0	-38dB
1	1	1	0	0	1	0	0	-39dB
0	0	0	1	0	1	0	0	-40dB
1	0	0	1	0	1	0	0	-41dB
0	1	0	1	0	1	0	0	-42dB
1	1	0	1	0	1	0	0	-43dB
0	0	1	1	0	1	0	0	-44dB
1	0	1	1	0	1	0	0	-45dB
0	1	1	1	0	1	0	0	-46dB
1	1	1	1	0	1	0	0	-47dB
0	0	0	0	1	1	0	0	-48dB
1	0	0	0	1	1	0	0	-49dB
0	1	0	0	1	1	0	0	-50dB

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## Volume Control (-51 to $-\infty$ dB)

D8	D9	D10	D11	D12	D13	D14	D15	Operation
1	1	0	0	1	1	0	0	-51dB
0	0	1	0	1	1	0	0	-52dB
1	0	1	0	1	1	0	0	-53dB
0	1	1	0	1	1	0	0	-54dB
1	1	1	0	1	1	0	0	-55dB
0	0	0	1	1	1	0	0	-56dB
1	0	0	1	1	1	0	0	-57dB
0	1	0	1	1	1	0	0	-58dB
1	1	0	1	1	1	0	0	-59dB
0	0	1	1	1	1	0	0	-60dB
1	0	1	1	1	1	0	0	-61dB
0	1	1	1	1	1	0	0	-62dB
1	1	1	1	1	1	0	0	-63dB
0	0	0	0	0	0	1	0	-64dB
1	0	0	0	0	0	1	0	-65dB
0	1	0	0	0	0	1	0	-66dB
1	1	0	0	0	0	1	0	-67dB
0	0	1	0	0	0	1	0	-68dB
1	0	1	0	0	0	1	0	-69dB
0	1	1	0	0	0	1	0	-70dB
1	1	1	0	0	0	1	0	-71dB
0	0	0	1	0	0	1	0	-72dB
1	0	0	1	0	0	1	0	-73dB
0	1	0	1	0	0	1	0	-74dB
1	1	0	1	0	0	1	0	-75dB
0	0	1	1	0	0	1	0	-76dB
1	0	1	1	0	0	1	0	-77dB
0	1	1	1	0	0	1	0	-78dB
1	1	1	1	0	0	1	0	-79dB
*1	1	1	1	1	1	1	0	$-\infty$

\*1: '0' or '1'

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## Tone Control

D16	D17	D18	D19	D40	Bass
D24	D25	D26	D27	D41	Treble
1	1	0	0	1	+18dB
0	1	0	0	1	+16dB
1	0	0	0	1	+14dB
0	1	1	0	0	+12dB
1	0	1	0	0	+10dB
0	0	1	0	0	+8dB
1	1	0	0	0	+6dB
0	1	0	0	0	+4dB
1	0	0	0	0	+2dB
0	0	0	0	0	0dB
1	0	0	1	0	-2dB
0	1	0	1	0	-4dB
1	1	0	1	0	-6dB
0	0	1	1	0	-8dB
1	0	1	1	0	-10dB
0	1	1	1	0	-12dB
1	0	0	1	1	-14dB
0	1	0	1	1	-16dB
1	1	0	1	1	-18dB

D20	D21	D22	D23	Setting
0	0	0	0	Set to 0

## Fader Volume Control

D28	D29	D30	D31	Operation
0	0	0	0	0dB
1	0	0	0	-1dB
0	1	0	0	-2dB
1	1	0	0	-4dB
0	0	1	0	-6dB
1	0	1	0	-8dB
0	1	1	0	-10dB
1	1	1	0	-12dB
0	0	0	1	-14dB
1	0	0	1	-16dB
0	1	0	1	-18dB
1	1	0	1	-20dB
0	0	1	1	-30dB
1	0	1	1	-45dB
0	1	1	1	-60dB
1	1	1	1	-∞



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## Channel Selection Control

D32	D33	Setting
1	0	RCH
0	1	LCH
1	1	L/R simultaneously

## Fader Rear/Front Control

D34	Setting
0	Rear
1	Front

## Loudness Control

D35	Setting
0	OFF
1	ON

## Zero-Cross Control

D36	D37	Setting
0	0	Data write through zero-cross detection
1	1	Zero-cross detection stopped (data write at falling edge of CE)

## Zero-Cross Signal Detection Block Control

D38	D39	Setting
0	0	Selector
1	0	Volume
0	1	Tone
1	1	Fader

## Test Mode Control

D42	D43	Setting
0	0	For IC testing. Always set to 0.

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## Pin Functions

Pin	Pin No.	Function	Equivalent circuit
L1 L2 L3 L4 L6 R1 R2 R3 R4 R6	54 53 52 51 55 59 60 61 62 58	• Single-end input pins.	
L5M L5P R5M R5P	50 49 63 64	• Differential input pins.	
LSELO RSELO	48 1	• Input selector output pins.	
LCT RCT	46 3	• Loudness pins. Connect high-pass compensation CR between LCT (RCT) and LVRIN (RVRIN), and connect low-pass compensation CR between LCT (RCT) and GND.	
LVRIN RVRIN	47 2	• Volume and equalizer input pins.	
LF1C1 LF1C2 LF1C3 RF1C1 RF1C2 RF1C3	42 41 40 7 8 9	• Equalizer F1 band filter configuration capacitor connection pins. Connect capacitor between LF1C1 (RF1C1) and LF1C2 (RF1C2) LF1C2 (RF1C2) and LF1C3 (RF1C3)	
LF3C1 LF3C2 LF3C3 RF3C1 RF3C2 RF3C3	36 35 34 13 14 15	• Equalizer F3 band filter configuration capacitor connection pins. Connect capacitor between LF3C1 (RF3C1) and LF3C2 (RF3C2) LF3C2 (RF3C2) and LF3C3 (RF3C3)	

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Pin	Pin No.	Function	Equivalent circuit
NC NC NC NC NC NC NC NC NC NC NC NC NC	45 44 43 39 38 37 21 12 11 10 6 5 4	<ul style="list-style-type: none"> <li>No connect pin.</li> </ul>	
TEST	28	<ul style="list-style-type: none"> <li>Dedicated IC test pin.</li> <li>Normally this pin is used connected to GND.</li> </ul>	
LTOUIT RTOUT	33 16	<ul style="list-style-type: none"> <li>Equalizer output pins.</li> </ul>	
LFIN RFIN	32 17	<ul style="list-style-type: none"> <li>Fader block input pins.</li> <li>Drive at low impedance.</li> </ul>	
LFOUT LROUT RFOUT RROUT	31 30 18 19	<ul style="list-style-type: none"> <li>Fader output pins. Attenuation is possible separately for the front end and rear end. The attenuation amount is the same for L and R.</li> </ul>	
Vref	57	<ul style="list-style-type: none"> <li>Connect a capacitor of a few tens of <math>\mu\text{F}</math> between Vref and AVSS (<math>V_{SS}</math>) as a <math>V_{DD}/2</math> voltage generator, current ripple countermeasure.</li> </ul>	
$V_{DD}$	56	<ul style="list-style-type: none"> <li>Power supply pin.</li> </ul>	
DVSS	27	<ul style="list-style-type: none"> <li>Logic system ground pin.</li> </ul>	
LAVSS RAVSS	29 22	<ul style="list-style-type: none"> <li>Analog system ground pins.</li> </ul>	
MUTE	23	<ul style="list-style-type: none"> <li>External muting control pin.</li> <li>Setting this pin to <math>V_{SS}</math> level sets forcibly fader volume block to <math>-\infty</math> level.</li> </ul>	

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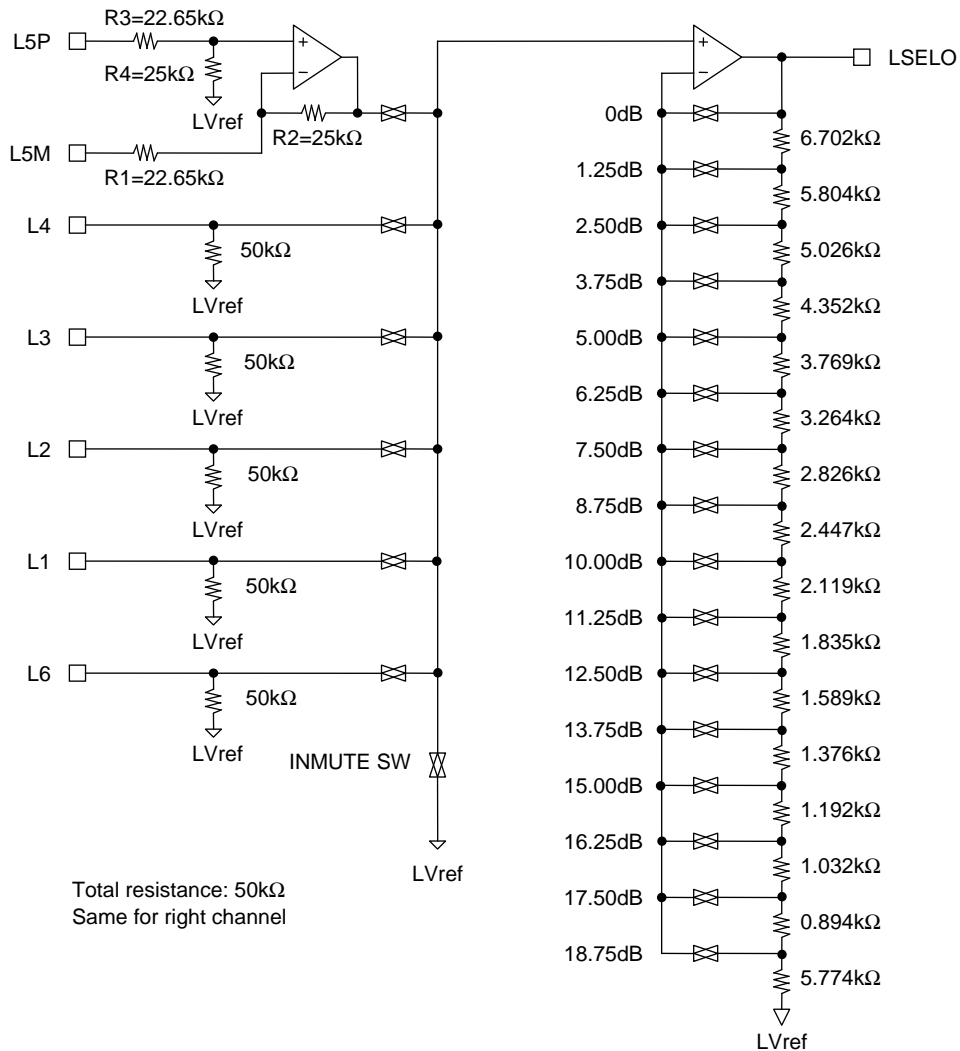
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Pin	Pin No.	Function	Equivalent circuit
TIM	20	<ul style="list-style-type: none"> <li>Timer pin when there is no signal in the zero-cross circuit.</li> <li>Forcibly set data when there is no zero-cross signal, from the time the data is set until the timer ends.</li> </ul>	
CL DI	26 25	<ul style="list-style-type: none"> <li>Input pin for serial data and clock used for control.</li> </ul>	
CE	24	<ul style="list-style-type: none"> <li>Chip enable pin. Data is written to the internal latch and the analog switches are operated when the level changes from High to Low.</li> <li>Data transfer is enabled when the level is High.</li> </ul>	

## Internal Equivalent Circuit Block Diagram

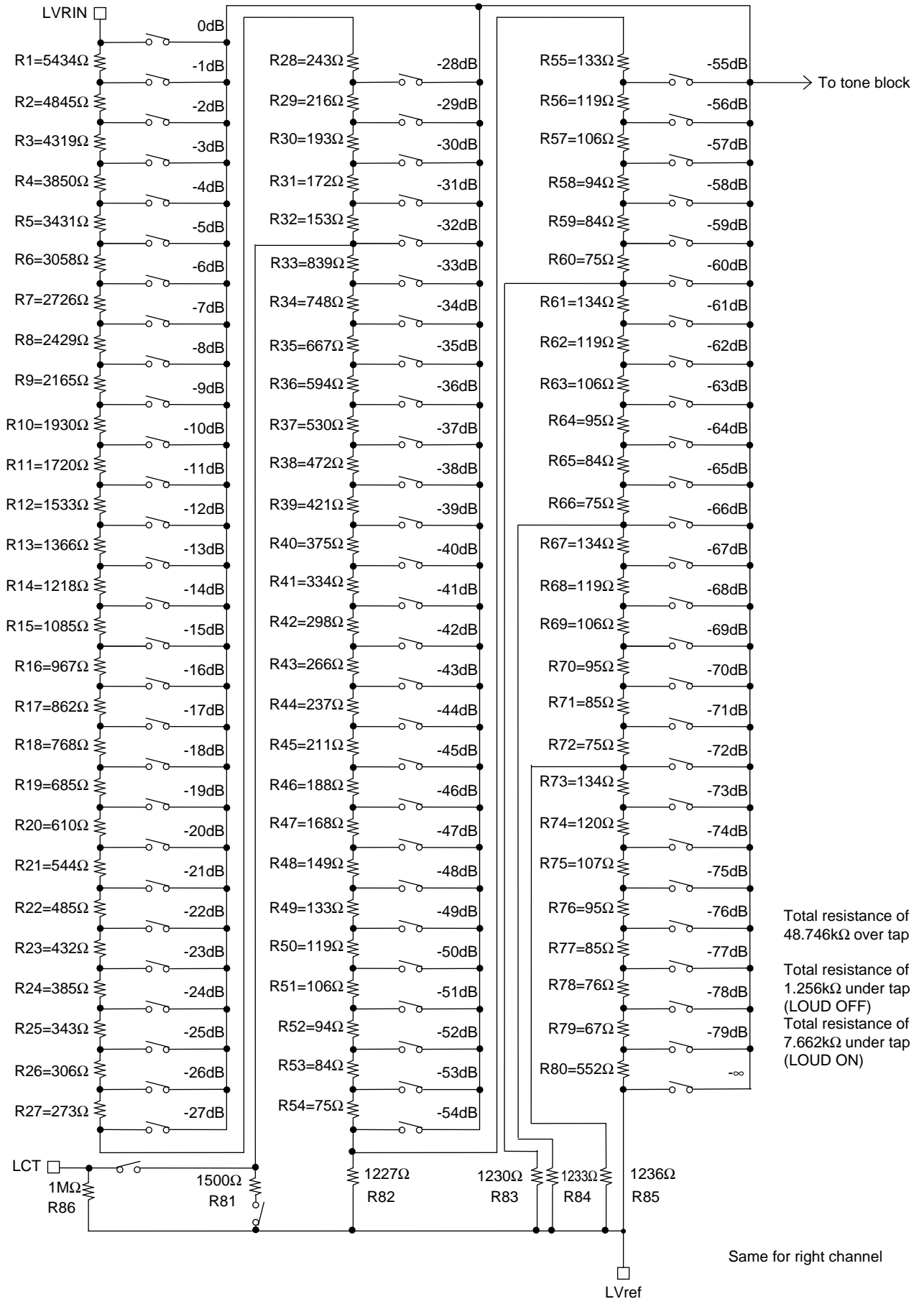
Selector Block Equivalent Circuit Block Diagram



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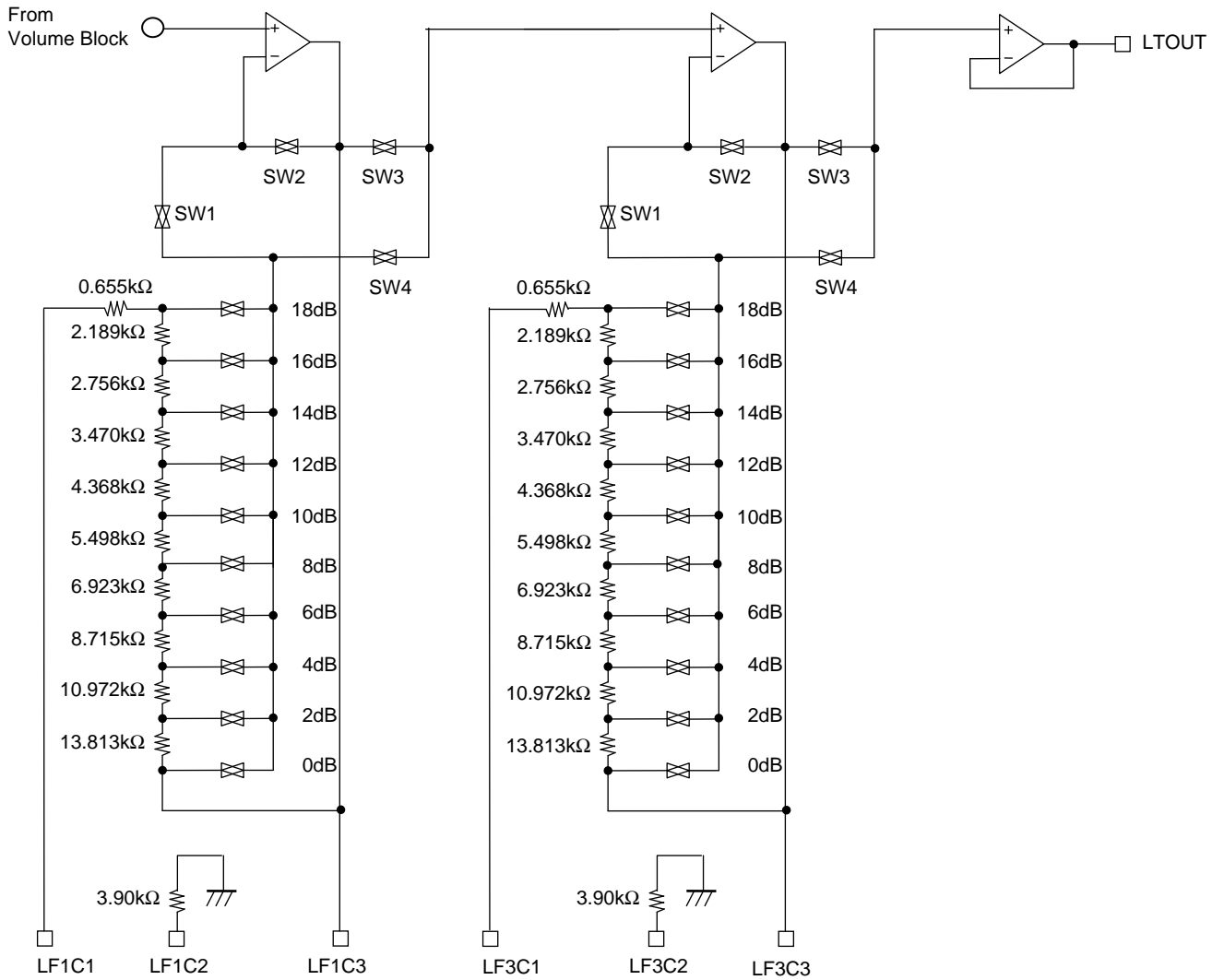
## Volume Block Equivalent Circuit Block Diagram

0dB &  $\infty$  ASW=1k $\Omega$   
Others ASW=3k $\Omega$



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Tone Control Block Equivalent Circuit Diagram



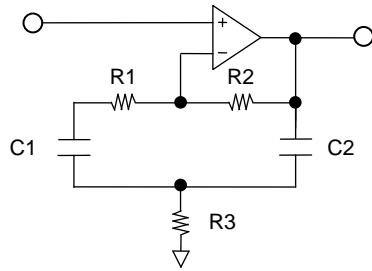
Total resistance: 59.359kΩ  
Same for right channel

During boost, SW1 and SW3 are ON, during cut SW2 and SW4 are ON, and when 0dB, 0dB SW and SW2 and SW3 are ON.

## F1/F3 Band Circuit

The equivalent circuit and the formula for calculating the external CR with a mean frequency of 1kHz are shown below.

- F1/F3 band equivalent circuit block diagram



- Calculation example

Specification Mean frequency :  $f_0 = 1\text{kHz}$

Gain during maximum boost :  $G_{+18\text{dB}} = 18\text{dB}$

Let us use  $R1 = 0.665\text{k}\Omega$ ,  $R2 = 58.704\text{k}\Omega$ , and  $C1 = C2 = C$ .

$$G_{+18\text{dB}} = 20 \times \text{LOG}_{10} \left( 1 + \frac{R2}{2R3 + R1} \right)$$

- 1) Calculate  $R3$  with  $G_{+18\text{dB}} = 18\text{dB}$ :

$$R3 = \left( \frac{R2}{10^{G/20} - 1} - R1 \right) \div 2 = 3900\Omega$$

- 2) Calculate  $C$  with the center frequency  $f_0 = 1\text{kHz}$

$$f_0 = \frac{1}{2\pi \sqrt{(R1 + R2)R3C1C2}}$$

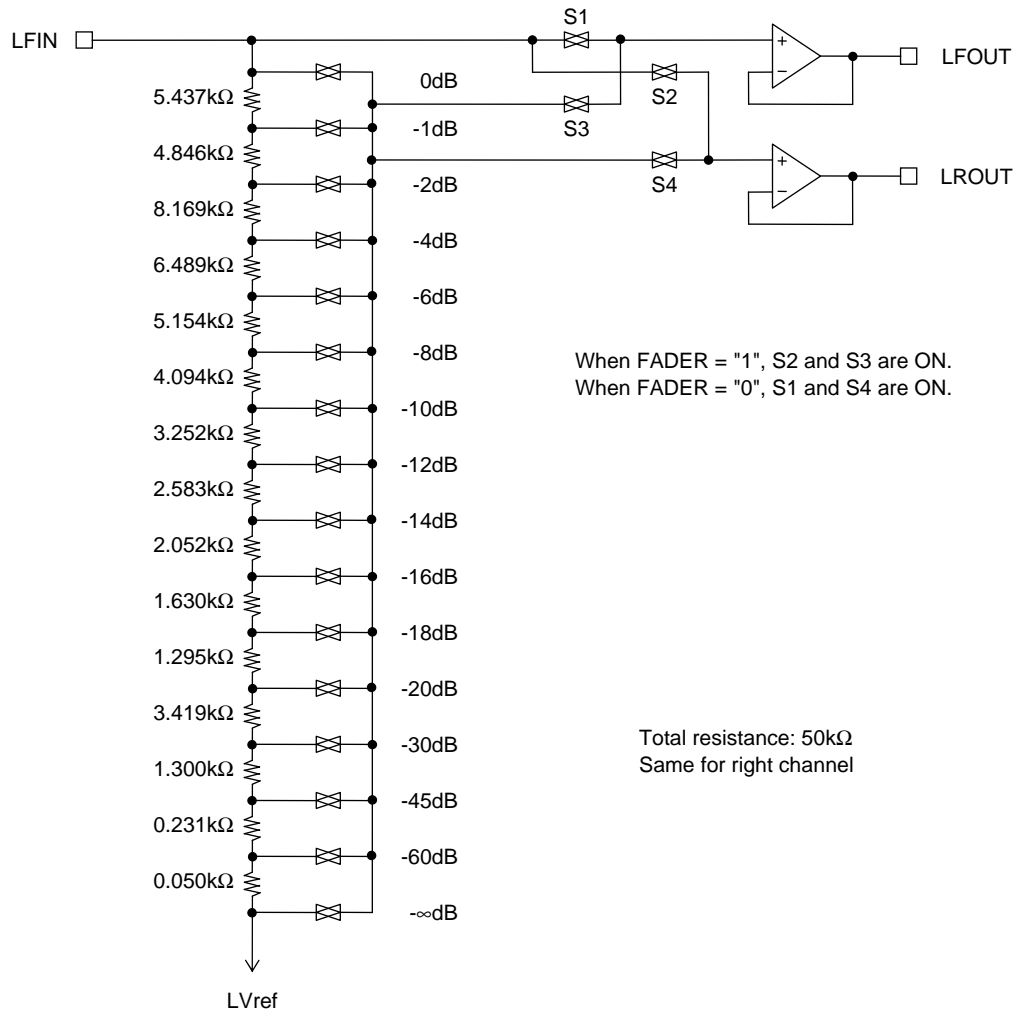
$$C = \frac{1}{2\pi f_0 \sqrt{(R1 + R2)R3}} = \frac{1}{2\pi \times 1000 \sqrt{39359 \times 3900}} = 0.010 \times 10^{-6} \cong 0.01\mu\text{F}$$

- 3) Calculate  $Q$ :

$$Q = \frac{1}{\sqrt{(R1 + R2)R3}} \times \frac{R3(R1 + R2)}{(2R3 + R1)} \cong 1.789$$

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Fader Volume Block Equivalent Circuit Block Diagram



When  $-\infty$  data is sent to the main volume, S1 and S2 become open, and S3 and S4 simultaneously become ON.



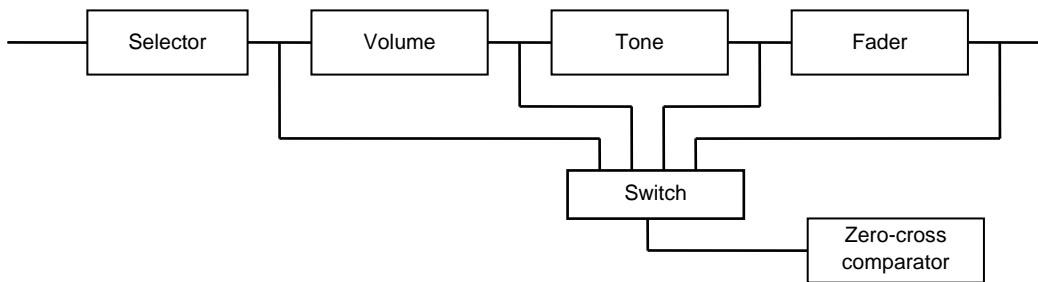
## Usage Cautions

(1) Data transmission at power ON

The status of internal analog switches is unstable at power ON. Therefore, perform muting or some other countermeasure until the data has been set.

(2) Description of zero-cross switching circuit operation

The LC75412WS have a function to switch zero-cross comparator signal detection locations, enabling the selection of the optimum detection location for blocks whose data is to be updated. Basically, the switching noise can be minimized by inputting the signal immediately following the block whose data is to be updated to the zero-cross comparator, so it is necessary to switch the detection location every time.



LC75412WS Zero-Cross Detection Circuit

(3) Zero-cross switching control method

The zero-cross switching control method consists of setting the zero-cross control bits to the zero-cross detection mode (D36, D37 = 0), and specifying the detection blocks (D38, D39) before transmitting the data. These control bits are latched immediately following data transfer, that is to say beforehand in sync with the falling edge of CE, so when updating data of volumes, etc., it is possible to perform mode setting and zero-cross switching with one data transfer. An example of control when updating the data of the volume block is shown below.

D36	D37	D38	D39
0	0	1	0

Zero-cross detection  
mode setting

Volume block  
setting

(4) Zero-cross timer setting

If the input signal becomes lower than the zero-cross comparator detection sensitivity, or if only low-frequency signals are input, zero-cross detection continues to be impossible, and data is not latched during this time.

The zero-cross timer can set a time for forcible latch during such a status when zero-cross detection is not possible.

For example, to set 25ms, using  $T = 0.69CR$  and  $C = 0.033\mu\text{F}$ , we obtain

$$R = \frac{25 \times 10^{-3}}{0.69 \times 0.033 \times 10^{-6}} \approx 1.1 \text{M}\Omega$$

Normally, a value between 10ms and 50ms is set.

# LC75412WS

## (5) Cautions related to serial data transfer

- 1) To ensure that the high-frequency digital signals transferred to the CL, DI, and CE pins do not spill over to the analog signal block, either guard these signal lines with a ground pattern, or perform transmission using shielded wires.
- 2) The data format of the LC75412WS uses 8-bit addresses and 44-bit data. When sending data using multiples of 8 (when sending 48 bits), use the method described in Figure 1.

### Method for Receiving Data Using Multiple of 8 of LC75412WS

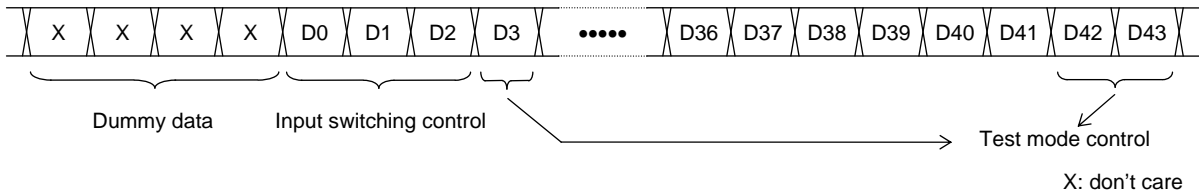


Figure 1

## (6) Note on usage of external muting

See Figure 2, to control muting with an external switch. If a microcontroller is used for the control, it is likely that an overvoltage is applied to the microcontroller via the  $\overline{\text{MUTE}}$  pin because the  $\overline{\text{MUTE}}$  pin is connected internally to  $V_{DD}$ . To avoid such problems, add the resistor R2 as shown in Figure 3 to resistor-divide the voltage at the  $\overline{\text{MUTE}}$  pin.

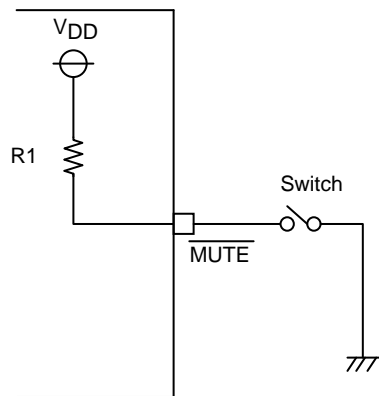


Figure 2

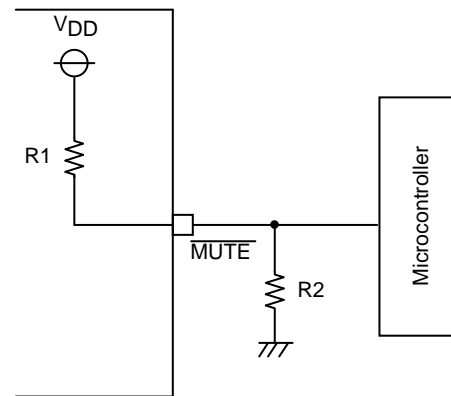
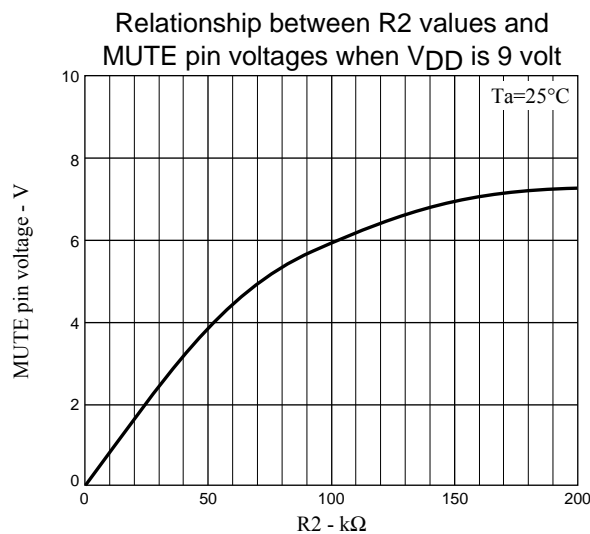


Figure 3

As an example, the relationship between the voltages at the  $\overline{\text{MUTE}}$  pin and the values of R2 when  $V_{DD}$  is 9 volts is shown below. The characteristic curve shown in the figure is a standard one.



\* $V_{IH}$  (High detection voltage) at the  $\overline{\text{MUTE}}$  pin must always be 4V or higher regardless of the supply voltage to be used.

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