

June 2012

## FDP053N08B\_F102

# N-Channel PowerTrench® MOSFET 80V, 120A, $5.3m\Omega$

#### **Features**

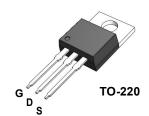
- $R_{DS(on)} = 4.2 \text{m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{V}$ ,  $I_D = 75 \text{A}$
- Low FOM R<sub>DS(on)</sub>\*Q<sub>G</sub>
- · Low reverse recovery charge, Q<sub>rr</sub>
- · Soft reverse recovery body diode
- · Enables highly efficiency in synchronous rectification
- · Fast Switching Speed
- · 100% UIL Tested
- · RoHS Compliant

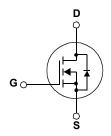
### **Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### **Application**

- · Synchronous Rectification for Server / Telecom PSU
- · Battery Charger and Battery Protection circuit
- · DC motor drives and Uninterruptible Power Supplies
- · Micro Solar Inverter





### MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted\*

Symbol		Parameter		Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage			80	V
V <sub>GSS</sub>	Gate to Source Voltage			±20	V
		- Continuous (T <sub>C</sub> = 25°C,	Silicon Limited)	120*	
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 100°C	, Silicon Limited)	85.2*	Α
		- Continuous (T <sub>C</sub> = 25°C,	Package Limited)	75	
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	480*	Α
E <sub>AS</sub>	Single Pulsed Avalanche E	nergy	(Note 2)	365	mJ
dv/dt	Peak Diode Recovery dv/d	t	(Note 3)	6.0	V/ns
D	Dower Dissination	$(T_C = 25^{\circ}C)$		146	W
$P_{D}$	Power Dissipation	- Derate above 25°C		0.97	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +175	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C	

<sup>\*</sup> Package limitation current is 75A.

### **Thermal Characteristics**

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.03	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	- 6/00

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Description	Quantity
FDP053N08B	FDP053N08B_F102	TO-220	F102: Trimmed Leads	50

### **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Charac	teristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	80	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.089	-	V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64V, V <sub>GS</sub> = 0V	-	-	1	^
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 64V, T_{C} = 125^{\circ}C$	-	-	500	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	±100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu A$	2.5	-	4.5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A	-	4.2	5.3	mΩ
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10V, I_{D} = 75A$	-	100	-	S

### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	101/11/101/11	-	4480	5960	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 40V, V_{GS} = 0V$ 	-	740	985	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1101112	-	20.5	-	pF
C <sub>oss(er)</sub>	Energy Related Output Capacitance	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V	-	1333	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V		-	65.4	85	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = 40V, I_{D} = 75A$	-	26.7	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	V <sub>GS</sub> = 10V	-	14.3	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(Note	4) -	15.3	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	1.2	-	Ω

### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	32	74	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 40V, I_{D} = 75A$	-	30	70	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10V, $R_{GEN}$ = 4.7 $\Omega$	-	44	98	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	16	42	ns

### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode I	Maximum Continuous Drain to Source Diode Forward Current			120*	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	480*	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 75A	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, V <sub>DD</sub> =40V, I <sub>SD</sub> = 75A	-	59.3	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	62.5	-	nC

### Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 3mH,  $I_{AS}$  = 15.6A, Starting  $T_J$  = 25°C
- 3. I\_{SD}  $\leq$  100A, di/dt  $\leq$  200A/µs, V\_{DD}  $\leq$  BV\_DSS, Starting T\_J = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics

### **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

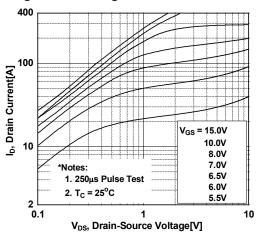


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

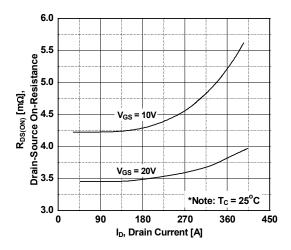


Figure 5. Capacitance Characteristics

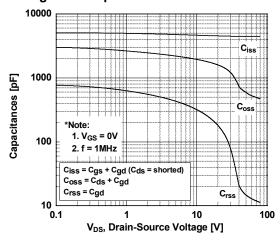


Figure 2. Transfer Characteristics

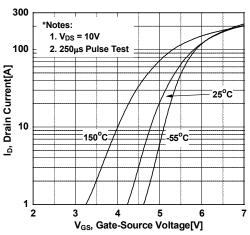


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

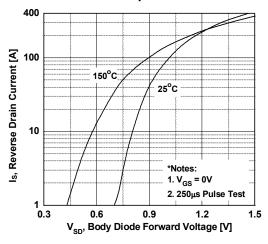
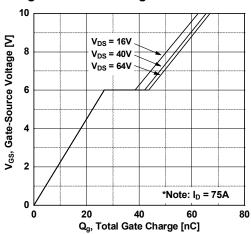


Figure 6. Gate Charge Characteristics



### **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

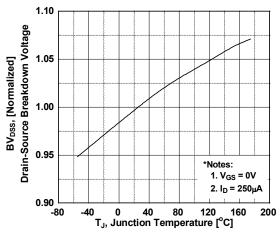


Figure 9. Maximum Safe Operating Area vs. Case Temperature

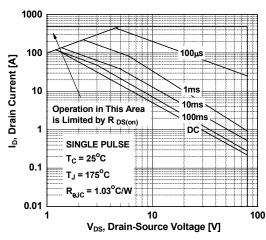


Figure 11. Eoss vs. Drain to Source Voltage

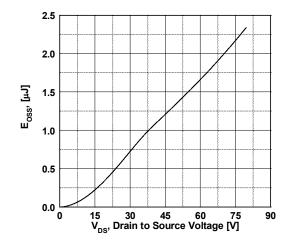


Figure 8. On-Resistance Variation vs. Temperature

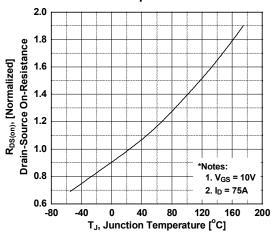


Figure 10. Maximum Drain Current

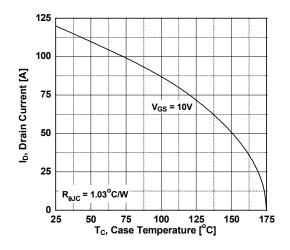
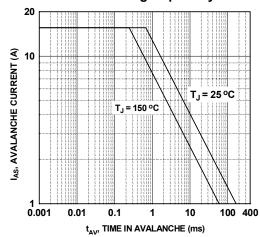
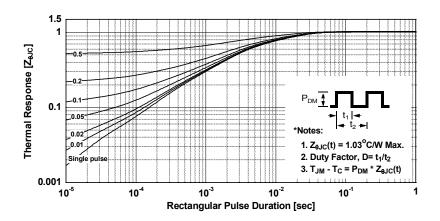


Figure 12. Unclamped Inductive Switching Capability

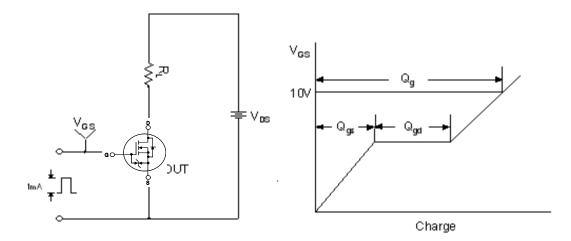


### **Typical Performance Characteristics** (Continued)

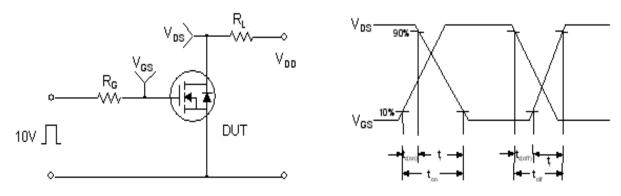




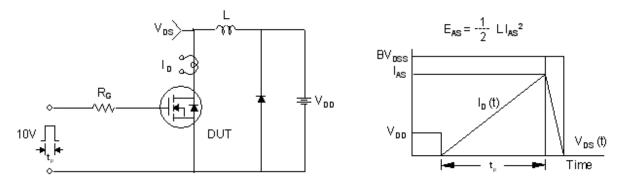
### **Gate Charge Test Circuit & Waveform**



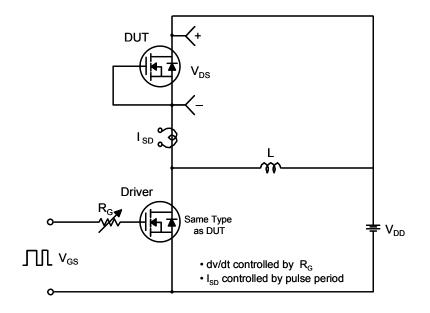
### **Resistive Switching Test Circuit & Waveforms**

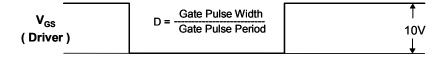


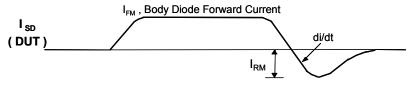
### **Unclamped Inductive Switching Test Circuit & Waveforms**



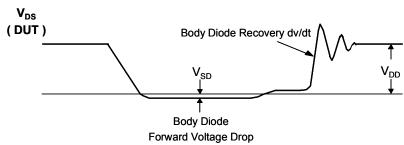
### Peak Diode Recovery dv/dt Test Circuit & Waveforms





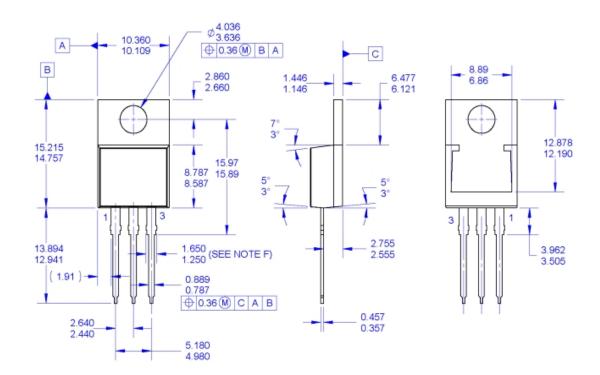


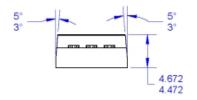
Body Diode Reverse Current



### **Mechanical Dimensions**

TO-220 (F102: Trimmed Leads)





#### NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- Y14.5-1994.

  D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

  E. THIS PACKAGE IS FSZZ INTERNAL PRODUCTION AND INTENDED FOR DELTA CUSTOMER ONLY.

  F. MAX WIDTH FOR F102 DEVICE = 1.35mm.

  G. DRAWING FILE NAME: TO220T03REV2

Dimensions in Millimeters





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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