AERO™ I+ TRANSCEIVER FOR GSM AND GPRS WIRELESS COMMUNICATIONS

Features

- Single 8 x 8 mm package
- CMOS process technology
- Integrated GSM/GPRS transceiver including:
  - Low-IF receiver
  - Universal baseband interface
  - Offset-PLL transmitter
  - Dual RF synthesizer
  - Digitally-controlled crystal oscillator (DCXO)
- Integrated VCOs, frequency synthesizers, and tuning inductors
- Quad-band support:
  - GSM 850 Class 4, small MS
  - E-GSM 900 Class 4, small MS
  - DCS 1800 Class 1
  - PCS 1900 Class 1
- GPRS Class 12 compliant
- 3-wire serial interface
- 2.7 V to 3.0 V operation

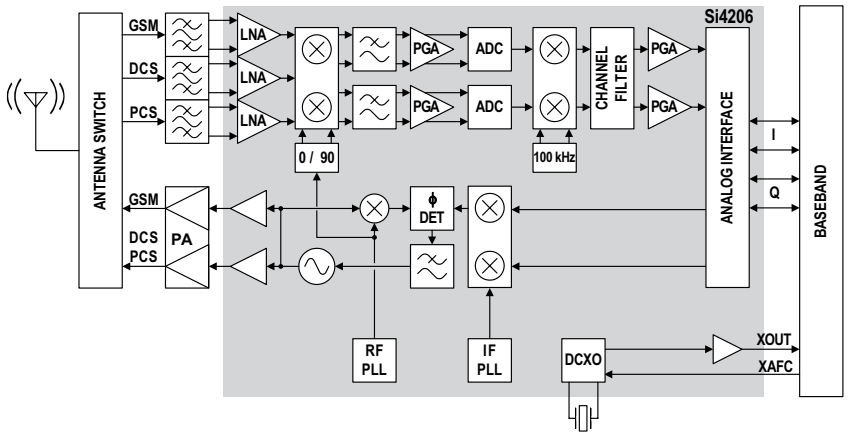
Applications

- Multi-band GSM/GPRS digital cellular handsets
- Multi-band GSM/GPRS wireless data modems

Description

The Aero I+ transceiver is a complete RF front end for multi-band GSM and GPRS wireless communications. The transmit section interfaces between the baseband processor and the power amplifier. The receive section interfaces between the RF band-select SAW filters and the baseband processor. All sensitive components, such as RF/IF VCOs, loop filters, and tuning inductors, are completely integrated into a single compact package. The Aero I+ includes a digitally-controlled crystal oscillator (DCXO) function and completely integrates the reference oscillator and varactor.

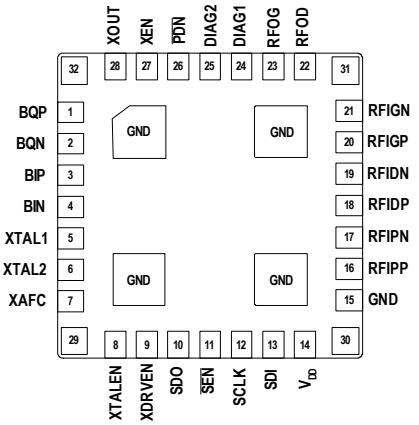
Functional Block Diagram



Pin Assignments (Top View)

Si4206-BM

(Pin description, see page 35)



Ordering Information: See page 36.

Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–20	25	85	°C
DC Supply Voltage	V_{DD}		2.7	2.85	3.0	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at 2.85 V and an operating temperature of 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.3	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		10	dBm

Notes:

1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. **The Si4206 device is a high-performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.**
3. For signals SCLK, SDI, $\overline{SEN}$, $\overline{PDN}$, XIN, XEN, XTALEN, and XDRVEN.
4. At SAW filter output for all bands.

Table 3. DC Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current[1]	I_{RX}	Receive mode	—	83	115	mA
	I_{TX}	Transmit mode	—	85	109	mA
	I_{XTAL13}	$\overline{PDN}$ = 0, XEN = 1, f_{XTAL} = 13 MHz	—	4.0	6.0	mA
	I_{XTAL26}	$\overline{PDN}$ = 0, XEN = 1, f_{XTAL} = 26 MHz	—	5.0	7.0	mA
	I_{PDN}	$\overline{PDN}$ = 0, XEN = 0, XBUF = 0, XPD1 = 1	—	5	80	µA
High Level Input Voltage[2]	V_{IH}		0.7 V_{DD}	—	—	V
Low Level Input Voltage[2]	V_{IL}		—	—	0.3 V_{DD}	V
High Level Input Current[2]	I_{IH}	V_{IH} = V_{DD} = 3.0 V	–10	—	10	µA
Low Level Input Current[2]	I_{IL}	V_{IL} = 0 V, V_{DD} = 3.0 V	–10	—	10	µA
High Level Output Voltage[3]	V_{OH}	I_{OH} = –500 µA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[3]	V_{OL}	I_{OL} = 500 µA	—	—	0.4	V
High Level Output Voltage[4]	V_{OH}	I_{OH} = –10 mA	V_{DD}–0.4	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OL} = 10 mA	—	—	0.4	V

Notes:
1. Measured with load on XOUT pin of 10 pF and f_{XTAL} = 13 MHz. Limits with XEN = 1 guaranteed by characterization. Measured with XEN, XDRVEN, and XTALEN tied together and controlled simultaneously.
2. For pins SCLK, SDI, $\overline{SEN}$, XEN, $\overline{PDN}$, XDRVEN, and XTALEN.
3. For pins SDO, XOUT.
4. For pins DIAG1, DIAG2.

Table 4. AC Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Cycle Time	t_{CLK}	Figures 1, 3	35	—	—	ns
SCLK Rise Time	t_R	Figures 1, 3	—	—	50	ns
SCLK Fall Time	t_F	Figures 1, 3	—	—	50	ns
SCLK High Time	t_{HI}	Figures 1, 3	10	—	—	ns
SCLK Low Time	t_{LO}	Figures 1, 3	10	—	—	ns
$\overline{\text{PDN}}$ Rise Time	t_{PR}	Figure 2	—	—	10	ns
$\overline{\text{PDN}}$ Fall Time	t_{PF}	Figure 2	—	—	10	ns
SDI Setup Time to SCLK↑	t_{SU}	Figure 3	15	—	—	ns
SDI Hold Time from SCLK↑	t_{HOLD}	Figure 3	10	—	—	ns
$\overline{\text{SEN}}$↓ to SCLK↑ Delay Time	t_{EN1}	Figure 3	10	—	—	ns
SCLK↑ to $\overline{\text{SEN}}$↑ Delay Time	t_{EN2}	Figures 3, 4	12	—	—	ns
$\overline{\text{SEN}}$↑ to SCLK↑ Delay Time	t_{EN3}	Figures 3, 4	12	—	—	ns
$\overline{\text{SEN}}$ Pulse Width	t_W	Figures 3, 4	10	—	—	ns
SCLK↓ to SDO Time	t_{CA}	Figure 4	—	—	27	ns
Digital Input Pin Capacitance*			—	—	5	pF

***Note:** For pins SCLK, SDI, $\overline{\text{SEN}}$, XEN, $\overline{\text{PDN}}$, XDRVEN, and XTALEN.

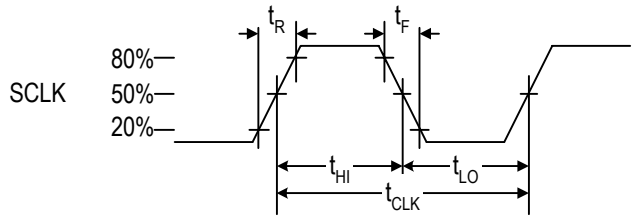


Figure 1. SCLK Timing Diagram

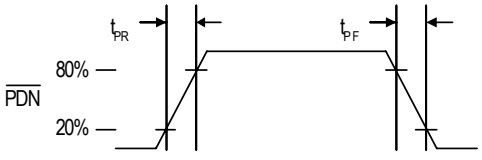


Figure 2. $\overline{\text{PDN}}$ Timing Diagram

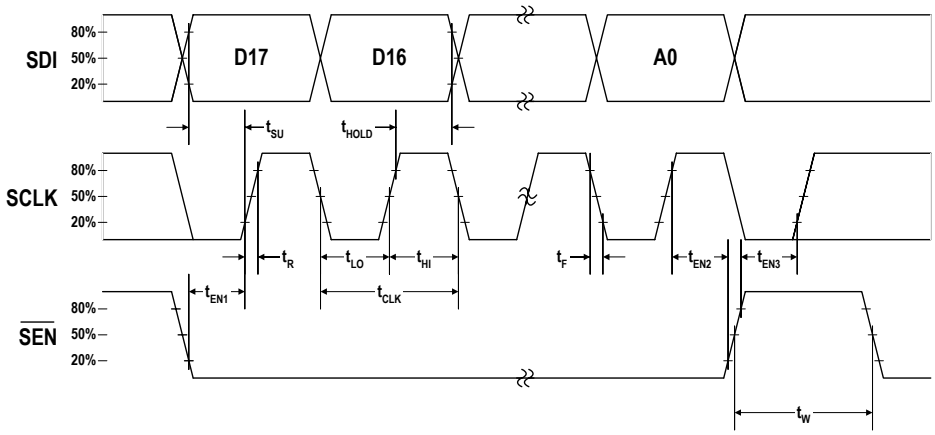


Figure 3. Serial Interface Write Timing Diagram

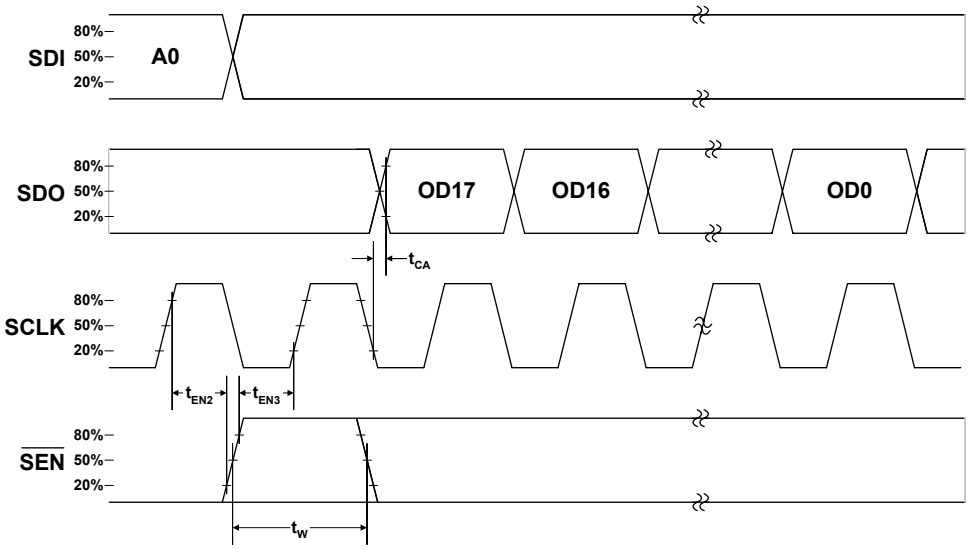


Figure 4. Serial Interface Read Timing Diagram

Table 5. Receiver Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GSM Input Frequency[1]	f_{IN}	GSM 850 band	869	—	894	MHz
		E-GSM 900 band	925	—	960	MHz
DCS or PCS Input Frequency[1]		DCS 1800 band	1805	—	1880	MHz
		PCS 1900 band	1930	—	1990	MHz
Noise Figure at 25 °C[2,3]	NF_{25}	GSM 850 band	—	2.9	3.8	dB
		E-GSM 900 band	—	3.0	3.9	dB
		DCS 1800 band	—	3.3	4.1	dB
		PCS 1900 band	—	3.7	4.5	dB
Noise Figure at 75 °C[2,3]	NF_{75}	GSM 850 band	—	3.6	4.5	dB
		E-GSM 900 band	—	3.7	4.6	dB
		DCS 1800 band	—	4.2	5.0	dB
		PCS 1900 band	—	4.9	5.7	dB
Noise Figure at 85 °C[2,3]	NF_{85}	GSM 850 band	—	3.7	4.6	dB
		E-GSM 900 band	—	3.8	4.7	dB
		DCS 1800 band	—	4.6	5.4	dB
		PCS 1900 band	—	5.2	6.0	dB
3 MHz Input Desensitization[2,3,4]	DES_3	GSM input	–25	–21	—	dBm
		DCS/PCS inputs	–28	–25	—	dBm
20 MHz Input Desensitization[2,3,4]	DES_{20}	GSM input	–20	–16	—	dBm
		DCS/PCS inputs	–19	–15	—	dBm
Input IP2[2]	IP2	$\lvert f_{1,2} - f_0 \rvert \geq 6$ MHz, $\lvert f_2 - f_1 \rvert = 100$ kHz	29	40	—	dBm
Input IP3[2]	IP3	$\lvert f_2 - f_1 \rvert \geq 800$ kHz, $f_0 = 2f_1 - f_2$	–18	–12	—	dBm
Image Rejection[2,4]	IR	GSM Input	28	35	—	dB
		DCS/PCS Inputs	28	40	—	dB
1 dB Input Compression[2,5]	CP_{MAX}	GSM Input	–28	–23	—	dBm
		DCS/PCS inputs	–27	–22	—	dBm
1 dB Input Compression[2,6]	CP_{MIN}	GSM Input	–23	–18	—	dBm
		DCS/PCS inputs	–23	–18	—	dBm
Minimum Voltage Gain[2,6,7]	G_{MIN}	GSM input	3.0	8.5	12.5	dB
		DCS/PCS inputs	10.0	15.5	19.5	dB
Maximum Voltage Gain[2,7]	G_{MAX}	GSM input	100	104	109	dB
		DCS/PCS inputs	96	102	107	dB
LNA Voltage Gain[3,8]	G_{LNA}	GSM input	—	17	—	dB
		DCS/PCS inputs	—	15	—	dB
LNA Gain Control Range	ΔG_{LNA}	GSM input	13	17	21	dB
		DCS/PCS inputs	4	8	12	dB

Table 5. Receiver Characteristics (Continued)
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog PGA Control Range	ΔG_{APGA}		13	16	19	dB
Analog PGA Step Size			3.2	4.0	4.8	dB
Digital PGA Control Range	ΔG_{DPGA}		—	63	—	dB
Digital PGA Step Size			—	1	—	dB
Maximum Differential Output Voltage[9]		DACFS[1:0] = 00	0.7	1.0	1.3	V_{PPD}
		DACFS[1:0] = 01	1.5	2.0	2.5	V_{PPD}
		DACFS[1:0] = 10	2.6	3.5	4.4	V_{PPD}
Output Common Mode Voltage[9]		DACCM[1:0] = 00	0.8	1.0	1.2	V
		DACCM[1:0] = 01	1.05	1.25	1.45	V
		DACCM[1:0] = 10	1.15	1.35	1.55	V
Differential Output Offset Voltage[9,10,11]			—	—	16	mV
Differential Output Offset Voltage Drift[9,10,11]			—	—	5	mV
Baseband Gain Error[9,11]			—	—	1	%
Baseband Phase Error[9,11]			—	—	1	deg
Output Load Resistance[9]	R_L	Single-ended	10	—	—	kΩ
Output Load Capacitance[9]	C_L	Single-ended	—	—	10	pF
Group Delay[12]		CSEL = 0	—	—	22	μs
		CSEL = 1	—	—	16	μs
Differential Group Delay[12]		CSEL = 0	—	—	1.5	μs
		CSEL = 1	—	—	1	μs
Powerup Settling Time[3,13]		From powerdown	—	200	220	μs

Notes:

1. GSM input pins RFIGP and RFIGN. DCS input pins RFIDP and RFIDN. PCS input pins RFIPP and RFIPN.
2. Measurement is performed with a 2:1 balun (50 Ω input, 200 Ω balanced output) and includes matching network and PCB losses. Measured at max gain (AGAIN[2:0] =100_b, LNAG[1:0] = 01_b, LNAC[1:0] = 01_b) unless otherwise noted. Noise figure measurements are referred to 290 °K. Insertion loss of the balun is removed.
3. Specifications guaranteed by characterization using LQW15AN series matching inductors.
4. Input signal at balun is –102 dBm. SNR at baseband output is 9 dB.
5. AGAIN[2:0]=min=000_b, LNAG[1:0] = max=01_b, LNAC[1:0] =max= 01_b.
6. AGAIN[2:0]=min=000_b, LNAG[1:0] = min=00_b, LNAC[1:0] = min=00_b.
7. Voltage gain is defined as the differential rms voltage at the BIP/BIN pins or BQP/BQN pins divided by the rms voltage at the balun input with DACFS[1:0] = 01 and CSEL = 1. Gain is 1.5 dB higher with CSEL = 0. Minimum and maximum values do not include the variation in the DAC full scale voltage (also see Maximum Differential Output Voltage specification).
8. Voltage gain is defined as the differential rms voltage at the LNA output divided by the rms voltage at the balun output.
9. Output pins BIP, BIN, BQP, BQN.
10. Specified as root sum square: $\sqrt{(RXIP - RXIN)^2 + (RXQP - RXQN)^2}$. Drift specification applies to dc offset calibration and is guaranteed by characterization. See ZERODEL[2:0] in the register description.
11. The baseband signal path is entirely digital. Gain, phase, and offset errors at the baseband outputs are because of the D/A converters. Offsets can be measured and calibrated out. See ZERODEL[2:0] in the register description.
12. Group delay is measured from antenna input to baseband outputs. Differential group delay is measured in-band.
13. Includes settling time of the frequency synthesizer. Settling to 5 degrees phase error measured at BIP, BIN, BQP, and BQN pins.

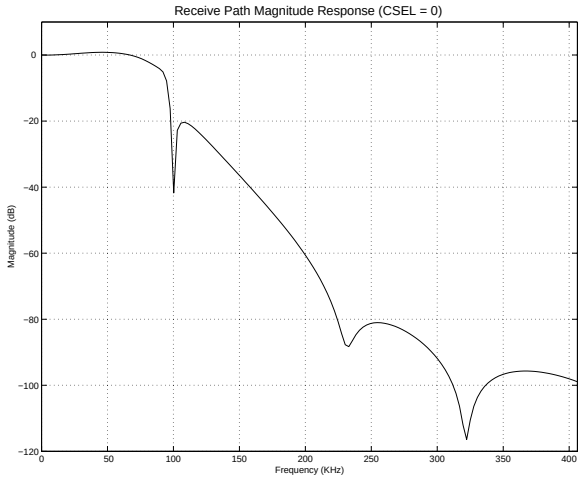


Figure 5. Receive Path Magnitude Response (CSEL = 0)

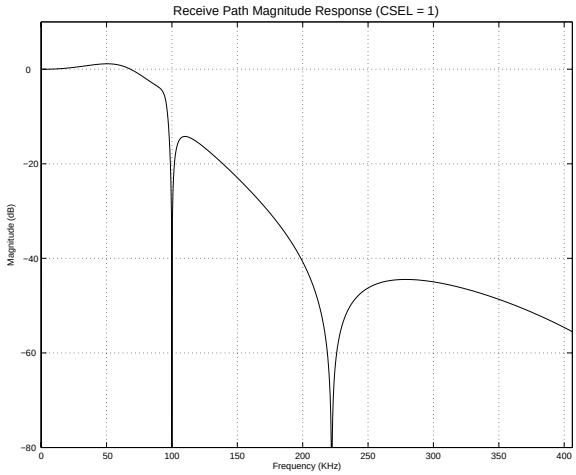


Figure 8. Receive Path Magnitude Response (CSEL = 1)

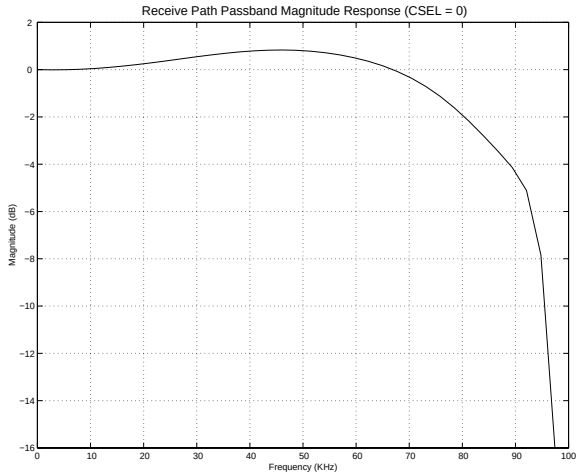


Figure 6. Receive Path Passband Magnitude Response (CSEL = 0)

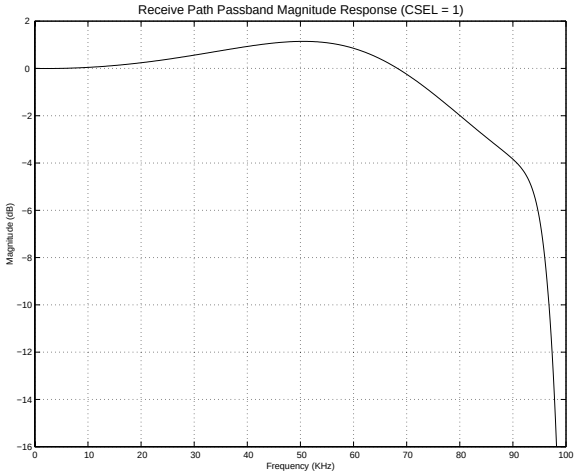


Figure 9. Receive Path Passband Magnitude Response (CSEL = 1)

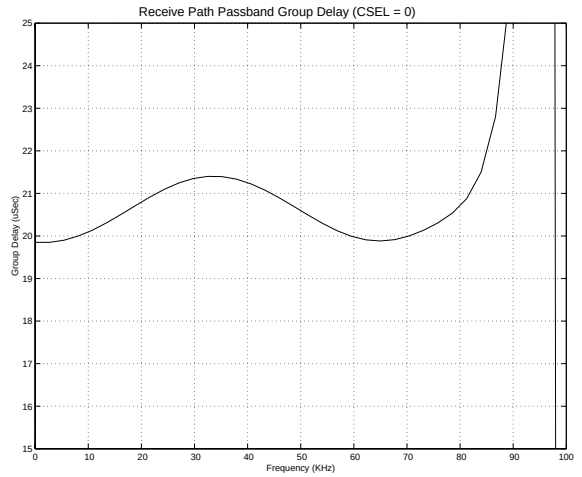


Figure 7. Receive Path Passband Group Delay (CSEL = 0)

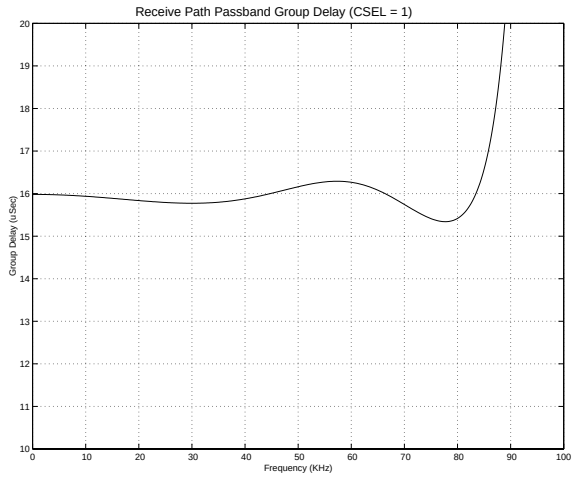


Figure 10. Receive Path Passband Group Delay (CSEL = 1)

Table 6. Transmitter Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RFOG Output Frequency[1]		GSM 850 band	824	—	849	MHz
		E-GSM 900 band	880	—	915	MHz
RFOD Output Frequency[2]		DCS 1800 band	1710	—	1785	MHz
		PCS 1900 band	1850	—	1910	MHz
I/Q Differential Input Swing[3,4]			0.88	—	2.2	V_{PPD}
I/Q Input Common Mode[3]			1.1	—	1.4	V
I/Q Differential Input Resistance[3,4]		BBG[1:0] = 11_b	16	19	22	kΩ
		BBG[1:0] = 00_b	14	17	20	kΩ
		BBG[1:0] = 01_b	12	15	18	kΩ
		Powered down	—	Hi-Z	—	kΩ
I/Q Input Capacitance[3,5]			—	—	5	pF
I/Q Input Bias Current[3]			13	16	19	μA
Sideband Suppression		67.7 kHz sinusoid	—	–46	–34	dBc
Carrier Suppression		67.7 kHz sinusoid	—	–48	–33	dBc
IM3 Suppression		67.7 kHz sinusoid	—	–57	–50	dBc
Phase Error[5]			—	1.9	3.0	$^o_{rms}$
			—	5	10	$^o_{PEAK}$
TXVCO Pushing[1,2]		Open loop	—	100	—	kHz/V
TXVCO Pulling[1,2]		VSWR 2:1, all phases, open loop	—	200	—	kHz_{PP}
RFOG Output Modulation Spectrum[1,6]		400 kHz offset	—	–65	–63	dBc
		1.8 MHz offset	—	–70	–68	dBc
RFOD Output Modulation Spectrum[2,6]		400 kHz offset	—	–65	–63	dBc
		1.8 MHz offset	—	–70	–65	dBc
RFOG Output Phase Noise[1,5,7]		10 MHz offset	—	–160	–155	dBc/Hz
		20 MHz offset	—	–166	–164	dBc/Hz
RFOD Output Phase Noise[2,5,7]		20 MHz offset	—	–163	–157	dBc/Hz
RFOG Output Power Level[1]		Z_L = 50 Ω	7	9	11	dBm
RFOD Output Power Level[2]		Z_L = 50 Ω	6	8	10	dBm

Table 6. Transmitter Characteristics (Continued)
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Output Harmonic Suppression[1,2]		2nd harmonic	—	—	–20	dBc
		3rd harmonic	—	—	–10	dBc
Powerup Settling Time[5,8]		From powerdown	—	—	150	μs

Notes:
1. Measured at RFOG pin.
2. Measured at RFOD pin.
3. Input pins BIP, BIN, BQP, and BQN.
4. Differential Input Swing is programmable with the BBG[1:0] bits in register 04h. Program these bits to the closest appropriate value. The I/Q Input Resistance scales inversely with the BBG[1:0] setting.
5. Specifications guaranteed by characterization.
6. Measured with pseudo-random pattern. Carrier power and noise power < 1.8 MHz measured with 30 kHz RBW. Noise power ≥ 1.8 MHz measured with 100 kHz RBW.
7. Measured with all 1s pattern.
8. Including settling time of the frequency synthesizer. Settling time measured at the RFOD and RFOG pins to 0.1 ppm frequency error.

Table 7. Frequency Synthesizer Characteristics
(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF1 VCO Frequency[1]	f_{RF1}	GSM 850 band	1737.8	—	1787.8	MHz
		E-GSM 900 band	1849.8	—	1919.8	MHz
		DCS 1800 band	1804.9	—	1879.9	MHz
		PCS 1900 band	1929.9	—	1989.9	MHz
RF2 VCO Frequency[1]	f_{RF2}	GSM 850 band	1272	—	1297	MHz
		E-GSM 900	1279	—	1314	MHz
		DCS 1800 band	1327	—	1402	MHz
		PCS 1900 band	1423	—	1483	MHz
IF VCO Frequency[1]	f_{IF}	GSM 850 band	—	896	—	MHz
		E-GSM 900 band 880–895 MHz 900–915 MHz	—	798	—	MHz
		E-GSM 900 band 895–900 MHz	—	790	—	MHz
		DCS 1800 band	—	766	—	MHz
		PCS 1900 band	—	854	—	MHz
RF1 PLL Phase Detector Update Frequency	f_ϕ	GSM input, RFUP = 0	—	200	—	kHz
		DCS/PCS inputs, RFUP = 1	—	100	—	kHz
IF and RF2 PLL Phase Detector Update Frequency	f_ϕ		—	200	—	kHz
RF1 VCO Pushing[2]		Open Loop	—	500	—	kHz/V
RF2 VCO Pushing[2]			—	400	—	kHz/V
IF VCO Pushing[2]			—	300	—	kHz/V
RF1 VCO Pulling[2]		VSWR = 2:1, all phases, open loop	—	400	—	kHz_{PP}
RF2 VCO Pulling[2]			—	100	—	kHz_{PP}
IF VCO Pulling[2]			—	100	—	kHz_{PP}
RF1 PLL Phase Noise[2]		3 MHz offset	—	–144	–138	dBc/Hz
RF2 PLL Phase Noise[2]		400 kHz offset	—	–126	–121	dBc/Hz
IF PLL Phase Noise[2]		400 kHz offset	—	–128	–123	dBc/Hz
RF1 PLL Spurious[2]		3 MHz offset	—	–95	–83	dBc
RF2 PLL Spurious[2]		400 kHz offset	—	–80	–75	dBc
IF PLL Spurious[2]		400 kHz offset	—	–80	–70	dBc

Notes:
1. For the GSM input, the RF1 VCO is divided by two. During transmit, the IF VCO is divided by two.
2. Specifications are guaranteed by characterization.

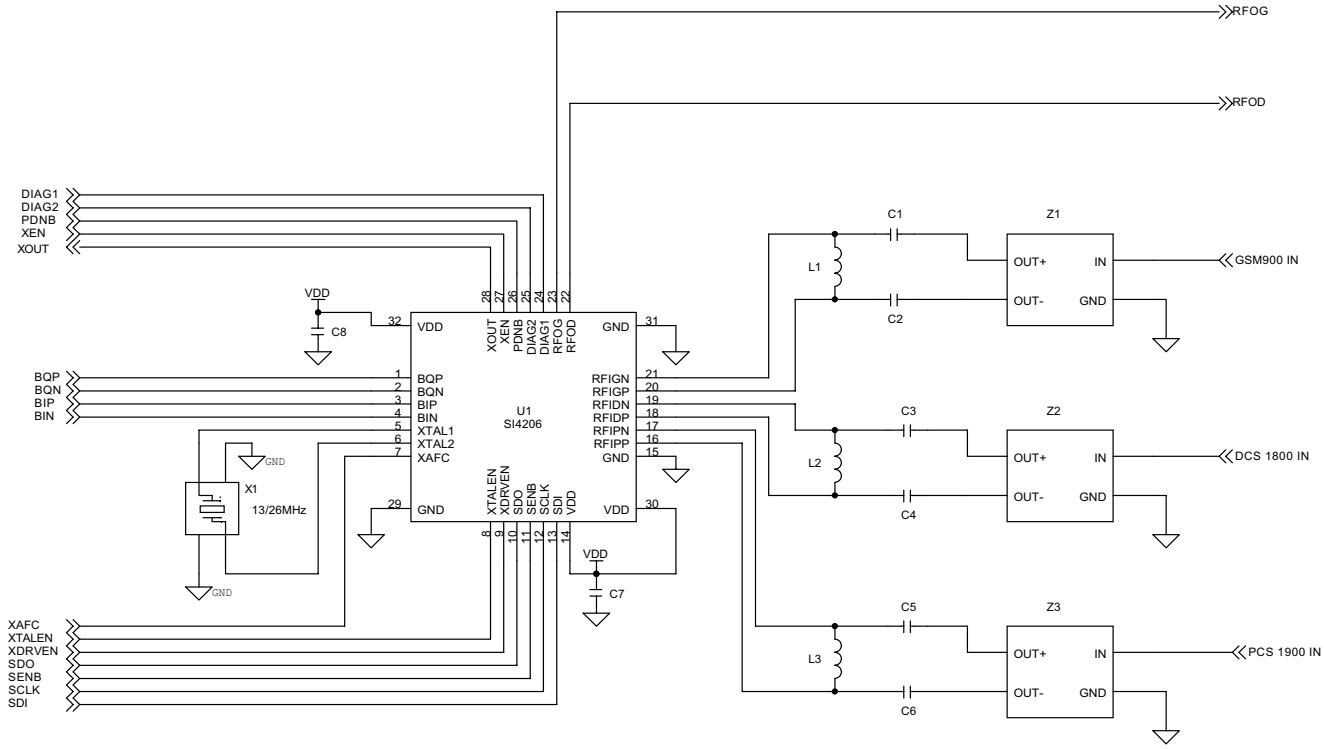
Table 8. Reference Oscillator Characteristics

(V_{DD} = 2.7 to 3.0 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillation Frequency	f_{XTAL}	XSEL = 0, DIV2 = 0	—	13	—	MHz
		XSEL = 1, DIV2 = 1	—	26	—	MHz
AFC Input Voltage	V_{AFC}		0	—	2.5	V
AFC Capacitance Range*	C_{VAR}	f_{XTAL} = 13 MHz	—	1.7	—	pF
		f_{XTAL} = 26 MHz	—	1.4	—	pF
DAC Capacitance Range*	C_{DAC}	f_{XTAL} = 13 MHz	—	3.0	—	pF
		f_{XTAL} = 26 MHz	—	2.9	—	pF
Fixed Capacitance*	C_{FIX}	f_{XTAL} = 13 MHz	—	4.4	—	pF
		f_{XTAL} = 26 MHz	—	4.3	—	pF
Powerup Settling Time	t_{DCXO}	V_{CTL} = 0 to 1.25 V	—	1.0	—	ms

***Note:** Parameters relate to reference oscillator frequency tuning range depending on the crystal characteristics. See “AN83: Selecting a Crystal for Aero™+/I+ Designs” for detailed instructions on crystal selection.

2. Typical Application Schematic



Notes:

1. Connect pads on bottom of U1 to GND.
2. See “AN92: Aero™ I/Aero™ I+ Transceiver PCB Layout Guidelines” for details on the following:
   - LNA matching network (C1–C6, L1–L3). Values should be custom tuned for a specific PCB layout and SAW filter to optimize performance.
   - Differential traces between the SAW filters (Z1–Z3) and transceiver (U1) pins 16–21.
   - Detailed SAW filter requirements.
   - Crystal connection to U1 pins 5–6.
3. XEN, XDRVEN, and XTALEN are recommended to be tied together and controlled simultaneously.

3. Bill of Materials

Component	Value/Description	Supplier(s)
C1–C2	1.2 pF, ±0.1 pF, C0G (GSM 850 and E-GSM 900)	Murata GRM36C0G series Venkel C0402C0G500 series
C3–C4	1.2 pF, ±0.1 pF, C0G (DCS 1800)	Murata GRM36C0G series Venkel C0402C0G500 series
C5–C6	1.5 pF, ±0.1 pF, C0G (PCS 1900)	Murata GRM36C0G series Venkel C0402C0G500 series
C7	22 nF, ±20%, Z5U/X7R	
C8	10 pF, ±5%, C0G	
L1	24 nH, ±2%	Murata LQG15HN series (0402 size) Murata LQW15AN series (0402 size)
L2	6.8 nH, ±0.2 nH	Murata LQG15HN series (0402 size) Murata LQW15AN series (0402 size)
L3	5.6 nH, ±0.2 nH	Murata LQG15HN series (0402 size) Murata LQW15AN series (0402 size)
U1	GSM/GPRS Transceiver	Silicon Laboratories Si4206
X1	13 or 26 MHz crystal	KDS 1BR13000AA0F KSS CX96FFFBQAJ13 NDK W-168-237 Toyocom TN4-25999-r0-2
Z1	GSM 850 RX SAW Filter (150 Ω balanced output)	EPCOS B39881-B9001-C710 (5-pin, 1.4 x 2.0 mm) EPCOS B39881-B9004-E710 (6-pin, 1.6 x 2.0 mm) Murata SAFEK881MFL0T00R00 (6-pin, 1.6 x 2.0 mm)
	E-GSM 900 RX SAW Filter (150 Ω balanced output)	EPCOS B39941-B7820-C710 (5-pin, 1.4 x 2.0 mm) Murata SAFEK942MFM0T00R00 (6-pin, 1.6 x 2.0 mm)
Z2	DCS 1800 RX SAW Filter (150 Ω balanced output)	EPCOS B39182-B7821-C710 (5-pin, 1.4 x 2.0 mm) EPCOS B39182-B9013-K310 (6-pin, 1.6 x 2.0 mm) Murata SAFEK1G84FA0T00R00 (6-pin, 1.6 x 2.0 mm)
Z3	PCS 1900 RX SAW Filter (150 Ω balanced output)	EPCOS B39202-B7825-C710 (5-pin, 1.4 x 2.0 mm) Murata SAFEK1G96FA0T00R00 (6-pin, 1.6 x 2.0 mm)

4. Functional Description

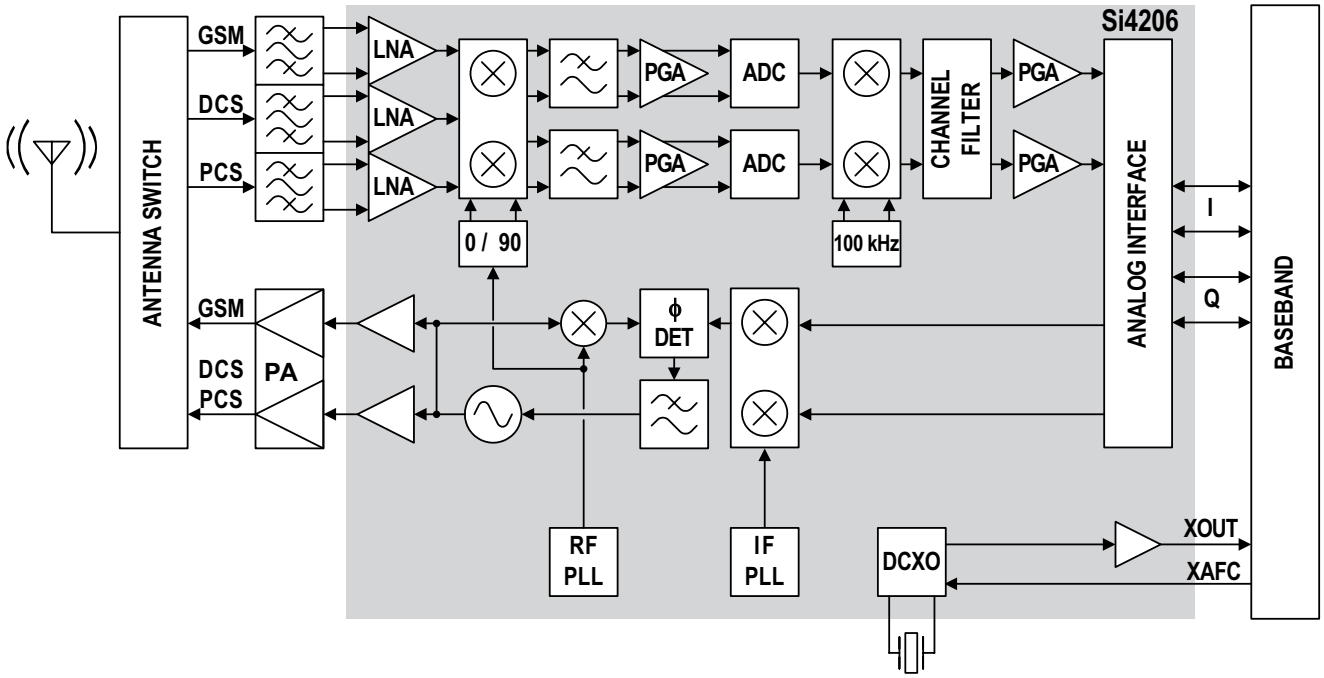


Figure 11. Aero I+ Transceiver Block Diagram

The Aero I+ transceiver is the industry's most integrated RF front end for multi-band GSM/GPRS digital cellular handsets and wireless data modems. The highly integrated solution eliminates the IF SAW filter, external low noise amplifiers (LNAs) for three bands, transmit and RF voltage-controlled oscillator (VCO) modules, and more than 70 other discrete components found in conventional designs.

The high level of integration obtained through high-performance packaging and fine line CMOS process technology results in a solution with 50% less area and 80% fewer components than competing solutions. A triple-band GSM transceiver using the Aero I+ transceiver can be implemented with 15 components in less than 1.2 cm^2 of board area. This level of integration is an enabling force in lowering the cost, simplifying the design and manufacturing, and shrinking the form factor in next-generation GSM/GPRS voice and data terminals.

The receive section uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduced complexity. The baseband interface is compatible with any supplier's baseband subsystem.

The transmit section is a complete up-conversion path from the baseband subsystem to the power amplifier, and uses an offset phase-locked loop (PLL) with a fully integrated transmit VCO. The frequency synthesizer uses Silicon Laboratories' proven technology that includes integrated RF and IF VCOs, varactors, and loop filters.

The unique integer-N PLL architecture produces a transient response superior in speed to fractional-N architectures without suffering the high phase noise or spurious modulation effects often associated with those designs. This fast transient response makes the Aero I+ transceiver well suited to GPRS multi-slot applications where channel switching and settling times are critical.

While conventional solutions use BiCMOS or other bipolar process technologies, the Aero I+ transceiver employs 100% CMOS process. This brings the dramatic cost savings and extensive manufacturing capacity of CMOS to the GSM market.

4.1. Receiver

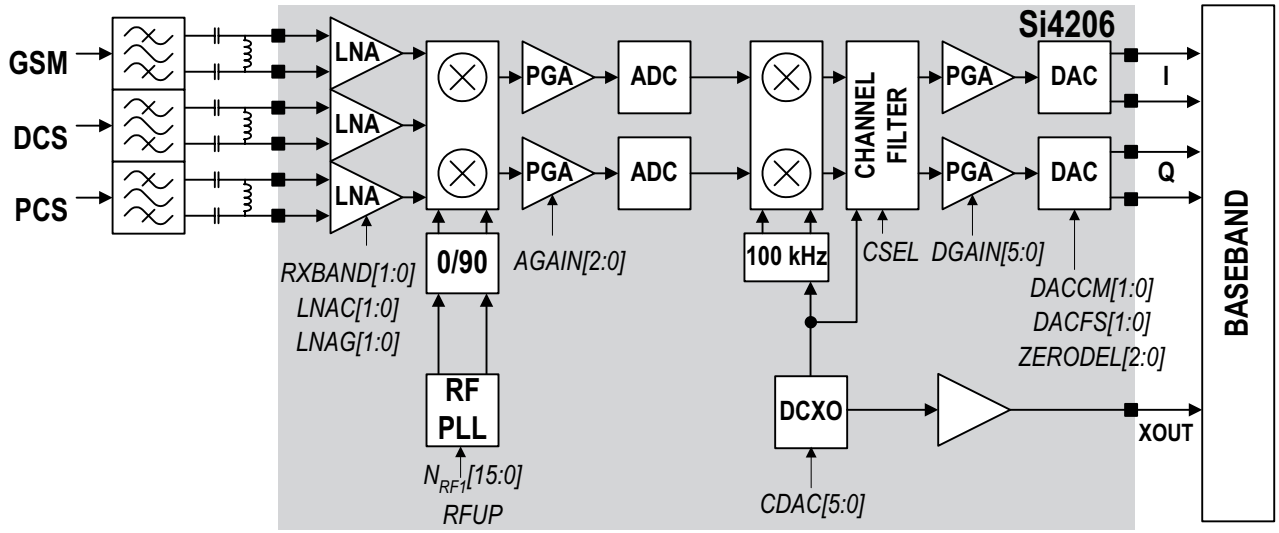


Figure 12. Receiver Block Diagram

The Aero I+ transceiver uses a low-IF receiver architecture that allows for on-chip integration of the channel selection filters, eliminating the external RF image reject filters and the IF SAW filter required in conventional superheterodyne architectures. Compared to a direct-conversion architecture, the low-IF architecture has a much greater degree of immunity to dc offsets that can arise from RF local oscillator (RFLO) self-mixing, 2nd-order distortion of blockers, and device 1/f noise. This relaxes the common mode balance requirements on the input SAW filters and simplifies PC board design and manufacturing.

Three differential-input LNAs are integrated. The GSM input supports the GSM 850 (869–894 MHz) or E-GSM 900 (925–960 MHz) bands. The DCS input supports the DCS 1800 (1805–1880 MHz) band. The PCS input supports the PCS 1900 (1930–1990 MHz) band.

The LNA inputs are matched to the 200 Ω balanced-output SAW filters through external LC matching networks. The LNA gain is controlled with the LNAG[1:0] and LNAC[1:0] bits in Register 05h.

A quadrature image-reject mixer downconverts the RF signal to a 100 kHz intermediate frequency (IF) with the RFLO from the frequency synthesizer. The RFLO frequency is between 1737.8 and 1989.9 MHz, and is divided by two for GSM 850 and E-GSM 900 modes. The mixer output is amplified with an analog programmable gain amplifier (PGA), which is controlled with the AGAIN[2:0] bits in Register 05h. The quadrature IF signal is digitized with high resolution A/D converters (ADCs).

The ADC output is downconverted to baseband with a digital 100 kHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interference signals. The response of the IIR filter is programmable to a high selectivity setting (CSEL = 0) or a low selectivity setting (CSEL = 1). The low selectivity filter has a flatter group delay response that may be desirable where the final channelization filter is in the baseband chip. After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN[5:0] bits in Register 05h.

The LNAG[1:0], LNAC[1:0], AGAIN[2:0] and DGAIN[5:0] bits must be set to provide a constant amplitude signal to the baseband receive inputs. See “AN51: Aero Transceiver AGC Strategy” for more details.

DACs drive a differential analog signal onto the BIP, BIN, BQP, and BQN pins to interface to standard analog-input baseband ICs. No special processing is required in the baseband for offset compensation or extended dynamic range. The receive and transmit baseband I/Q pins are multiplexed together through the BIP, BIN, BQP, and BQN pins. The common mode output level is programmable with the DACCM[1:0] bits, and the full scale level is programmable with the DACFS[1:0] bits in Register 12h.

4.2. Transmitter

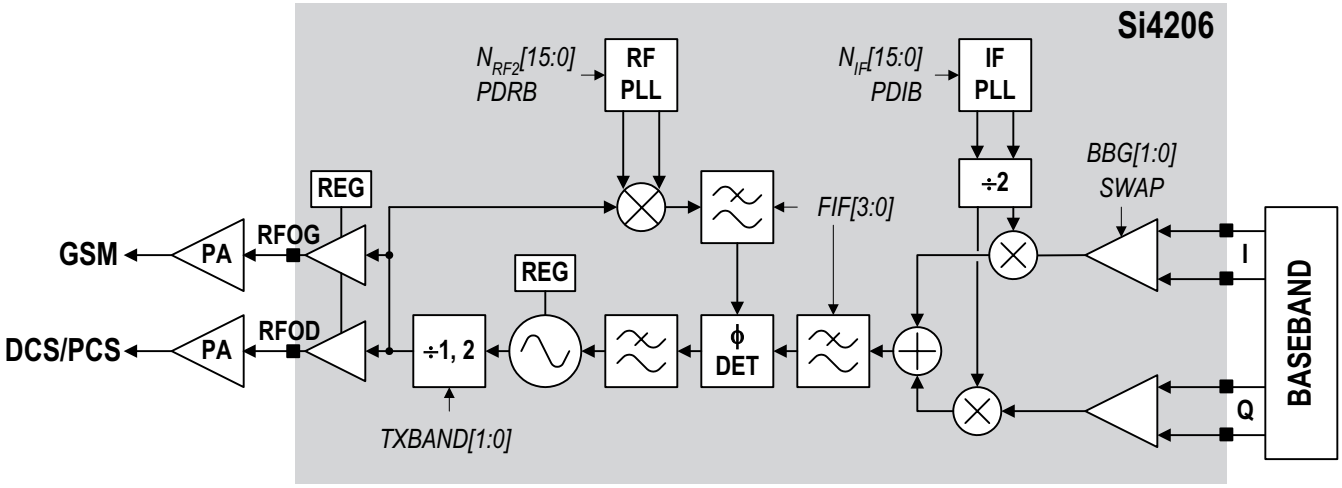


Figure 13. Transmitter Block Diagram

The transmit (TX) section consists of an I/Q baseband upconverter, an offset phase-locked loop (OPLL), and two 50 Ω output buffers that can drive external power amplifiers (PA), one for the GSM 850 (824–849 MHz) and E-GSM 900 (880–915 MHz) bands and one for the DCS 1800 (1710–1785 MHz) and PCS 1900 (1850–1910 MHz) bands. The OPLL requires no external duplexer to attenuate transmitter noise and spurious signals in the receive band, saving both cost and power. Additionally, the output of the transmit VCO (TXVCO) is a constant-envelope signal that reduces the problem of spectral spreading caused by non-linearity in the PA.

A quadrature mixer upconverts the differential in-phase (BIP, BIN) and quadrature (BQP, BQN) signals with the IFLO to generate a SSB IF signal that is filtered and used as the reference input to the OPLL. The IFLO frequency is generated between 766 and 896 MHz. The IFLO is divided by two to generate the quadrature LO signals for the quadrature modulator, resulting in an IF between 383 and 448 MHz. For the E-GSM 900 band, two different IFLO frequencies are required for spur management. Therefore, the IF PLL must be programmed per channel in the E-GSM 900 band. The IFLO frequencies are defined in Table 6 on page 11.

The OPLL consists of a feedback mixer, a phase detector, a loop filter, and a fully integrated TXVCO. The TXVCO is centered between the DCS 1800 and PCS 1900 bands, and its output is divided by two for the GSM 850 and E-GSM 900 bands. The Si4133T generates the RFLO frequency between 1272 and 1483 MHz. To allow a single VCO to be used for the RFLO, high-side injection is used for the GSM 850 and E-GSM 900 bands, and low-side injection is used for the DCS 1800 and PCS 1900 bands. The I and Q signals are automatically swapped when switching bands. Therefore, there is no need for the customer to externally swap the I and O signals. However, for additional layout flexibility, the SWAP bit in register 03h can be used to manually exchange the I and Q signals.

Low-pass filters before the OPLL phase detector reduce the harmonic content of the quadrature modulator and feedback mixer outputs. The cutoff frequency of the filters is programmable with the FIF[3:0] bits in Register 04h and should be set to the recommended settings detailed in the register description.

4.3. Frequency Synthesizer

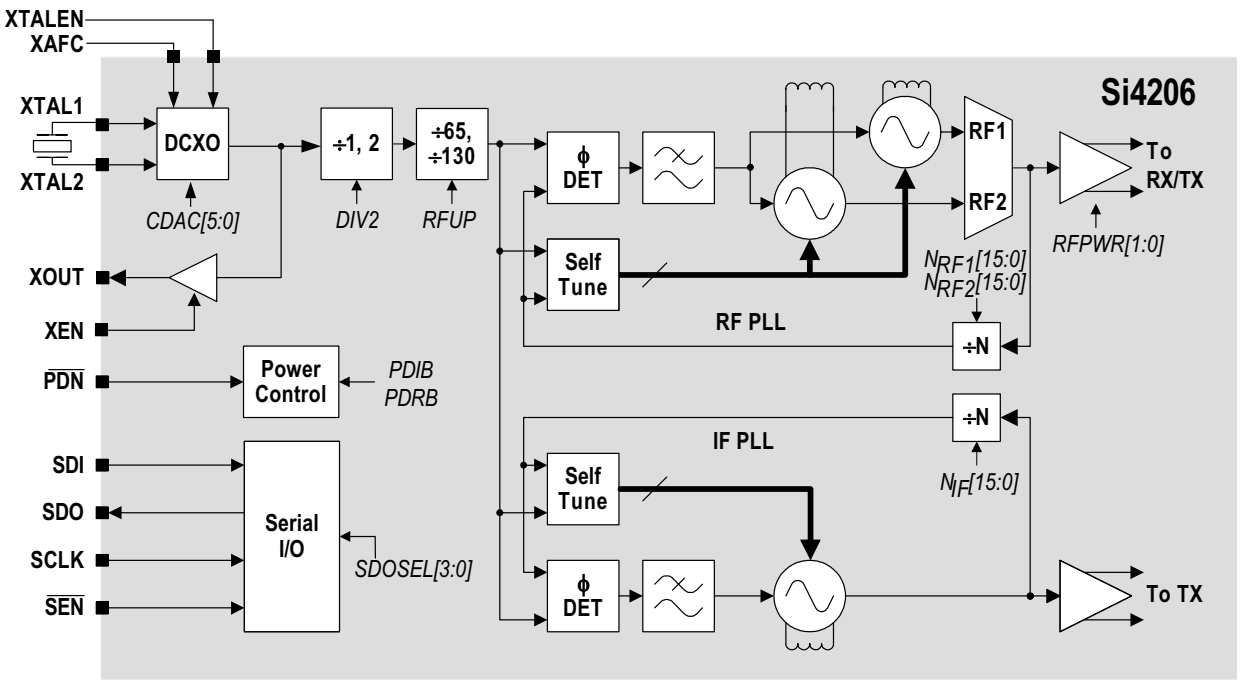


Figure 14. Frequency Synthesizer Block Diagram

The Aero I+ transceiver integrates two complete PLLs including VCOs, varactors, resonators, loop filters, reference and VCO dividers, and phase detectors. The RF PLL uses two multiplexed VCOs. The RF1 VCO is used for receive mode, and the RF2 VCO is used for transmit mode. The IF PLL is used only during transmit mode. All VCO tuning inductors are also integrated.

The IF and RF output frequencies are set by programming the N-Divider registers, N_{RF1}, N_{RF2}, and N_{IF}. Programming the N-Divider register for either RF1 or RF2 automatically selects the proper VCO. The output frequency of each PLL is as follows:

$$f_{OUT} = N \times f_{\phi}$$

A programmable divider in the input stage allows either a 13 or 26 MHz reference frequency depending on the choice of crystal. A 26 MHz reference clock can be divided by 2 using the DIV2 bit in Register 31h. The RF PLL phase detector update rate (f_{ϕ}) can be programmed with the RFUP bit in register 31h to either f_{ϕ} = 100 kHz or f_{ϕ} = 200 kHz. The IF PLL always uses f_{ϕ} = 200 kHz. Receive mode should use f_{ϕ} = 100 kHz in DCS 1800 and PCS 1900 bands, and f_{ϕ} = 200 kHz in the GSM 850 and E-GSM 900 bands. Transmit modes should always use f_{ϕ} = 200 kHz.

4.4. DCXO Overview

The Aero I+ transceiver integrates the DCXO circuitry required to generate a precise system reference clock using only an external crystal resonator. (See Figure 15.) An internal digitally programmable capacitor array (CDAC) provides a coarse method of adjusting the reference frequency in discrete steps. An integrated analog varactor (CVAR) allows for a fine and continuous adjustment of the reference frequency by an external control voltage (XAFC). This control voltage is supplied by the AFC DAC on the baseband IC. The complete DCXO solution effectively replaces TCVCXO modules typically required to provide a 13 or 26 MHz reference clock for the system.

4.4.1. DCXO Tuning

The DCXO uses the CDAC and the CVAR to correct for both static and dynamic frequency errors, respectively. To compensate for crystal offset error, the CDAC ensures a minimum of ±10 ppm frequency adjustment capability. The CDAC is programmed using Register 28h.

The CDAC register (Register 28) may be programmed during powerup or after an initial calibration. Periodic adjustments to compensate for aging may also be performed over time to ensure accuracy.

The baseband determines the appropriate frequency adjustment based on the receipt of the FCCH burst. The baseband then adjusts the XAFC voltage using the baseband AFC DAC (12 or 13-bit).

The baseband AFC DAC can adjust CVAR to correct for frequency variations caused by temperature drift. The step size per bit depends on the resolution of the AFC DAC and its output voltage range.

4.4.2. DCXO Crystal Selection

The tuning range specifications listed in Table 8 on page 14 for CDAC and CVAR assume that Aero I+ is used with a crystal that conforms to the crystal parameters listed in the same table. Other crystals may be used with Aero I+ for cost and/or performance reasons. For example, using a higher sensitivity crystal extends the CVAR and the CDAC frequency compensation range. However, care must be taken when using a more sensitive crystal because other system parameters are affected. Contact Silicon Laboratories' Application Support for assistance in selecting other crystals.

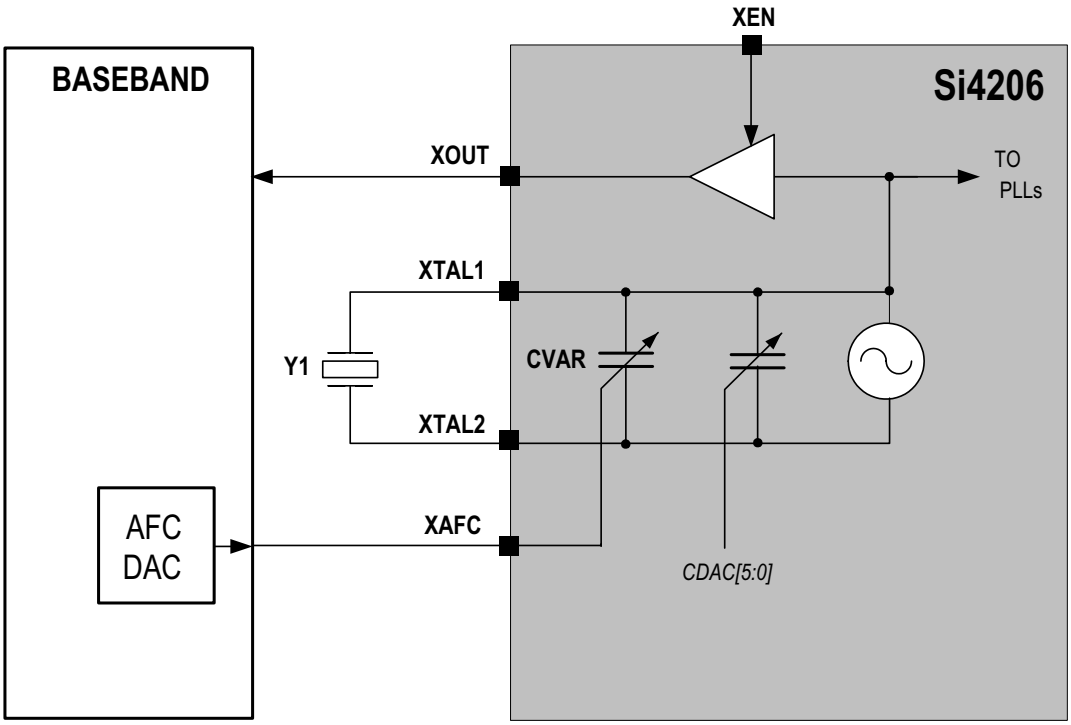


Figure 15. DCXO System Signal Routing Diagram

4.5. Serial Interface

A three-wire serial interface is provided to allow an external system controller to write the control registers for dividers, receive path gain, power down settings, and other controls. The serial control word is 24 bits in length, comprised of an 18-bit data field and a 6-bit address field as shown in Figure 16.

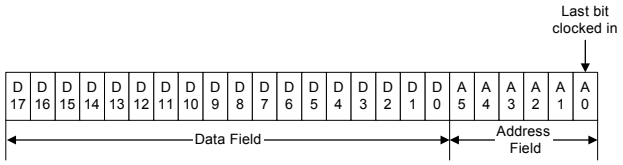


Figure 16. Serial Interface Format

All registers must be written when the $\overline{\text{PDN}}$ pin is asserted (low), except for Register 22h. All serial interface pins should be held at a constant level during receive and transmit bursts to minimize spurious emissions. This includes stopping the SCLK clock. A timing diagram for the serial interface is shown in Figure 3 on page 7.

When the serial interface is enabled (i.e., when $\overline{\text{SEN}}$ is low), data and address bits on the SDI pin are clocked into an internal shift register on the rising edge of SCLK. Data in the shift register is then transferred on the rising edge of $\overline{\text{SEN}}$ into the internal data register addressed in the address field. The internal shift register ignores any leading bits before the 24 required bits. The serial interface is disabled when $\overline{\text{SEN}}$ is high.

Optionally, registers can be read as illustrated in Figure 4 on page 7. The serial output data appears on the SDO pin after writing the revision register with the address to be read. Writing to any of the registers causes the function of SDO to revert to its previously programmed function.

4.6. XOUT Buffer

The Aero I+ transceiver contains a reference clock buffer to drive the baseband input. The XSEL control has no effect on the buffered clock signal. The XOUT buffer is a CMOS driver stage with approximately 250 Ω of series resistance. This buffer is enabled when the XEN pin is set high, independent of the $\overline{\text{PDN}}$ pin.

The XTALEN signal controls the powerup state of the DCXO and must be enabled (XTALEN = 1) before the XOUT signal can be sourced. To achieve complete powerdown during sleep, the XEN pin must be set low, the XBUF bit in Register 12 must be set to zero, and the XPD1 bit in Register 11 must be set to one. During normal operation, these bits should be set to their default values.

5. Control Registers

Table 9. Register Summary

	Reg	Name	Bit																	
			D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	01h	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET
	02h	Mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTO	MODE[1:0]	
	03h	Config	0	0	0	0	DIAG[1:0]		SWAP	0	0	0	TXBAND[1:0]		RXBAND[1:0]		0	0	1	0
	04h	Transmit	0	0	0	0	0	0	0	1	BBG[1:0]		FIF[3:0]				0	0	0	0
	05h	Receive	0	0	0	0	DGAIN[5:0]						0	AGAIN[2:0]			LNAC[1:0]		LNAG[1:0]	
	11h	Config	0	0	0	0	DPDS[2:0]			XPD1	1	XSEL	0	1	0	1	0	0	0	CSEL
	12h	DAC Config	0	0	0	0	0	0	0	1	XBUF	0	ZDBS	ZERODEL[2:0]			DACCM[1:0]		DACFS[1:0]	
	19h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Master Registers	20h	RX Master #1	RXBAND[1:0]		N_{RF1}[15:0]															
	21h	RX Master #2	0	DPDS[2:0]			LNAC[1:0]		LNAG[1:0]		AGAIN[2:0]		0	DGAIN[5:0]						
	22h	RX Master #3	0	0	0	0	0	0	0	0	0	0	0	0	DGAIN[5:0]					
	23h	TX Master #1	TXBAND[1:0]		N_{RF2}[15:0]															
	24h	TX Master #2	FIF[3:0]				N_{IF}[13:0]													
	28h	CDAC	0	0	0	0	0	0	0	0	0	0	0	0	CDAC[5:0]					
	31h	Config	0	0	0	SDOSEL[3:0]				0	0	0	0	0	0	RFUP	DIV2	0	0	0
	32h	Powerdown	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB
	33h	RF1 N Divider	0	0	N_{RF1}[15:0]															
	34h	RF2 N Divider	0	0	N_{RF2}[15:0]															
	35h	IF N Divider	0	0	N_{IF}[15:0]															

Notes:

1. Any register not listed here is reserved and should not be written. Writing to reserved registers may result in unpredictable behavior.
2. Master registers 20h to 24h simplify programming the Aero I+ to support initiation of receive (RX) and transmit (TX) operations with only two register writes.
3. See “AN50: Aero Transceiver Programming Guide” for detailed instructions on register programming.

Register 01h. Reset

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET

Bit	Name	Function
17:1	Reserved	Program to zero.
0	RESET	**Chip Reset.** 0 = Normal operation (default). 1 = Reset all registers to default values. **Note:** This register must be written to 0 twice after a reset operation. This bit does not reset registers 31h to 35h.

Register 02h. Mode Control

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUTO	MODE[1:0]	

Bit	Name	Function
17:3	Reserved	Program to zero.
2	AUTO	**Automatic Mode Select.** 0 = Manual. Mode is controlled by MODE[1:0] bits (default). 1 = Automatic. Last register write to N_{RF1} implies RX mode; Last register write to N_{RF2} implies TX mode. MODE[1:0] bits are ignored.
1:0	MODE[1:0]	**Transmit/Receive/Cal Mode Select.** 00 = Receive mode (default). 01 = Transmit mode. 10 = Calibration mode. 11 = Reserved. **Note:** These bits are valid only when AUTO = 0.

Note: Calibration must be performed each time the power supply is applied. To initiate the calibration mode, set MODE[1:0] = 10 and pulse the $\overline{PDN}$ pin high for at least 150 μs.

Register 03h. Configuration

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	DIAG[1:0]		SWAP	0	0	0	TXBAND[1:0]		RXBAND[1:0]		0	0	1	0

Bit	Name	Function
17:14	Reserved	Program to zero.
13:12	DIAG[1:0]	**DIAG1/DIAG2 Output Select.** DIAG1 DIAG2 00 = LOW LOW (default) 01 = LOW HIGH 10 = HIGH LOW 11 = HIGH HIGH **Note:** These pins can be used to control antenna switch functions. These bits must be programmed with the $\overline{PDN}$ pin is zero. The DIAG1/$\overline{DIAG2}$ pins will be held at the desired value regardless of the state of the $\overline{PDN}$ pin.
11	SWAP	**Transmit I/Q Swap.** 0 = Normal (default). 1 = Swap I and Q for TXIP, TXIN, TXQP, and TXQN pins.
10:8	Reserved	Program to zero.
7:6	TXBAND[1:0]	**Transmit Band Select.** 00 = GSM 850 or E-GSM 900 (default). 01 = DCS 1800. 10 = PCS 1900. 11 = Reserved.
5:4	RXBAND[1:0]	**Receive Band Select.** 00 = GSM input (default). 01 = DCS input. 10 = PCS input. 11 = Reserved.
3:2	Reserved	Program to zero.
1	Reserved	Program to one.
0	Reserved	Program to zero.

Register 04h. Transmit Control

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	1	BBG[1:0]		FIF[3:0]				0	0	0	0

Bit	Name	Function
17:11	Reserved	Program to zero.
10	Reserved	Program to one.
9:8	BBG[1:0]	**TX Baseband Input Full Scale Differential Input Voltage.** 10 = Reserved. 11 = 2.0 V_{PPD} 00 = 1.6 V_{PPD} (default). 01 = 1.2 V_{PPD} **Note:** Refer to Table 6 on page 11 for minimum and maximum values. Set this register to the nearest value.
7:4	FIF[3:0]	**TX IF Filter Cutoff Frequency.** 0111 = Use for GSM 850, E-GSM 900 and PCS 1900 bands. 0110 = Use for DCS 1800 band. **Note:** Use the recommended setting for each band. Other settings reserved.
3:0	Reserved	Program to zero.

Register 05h. Receive Gain

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	DGAIN[5:0]						0	AGAIN[2:0]			LNAC[1:0]		LNAG[1:0]	

Bit	Name	Function
17:14	Reserved	Program to zero.
13:8	DGAIN[5:0]	**Digital PGA Gain Control.** 00h = 0 dB (default). 01h = 1 dB. ... 3Fh = 63 dB. **Note:** See "AN51: Aero Transceiver AGC Strategy" for details on setting the gain registers.
7	Reserved	Program to zero.
6:4	AGAIN[2:0]	**Analog PGA Gain Control.** 000 = 0 dB (default). 001 = 4 dB. 010 = 8 dB. 011 = 12 dB. 100 = 16 dB. 101 = Reserved. 110 = Reserved. 111 = Reserved. **Note:** See "AN51: Aero Transceiver AGC Strategy" for details on setting the gain registers.
3:2	LNAC[1:0]	**LNA Bias Current Control.** 00 = Minimum current (default). 01 = Maximum current. 10 = Reserved. 11 = Reserved. **Note:** Program these bits to the same value as same as LNAG[1:0].
1:0	LNAG[1:0]	**LNA Gain Control.** 00 = Minimum gain (default). 01 = Maximum gain. 10 = Reserved. 11 = Reserved. **Notes:** **1.** Program these bits to the same value as LNAC[1:0]. **2.** See "AN51: Aero Transceiver AGC Strategy" for details on setting the gain registers.

Register 11h. Configuration

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	DPDS[2:0]			XPD1	1	XSEL	0	1	0	1	0	0	0	CSEL

Bit	Name	Function
17:14	Reserved	Program to zero.
13:11	DPDS[2:0]	**Data Path Delayed Start.** 111= Use for GSM 850 and GSM 900 bands. 011= Use for DCS 1800 and PCS 1900 bands (default). **Note:** Use the recommended setting for each band. Other settings reserved.
10	XPD1	**Reference Buffer Powerdown.** 0 = Reference buffer always powered up (default). 1 = Reference buffer powered down when not in use. **Note:** This bit should be set to 0 during normal operation. To achieve lowest Si4206 powerdown current (I_{PDN1}), this bit should be set to 1.
9	Reserved	Program to one.
8	XSEL	**Reference Frequency Select.** 0 = No divider. XIN = 13 MHz (default). 1 = Divide XIN by 2. XIN = 26 MHz. **Note:** The internal clock should always be 13 MHz.
7	Reserved	Program to zero.
6	Reserved	Program to one.
5	Reserved	Program to zero.
4	Reserved	Program to one.
3:1	Reserved	Program to zero.
0	CSEL	**Digital IIR Coefficient Select.** 0 = High selectivity filter (default). 1 = Low selectivity filter.

Register 12h. DAC Configuration

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	1	XBUF	0	ZDBS	ZERODEL[2:0]			DACCM[1:0]		DACFS[1:0]	

Bit	Name	Function
17:11	Reserved	Program to zero.
10	Reserved	Program to one.
9	XBUF	**Reference Buffer Power Control.** 0 = Reference buffer powered down when not in use. 1 = Reference buffer always powered up (default). **Note:** This bit should be set to 1 during normal operation. To achieve the lowest Aero I+ powerdown current (I_{PDN1}), this bit should be set to 0.
8	Reserved	Program to zero.
7	ZDBS	**ZERODEL Band Select.** 0 = Use ZERODEL[2:0] settings corresponding to DCS/PCS column (default). 1 = Use RXBAND[1:0] to determine ZERODEL[2:0] delay setting (GSM or DCS/PCS).
6:4	ZERODEL[2:0]	**RX Output Zero Delay.** Code GSM DCS/PCS 000: 90 µs 130 µs (default) 001: 110 µs 150 µs 010: 130 µs 170 µs 011: 140 µs 180 µs 100: 150 µs 190 µs 101: 160 µs 200 µs 110: 180 µs 220 µs 111: Reserved **Note:** DAC input is forced to zero after $\overline{PDN}$ is deasserted. This feature can be used by the baseband processor to cancel the Si4206 DAC dc offset. Offsets induced on channels due to 13 MHz harmonics will not be included in the calibrated value.
3:2	DACCM[1:0]	**RX Output Common Mode Voltage.** 00 = 1.0 V. 01 = 1.25 V (default). 10 = 1.35 V. 11 = Reserved.
1:0	DACFS[1:0]	**RX Output Differential Full Scale Voltage.** 00 = 1.0 V_{PPD}. 01 = 2.0 V_{PPD} (default). 10 = 3.5 V_{PPD}. 11 = Reserved.

Register 19h. Reserved

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Function
17:0	Reserved	Program to zero.

Register 20h. RX Master #1

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXBAND[1:0]	N_{RF1}[15:0]																

Notes:
1. See registers 03h and 33h for bit definitions.
2. When this register is written, the PDIB bit is automatically set to 0, the PDRB bit is set to 1 and the RFUP bit is set as a function of RXBAND[1:0].

Register 21h. RX Master #2

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	DPDS[2:0]			LNAC[1:0]		LNAG[1:0]		AGAIN[2:0]			0	DGAIN[5:0]					

Note: See registers 05h and 11h for bit definitions.

Register 22h. RX Master #3

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	DGAIN[5:0]					

Notes:
1. See register 05h for bit definitions.
2. The DGAIN[5:0] in register 22h can be changed without powering down.

Register 23h. TX Master #1

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXBAND[1:0]		N_{RF2}[15:0]															

Notes:
1. See registers 03h and 34h for bit definitions.
2. When this register is written, the PDIB bit is automatically set to 1, and the PDRB bit is set to 1.

Register 24h. TX Master #2

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FIF[3:0]				N_{IF}[13:0]													

Note: See registers 04h and 35h for bit definitions.

Register 28h. CDAC (Si4134T)

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	CDAC[5:0]					

Bit	Name	Function
17:6	Reserved	Read as zero.
5:0	CDAC[5:0]	**DCXO Coarse Frequency DAC Adjustment.** 64 steps. 1.0 ppm typical per step. An increase in CDAC results in a lower oscillating frequency. Likewise, a decrease in CDAC results in a higher oscillating frequency. 000000 = Highest frequency ... 111111 = Lowest frequency

Register 31h. Main Configuration

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	SDOSEL[3:0]				0	0	0	0	0	0	RFUP	DIV2	0	0	0

Bit	Name	Function
17:15	Reserved	Program to zero.
14:11	SDOSEL[3:0]	**SDO Output Control Register.** The mux_output table is as follows: 0000 Connected to the Output Shift Register (default). 0001 Force the Output to Low. 0010 Reference Clock. 0011 Lock Detect (LDETB) Signal from Phase Detectors. 1111 High Impedance. **Notes:** **1.** SDO is high-impedance when $\overline{\text{PDN}}$ = 0. **2.** SDO is Serial Data Output when in register read mode.
10:5	Reserved	Program to zero.
4	RFUP	**RF PLL Update Rate (RF1 VCO only).** 0 = 200 kHz update rate (Receive GSM modes). 1 = 100 kHz update rate (Receive DCS and PCS modes). **Notes:** **1.** This bit is set to 1 when register 20h D[17:16] = 01b or 10b (DCS 1800 or PCS 1900 receive modes) and is set to 0 when D[17:16] = 00b or 11b (GSM 850 or GSM 900 modes). **2.** This bit is set to 0 when register 23h is written (transmit mode)
3	DIV2	**Input Clock Frequency.** 0 = No divider. XIN = 13 MHz. 1 = Divide XIN by 2. XIN = 26 MHz.
2:0	Reserved	Program to zero.

Register 32h. Powerdown

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PDIB	PDRB

Bit	Name	Function
17:2	Reserved	Program to zero.
1	PDIB	**Powerdown IF PLL.** 0 = IF synthesizer powered down. 1 = IF synthesizer powered up when the $\overline{\text{PDN}}$ pin is high. **Notes:** **1.** The IF PLL is only used in transmit mode. Powerdown for receive mode. **2.** This bit is set to 0 when register 20h is written (receive mode). **3.** This bit is set to 1 when register 23h is written (transmit mode).
0	PDRB	**Powerdown RF PLL.** 0 = RF synthesizer powered down. 1 = RF synthesizer powered up when the $\overline{\text{PDN}}$ pin is high. **Notes:** **1.** This bit is set to 1 when register 20h is written (receive mode). **2.** This bit is set to 1 when register 23h is written (transmit mode).

Register 33h. RF1 N Divider

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	N_{RF1}[15:0]															

Bit	Name	Function
17:16	Reserved	Program to zero.
15:0	N_{RF1}[15:0]	**N Divider for RF PLL (RF1 VCO).** Used for receive mode.

Register 34h. RF2 N Divider

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	N_{RF2}[15:0]															

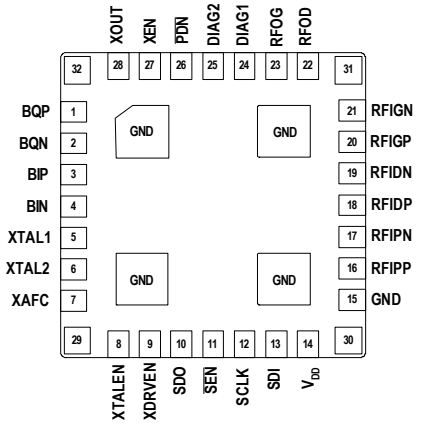
Bit	Name	Function
17:16	Reserved	Program to zero.
15:0	N_{RF2}[15:0]	**N Divider for RF PLL (RF2 VCO).** Used for transmit mode.

Register 35h. IF N Divider

Bit	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	N_{IF}[15:0]															

Bit	Name	Function
17:16	Reserved	Program to zero.
15:0	N_{IF}[15:0]	**N Divider for IF PLL.** Used for transmit mode.

6. Pin Descriptions: Si4206-BM



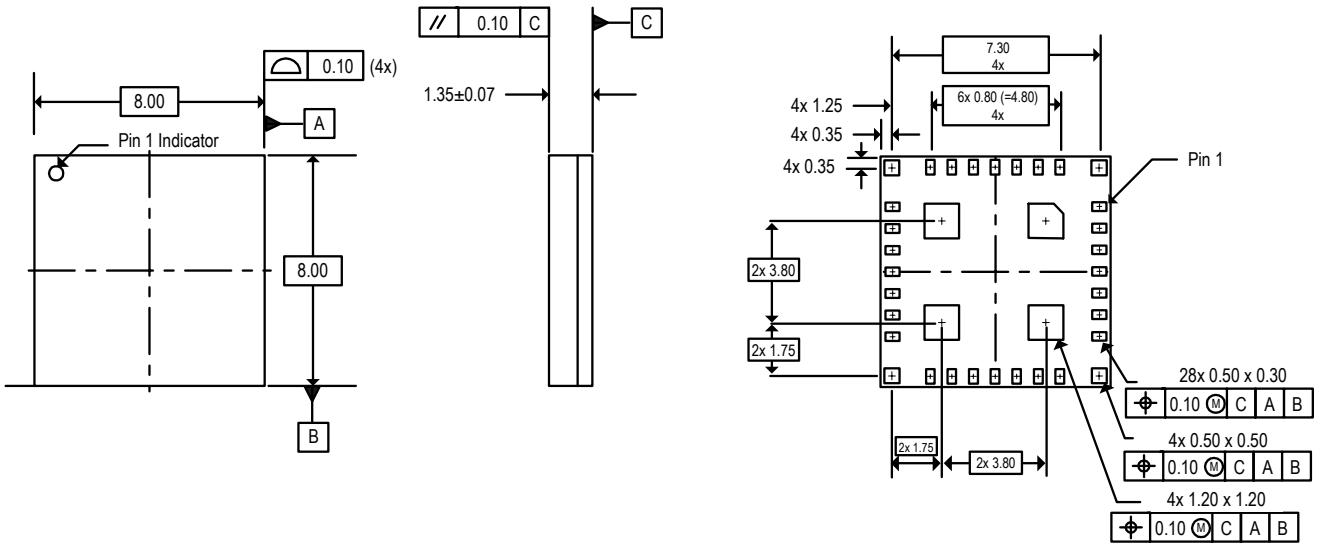
Pin Number(s)	Name	Description
1, 2	BQP, BQN	Transmit/Receive Q signal (differential).
3, 4	BIP, BIN	Transmit/Receive I signal (differential).
5	XTAL1	Crystal input.
6	XTAL2	Crystal output.
7	XAFC	Baseband AFC signal input.
8	XTALEN	Crystal enable.
9	XDRVEN	XDRV enable.
10	SDO	Serial data output.
11	$\overline{SEN}$	Serial enable input (active low).
12	SCLK	Serial clock input.
13	SDI	Serial data input.
14, 30, 32	V_{DD}	Supply voltage.
15, 29, 31	GND	Ground. Connect to ground plane on PCB.
16, 17	RFIPP, RFIPN	PCS LNA input (differential). Use for PCS 1900 band.
18, 19	RFIDP, RFIDN	DCS LNA input (differential). Use for DCS 1800 band.
20, 21	RFIGP, RFIGN	GSM LNA input (differential). Use for GSM 850 or E-GSM 900 bands.
22	RFOD	DCS and PCS transmit output to power amplifier. Use for DCS 1800 and PCS 1900 bands.
23	RFOG	GSM transmit output to power amplifier. Use for GSM 850 and E-GSM 900 bands.
24, 25	DIAG1, DIAG2	Diagnostic output. Can be used as digital outputs to control antenna switch functions.
26	$\overline{PDN}$	Powerdown input (active low).
27	XEN	XOUT pin enable.
28	XOUT	Clock output to baseband.

7. Ordering Guide

Part Number	Description	Operating Temperature
Si4206-BM	Tri-band Transceiver with DCXO GSM 850 or E-GSM 900, DCS 1800, PCS 1900	–20 to 85 °C

Note: Add an “R” at the end of the part number to denote tape and reel option; 2500 quantity per reel. The Si4206 is a lead-free device.

8. Package Outline: Si4206-BM



Top View **Side View** **Bottom View**

Figure 17. 32-Pin Land Grid Array (LGA)

Notes:

1. Dimensions in mm.
2. Approximate device weight is 184 mg.

DOCUMENT CHANGE LIST

Revision 0.81 to Revision 1.0

- Table 8 on page 14 updated.
  - CVAR Range, CDAC Range, and CFIX updated.
- Functional Description text on page 19 updated.
- Figure 15, “DCXO System Signal Routing Diagram,” on page 21 updated.
- "Ordering Guide" on page 36 updated.

NOTES:

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