

1-Mbit (128K x 8) Static RAM

Features

- Temperature Ranges
 - Automotive-E: -40 °C to 125 °C
- 4.5 V – 5.5 V operation
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Low active power
137.5 mW (max.) (25 mA)
- Low standby power
137.5 μW (max.) (25 μA)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} options
- Available in Pb-free 32-pin (450 mil-wide) small outline integrated circuit (SOIC) package

Functional Description

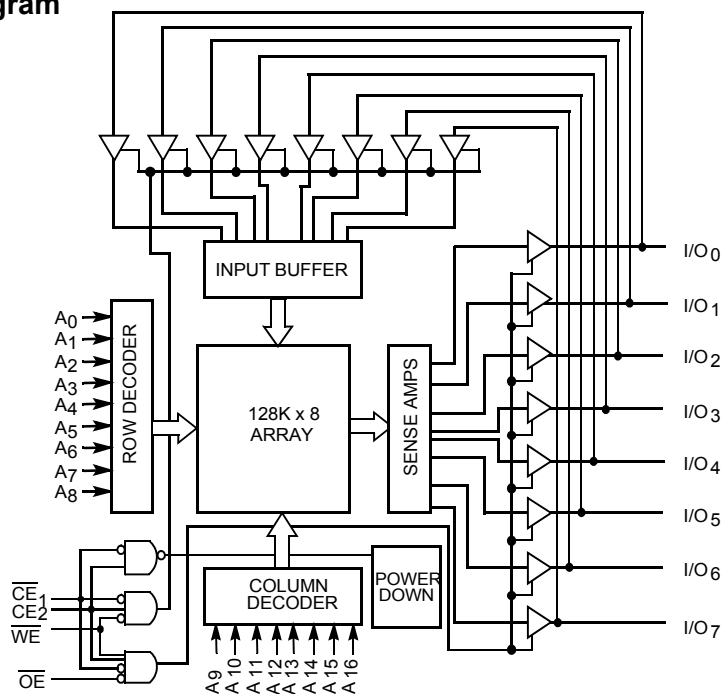
The CY621282BN^[1] is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}_1), an active HIGH Chip Enable (CE_2), and active LOW Output Enable (\overline{OE}). This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking Chip Enable One (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable One (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

Logic Block Diagram



Note

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

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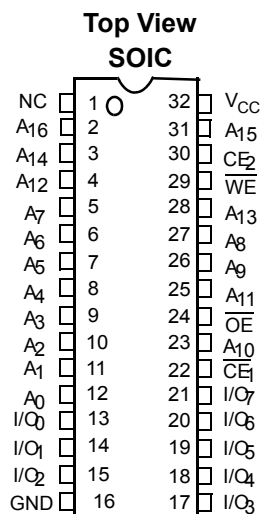
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Product Portfolio

Product		V _{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
		Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max
CY621282BN	Automotive-E	4.5	5.0	5.5	70	6	25	2.5	25

Pin Configuration

Figure 1. Pin Configuration



Pin Definition

Input	A₀–A₁₆ . Address inputs
Input/output	I/O₀–I/O₇ . Data lines. Used as input or output lines depending on operation
Input/control	WE . Write Enable, Active LOW. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
Input/control	CE₁ . Chip Enable 1, Active LOW.
Input/control	CE₂ . Chip Enable 2, Active HIGH.
Input/control	OE . Output Enable, Active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins
Ground	GND . Ground for the device
Power supply	V_{CC} . Power supply for the device

Note

2. Typical values are included for reference only and are not tested or guaranteed. Typical values are measured at V_{CC} = 5.0 V, T_A = 25 °C

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage on V_{CC} to relative GND^[3] -0.5 V to +7.0 V
 DC voltage applied to outputs in High-Z state^[3] -0.5 V to V_{CC} + 0.5 V

DC input voltage^[3,4] -0.5 V to V_{CC} + 0.5 V
 Current into outputs (LOW) 20 mA
 Static discharge voltage > 2001 V (per MIL-STD-883, Method 3015)
 Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Automotive-E	-40 °C to +125 °C	5 V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-70			Unit
			Min	Typ ^[5]	Max	
V _{OH}	Output HIGH voltage	V _{CC} = 4.5 V, I _{OH} = -1.0 mA	2.4	-	-	V
		V _{CC} = 5.5 V, I _{OH} = -0.1 mA	3.95	-	-	
		V _{CC} = 5 V, I _{OH} = -0.1 mA	3.6	-	-	
		V _{CC} = 4.5 V, I _{OH} = -0.1 mA	3.25	-	-	
V _{OL}	Output LOW voltage	V _{CC} = 4.5 V, I _{OL} = 2.1 mA	-	-	0.4	V
V _{IH}	Input HIGH voltage		2.2	-	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage ^[3]		-0.3	-	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-10	-	+10	μA
I _{OZ}	Output leakage current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10		+10	μA
I _{CC}	V _{CC} operating supply current	f = f _{MAX} = 1/t _{RC}		6	25	mA
		f = 1 MHz				
I _{SB1}	Automatic CE Power-down current —TTL inputs	V _{CC} = 5.5 V, CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	-	0.1	2	mA
I _{SB2}	Automatic CE Power-down current —CMOS inputs	V _{CC} = 5.5 V, CE ₁ ≥ V _{CC} - 0.3 V, or CE ₂ ≤ 0.3 V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	-	2.5	25	μA

Notes

- V_{IL} (min.) = -2.0 V for pulse durations of less than 20 ns.
- No input may exceed V_{CC} + 0.5 V.
- Typical values are included for reference only and are not tested or guaranteed. Typical values are measured at V_{CC} = 5.0 V, T_A = 25 °C

Capacitance

Parameter ^[6]	Description	Test Conditions	Max.	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{ V}$	9	pF
C_{OUT}	Output capacitance		9	pF

Thermal Resistance

Parameter ^[6]	Description	Test Conditions	32 pin-SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	66.17	$^\circ\text{C} / \text{W}$
Θ_{JC}	Thermal resistance (junction to case)		30.87	$^\circ\text{C} / \text{W}$

Figure 2. AC Test Loads and Waveforms

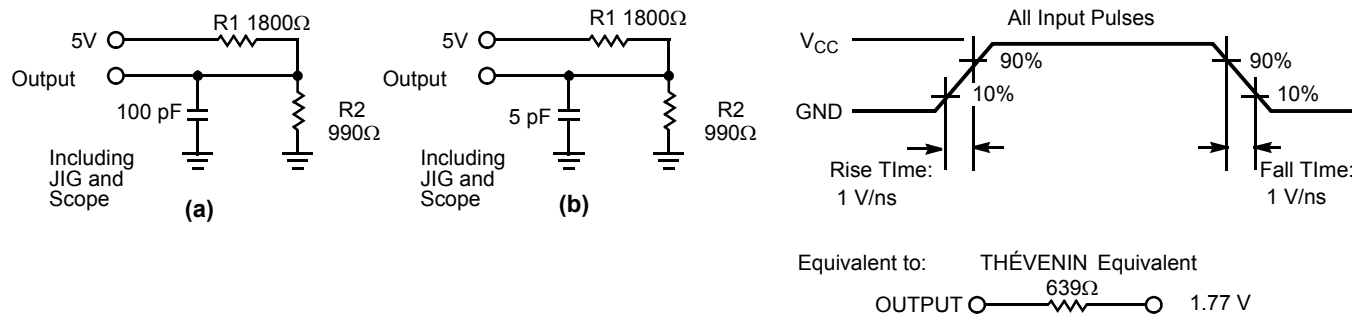
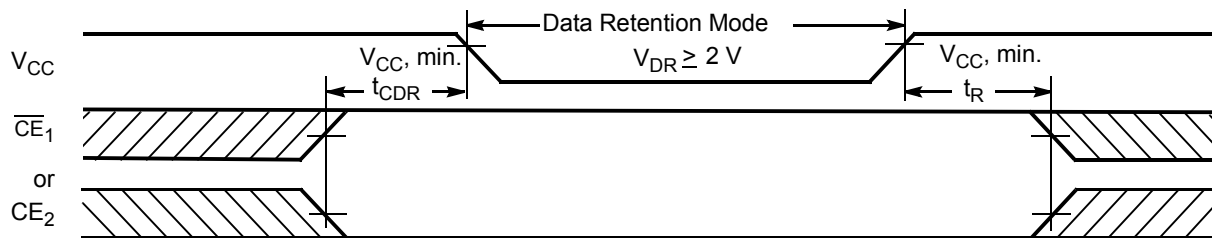


Figure 3. Data Retention Waveform



Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ	Max	Unit	
V_{DR}	V_{CC} for data retention		2.0	–	–	V	
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $CE_1 \geq V_{CC} - 0.3\text{ V}$, or $CE_2 \leq 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or, $V_{IN} \leq 0.3\text{ V}$	Automotive-E	–	1.5	25	μA
t_{CDR}	Chip deselect to data retention time		0	–	–	ns	
t_R	Operation recovery time		70	–	–	ns	

Note

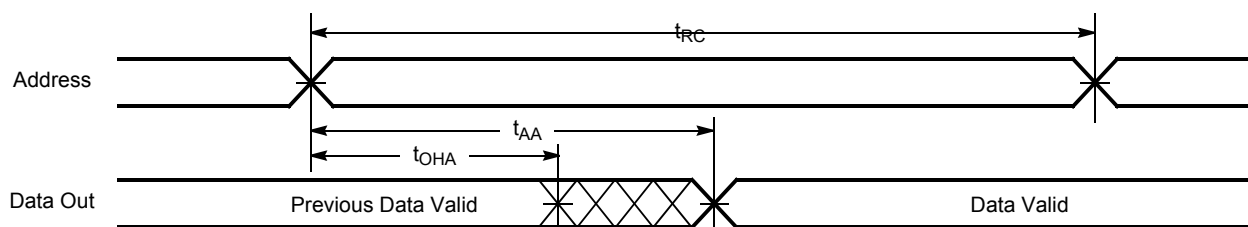
6. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range

Parameter ^[7]	Description	CY621282BN-70		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	70	–	ns
t_{AA}	Address to data valid	–	70	ns
t_{OHA}	Data hold from address change	5	–	ns
t_{ACE}	\overline{CE}_1 LOW to data valid, CE_2 HIGH to data valid	–	70	ns
t_{DOE}	\overline{OE} LOW to data valid	–	35	ns
t_{LZOE}	\overline{OE} LOW to Low Z	0	–	ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7, 9]	–	25	ns
t_{LZCE}	\overline{CE}_1 LOW to Low Z, CE_2 HIGH to Low Z ^[9]	5	–	ns
t_{HZCE}	\overline{CE}_1 HIGH to High Z, CE_2 LOW to High Z ^[8, 9]	–	25	ns
t_{PU}	\overline{CE}_1 LOW to Power-up, CE_2 HIGH to power-up	0	–	ns
t_{PD}	\overline{CE}_1 HIGH to Power-down, CE_2 LOW to power-down	–	70	ns
Write Cycle^[10]				
t_{WC}	Write cycle time	70	–	ns
t_{SCE}	\overline{CE}_1 LOW to Write End, CE_2 HIGH to write end	60	–	ns
t_{AW}	Address set-up to write end	60	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	50	–	ns
t_{SD}	Data set-up to write end	30	–	ns
t_{HD}	Data Hold from write end	0	–	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[9]	5	–	ns
t_{HZWE}	\overline{WE} LOW to High Z ^[8, 9]	–	25	ns

Switching Waveforms

Figure 4. Read Cycle No.1^[11, 12]



Notes

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW. \overline{CE}_1 and \overline{WE} must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
- \overline{WE} is HIGH for read cycle.

Switching Waveforms (continued)

Figure 5. Read Cycle No. 2 $\overline{\text{OE}}$ Controlled^[13, 14]

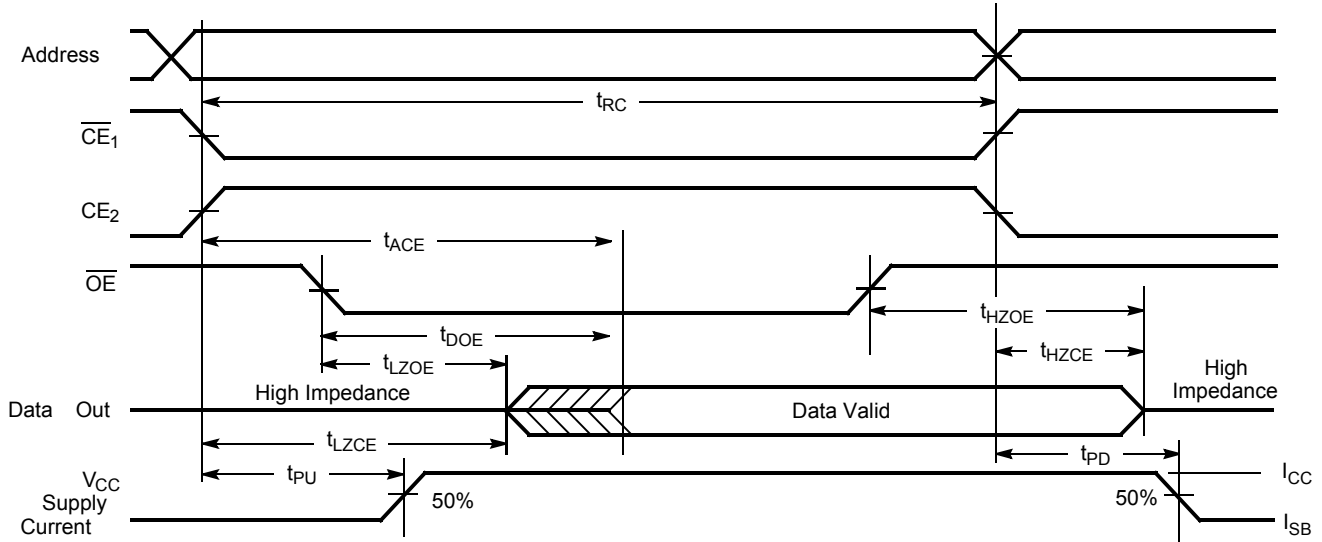
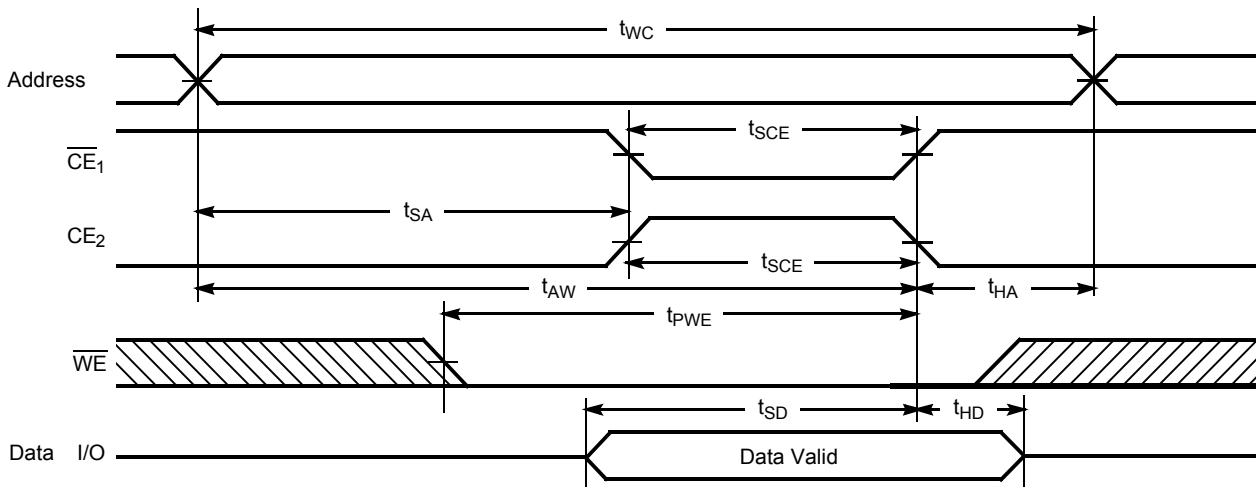


Figure 6. Write Cycle No. 1 $\overline{\text{CE}}_1$ or CE_2 Controlled^[15, 16]



Notes

- 13. $\overline{\text{WE}}$ is HIGH for read cycle.
- 14. Address valid prior to or coincident with $\overline{\text{CE}}_1$ transition LOW and CE_2 transition HIGH.
- 15. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 16. If $\overline{\text{CE}}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 \overline{WE} Controlled, \overline{OE} HIGH During Write^[17, 18]

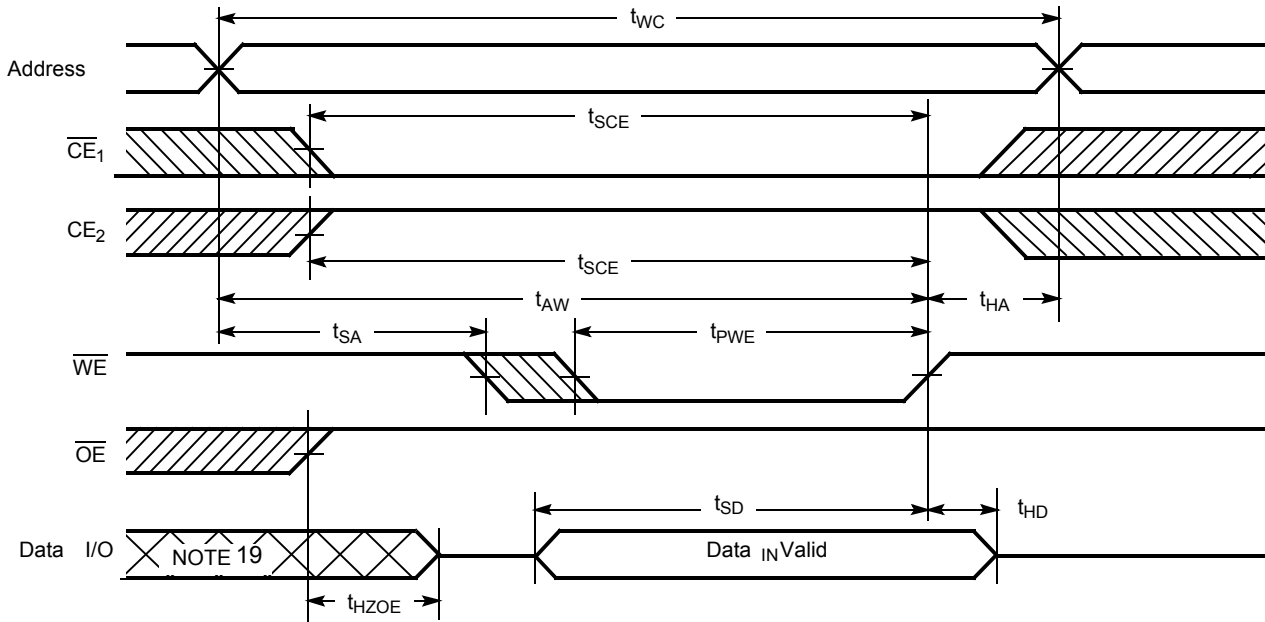
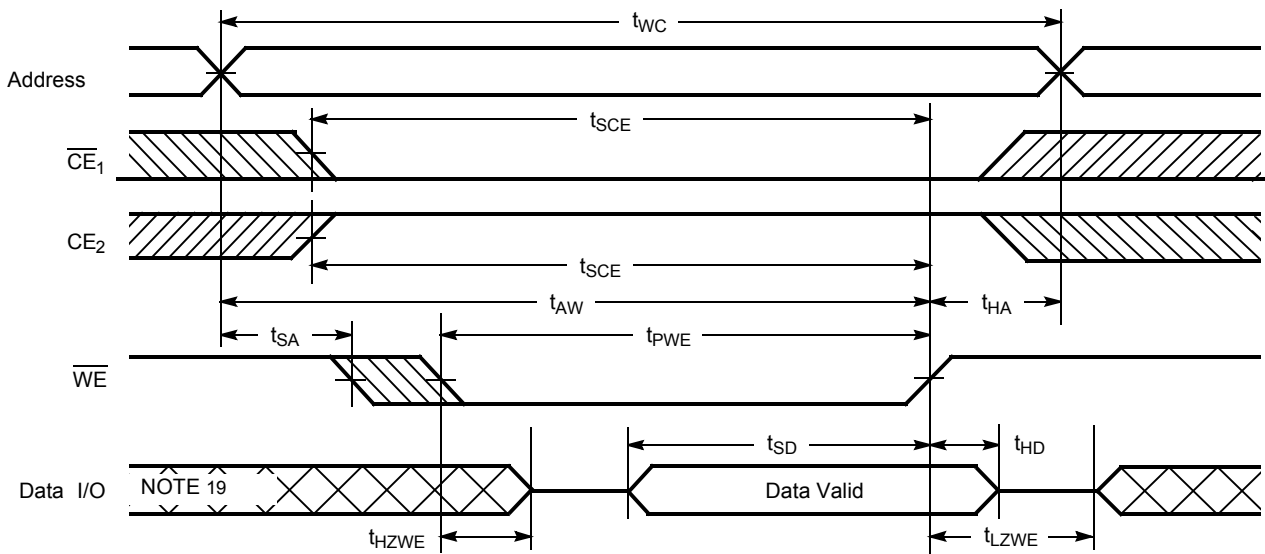


Figure 8. Write Cycle No.3 \overline{WE} Controlled, \overline{OE} LOW^[17, 18]



Notes

- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. If \overline{CE}_1 goes HIGH or \overline{CE}_2 goes LOW simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.
- 19. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

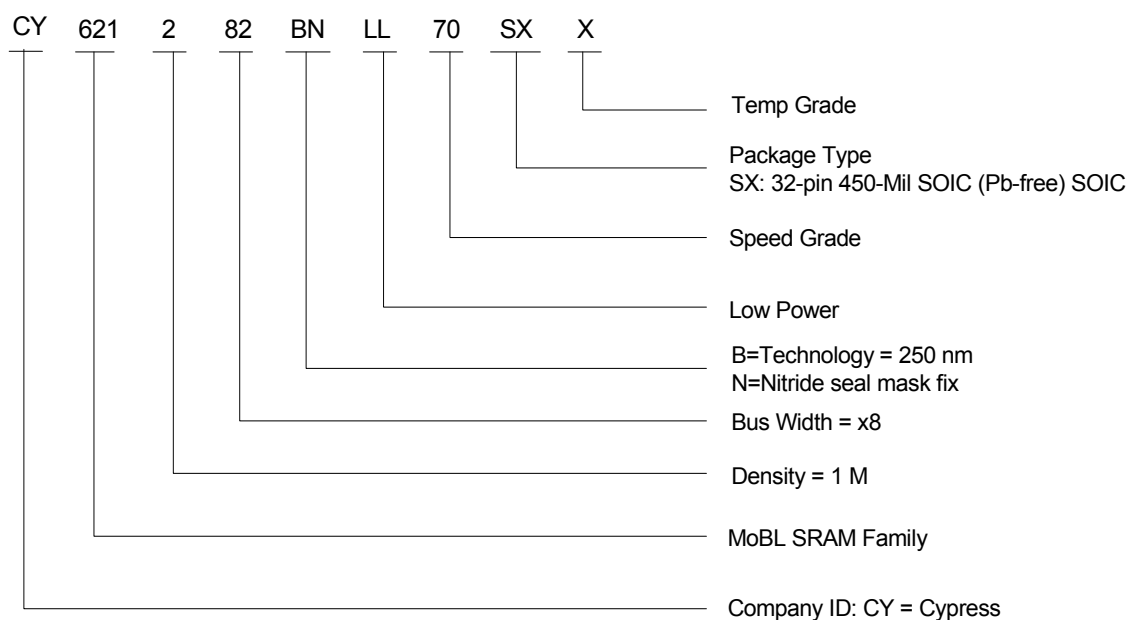
\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High Z	Power-down	Standby (I _{SB})
X	L	X	X	High Z	Power-down	Standby (I _{SB})
L	H	L	H	Data out	Read	Active (I _{CC})
L	H	X	L	Data in	Write	Active (I _{CC})
L	H	H	H	High Z	Selected, Outputs disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY621282BNLL-70SX	51-85081	32-pin 450-Mil SOIC (Pb-free)	Automotive-E

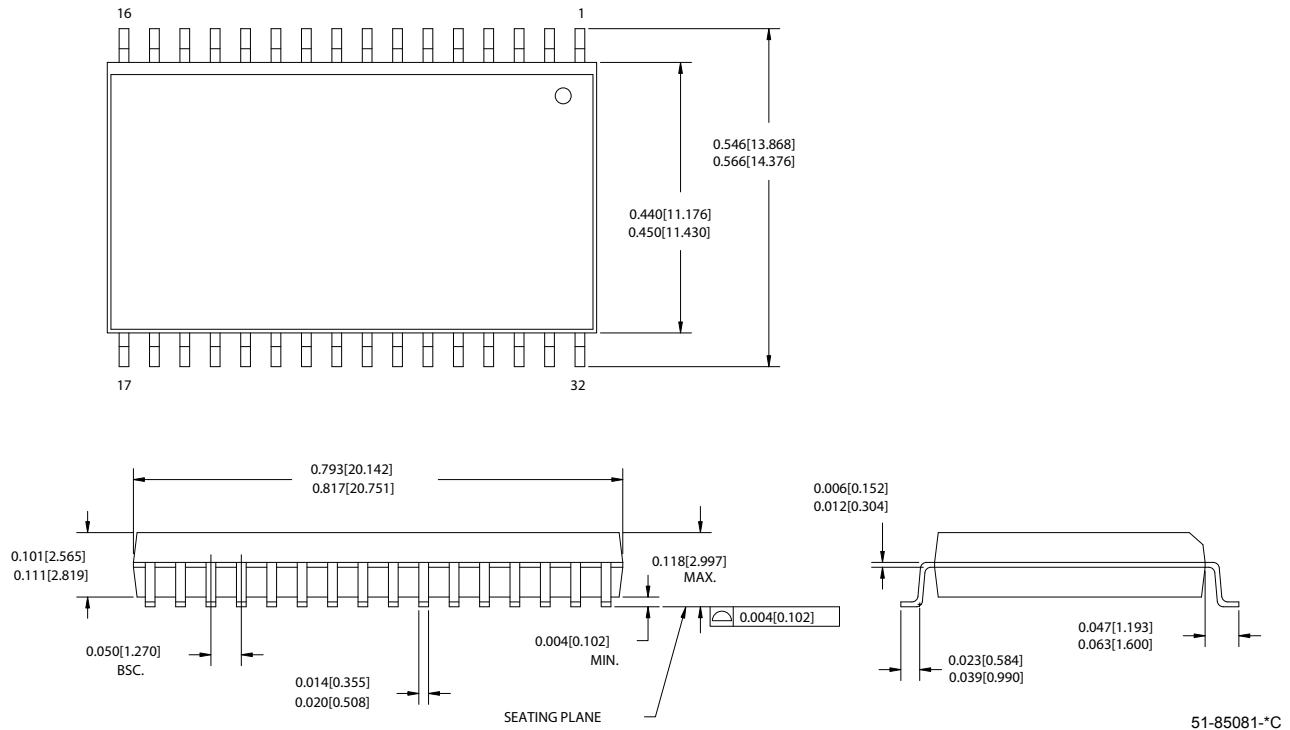
Please contact your local Cypress sales representative for availability of these parts

Ordering Code Definition



Package Diagrams

32-pin (450 Mil) Molded SOIC (51-85081)



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Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
SOIC	small outline integrated circuit
I/O	input/output
SRAM	static random access memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celcius
μA	micro Amperes
mA	milli Amperes
MHz	Mega Hertz
mV	milli Volts
ns	nano seconds
pF	pico Farad
V	Volts
Ω	Ohms
W	Watts

Document History Page

Document Title: CY621282BN MoBL [®] Automotive 1-Mbit (128K x 8) Static RAM				
Document Number: 001-65526				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	3115909	01/06/2011	RAME	New Data Sheet

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