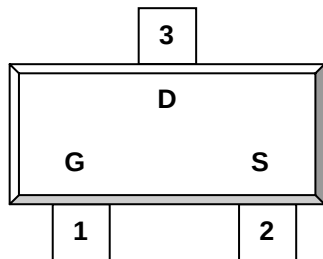


DESCRIPTION

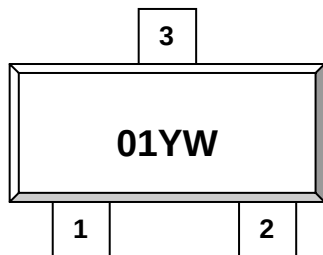
STP7401 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION SOT-323 (SC-70)



1.Gate 2.Source 3.Drain

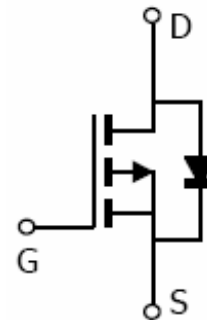
PART MARKING SOT-323



Y: Year Code A: Process Code

FEATURE

- -30V/-2.8A, $R_{DS(ON)} = 115m\Omega$ @ $V_{GS} = -10V$
- -30V/-2.5A, $R_{DS(ON)} = 135m\Omega$ @ $V_{GS} = -4.5V$
- -30V/-1.5A, $R_{DS(ON)} = 170m\Omega$ @ $V_{GS} = -2.5V$
- -30V/-1.0A, $R_{DS(ON)} = 240m\Omega$ @ $V_{GS} = -1.8V$
- Super high density cell design for Extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-323 (SC-70) package design



ORDERING INFORMATION

Part Number	Package	Part Marking
STP7401S32RG	SOT-323	01YW

※ Process Code : A ~ Z ; a ~ z

※ ST7401S32RG S32 : SOT-23-3L ; R : Tape Reel ; G : Pb – Free

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
<http://www.stansontech.com>

**STP7401**

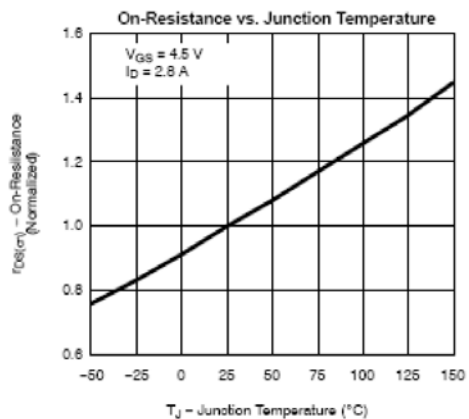
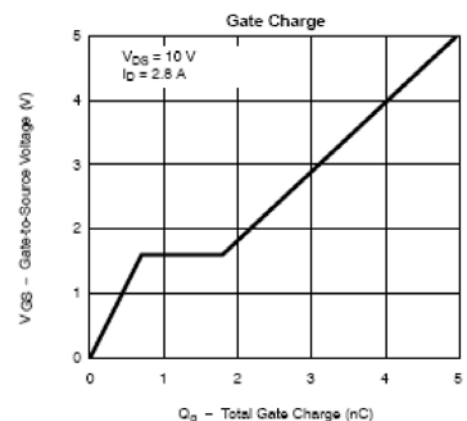
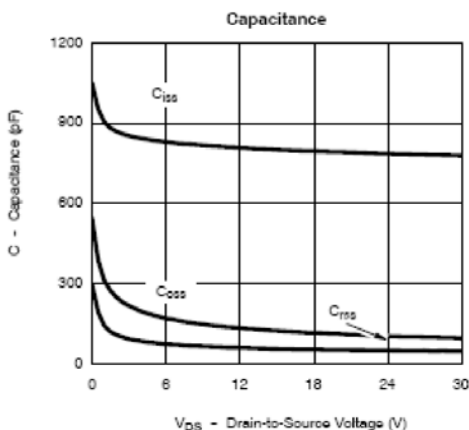
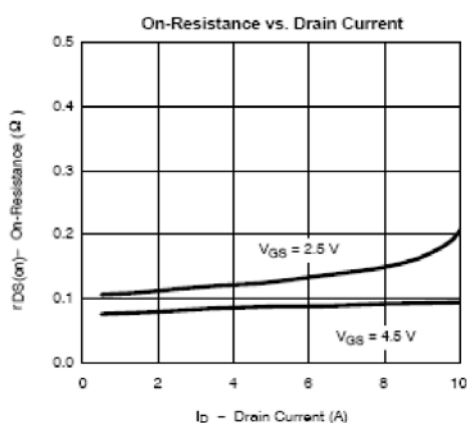
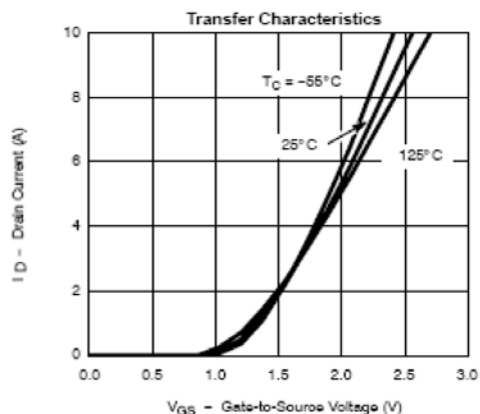
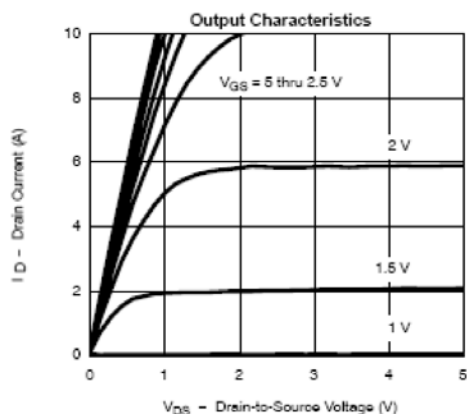
P Channel Enhancement Mode MOSFET

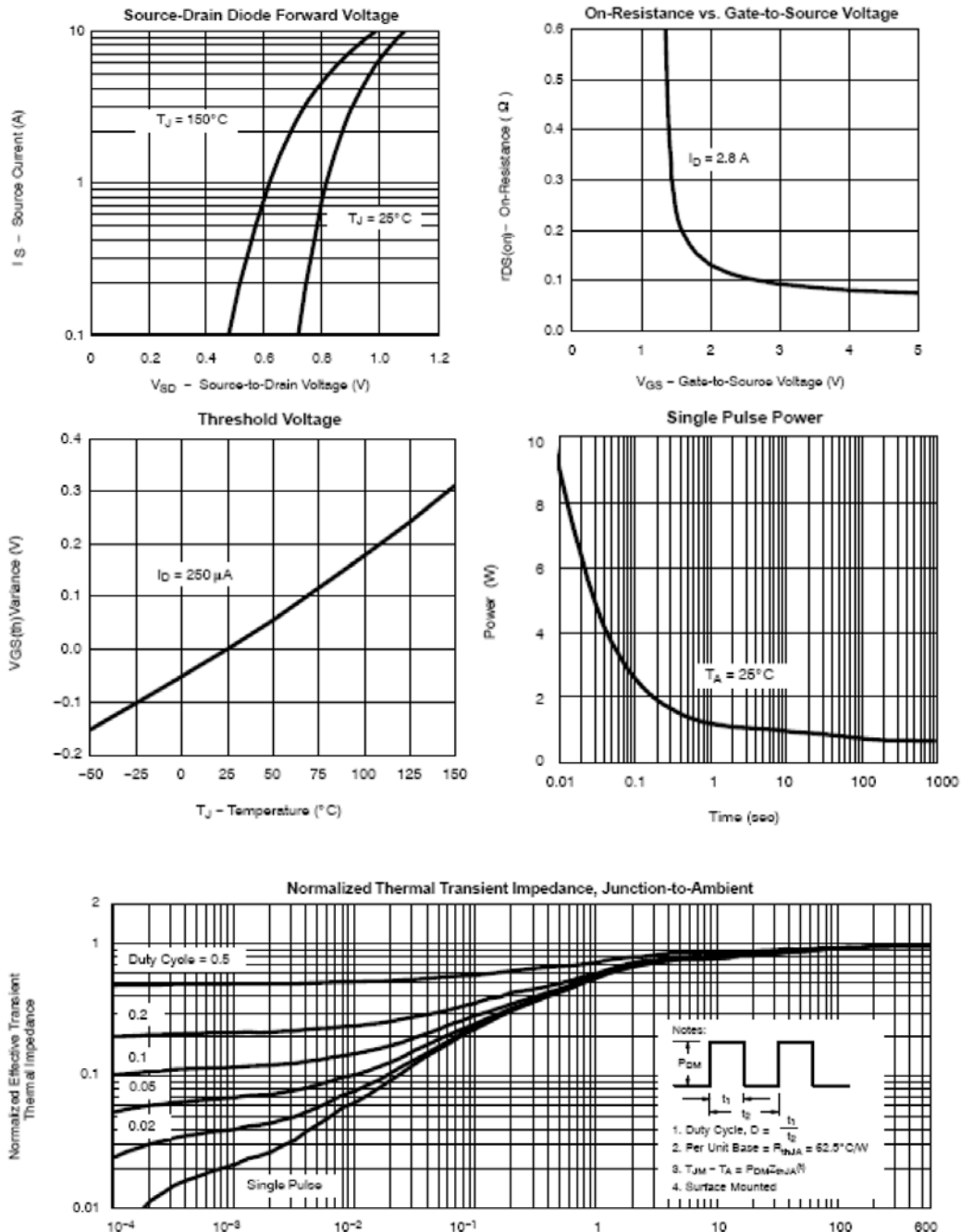
-2.8A**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted)

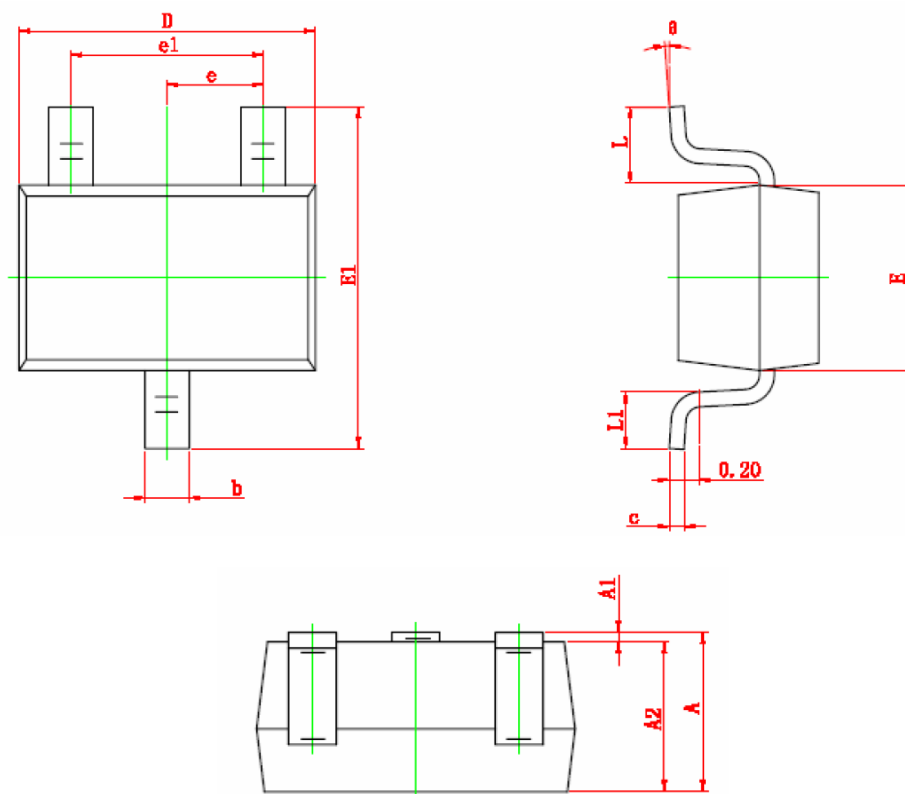
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-30	V
Gate-Source Voltage		V _{GSS}	±12	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	-2.8 -2.1	A
Pulsed Drain Current		I _{DM}	-8	A
Continuous Source Current (Diode Conduction)		I _S	-1.4	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	0.33 0.21	W
Operation Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	105	°C/W

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4		-1.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$			-1	μA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=85^{\circ}C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-4.5V$	-4.0			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-2.8A$ $V_{GS}=-4.5V, I_D=-2.5A$ $V_{GS}=-2.5V, I_D=-1.5A$ $V_{GS}=-1.8V, I_D=-1.0A$		105 125 155 210	115 135 170 240	$m\Omega$
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-4.0V$		4		S
Diode Forward Voltage	V_{SD}	$I_S=-1.0A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V$ $V_{GS}=-4.5V$ $I_D=-2.0A$		5.8		nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V$ $V_{GS}=0V$ $F=1MHz$		380		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)tr}$	$V_{DS}=-15V$ $I_D=-1A$ $R_L=15\Omega$ $R_G=-3\Omega$ $V_{GEN}=-10V$		6		nS
				3.9		
Turn-Off Time	$t_{d(off)tf}$			40		
				15		

TYPICAL CHARACTERISTICS (25°C unless otherwise noted)


TYPICAL CHARACTERISTICS (25°C unless otherwise noted)


SOT-323 PACKAGE OUTLINE


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°