16/20/24Bit 32/44.1/48kHz Sigma-Delta Stereo DAC DAC0415X

General Description

This product is Sigma-Delta Digital-To-Analog Converter for High grade Digital Audio Applications. The product contains Serial-to-Parallel Interface Converter and Compensation Filter, Digital Volume Attenuator by the Mode Interface, De-Emphasis Filter, FIR filter, Sinc Filter, Digital Sigma-Delta Modulator, Analog Postfilter, AIF (Anti-Image-Filter). The normal input and output channels provides 95dB SNR (Signal to Noise Ratio) over in band (20kHz : Sampling Rate = 44.1KHz).

The product employs the 1bit 4th-order Sigma-Delta architecture with 16bit resolution, over sampling of 64X. And Analog Postfilter with low clock sensitivity and Linear phase, filters the Shaping-Nosie and outputs Analog voltage with high resolution. An on-chip reference voltage is included to allow single supply operations.

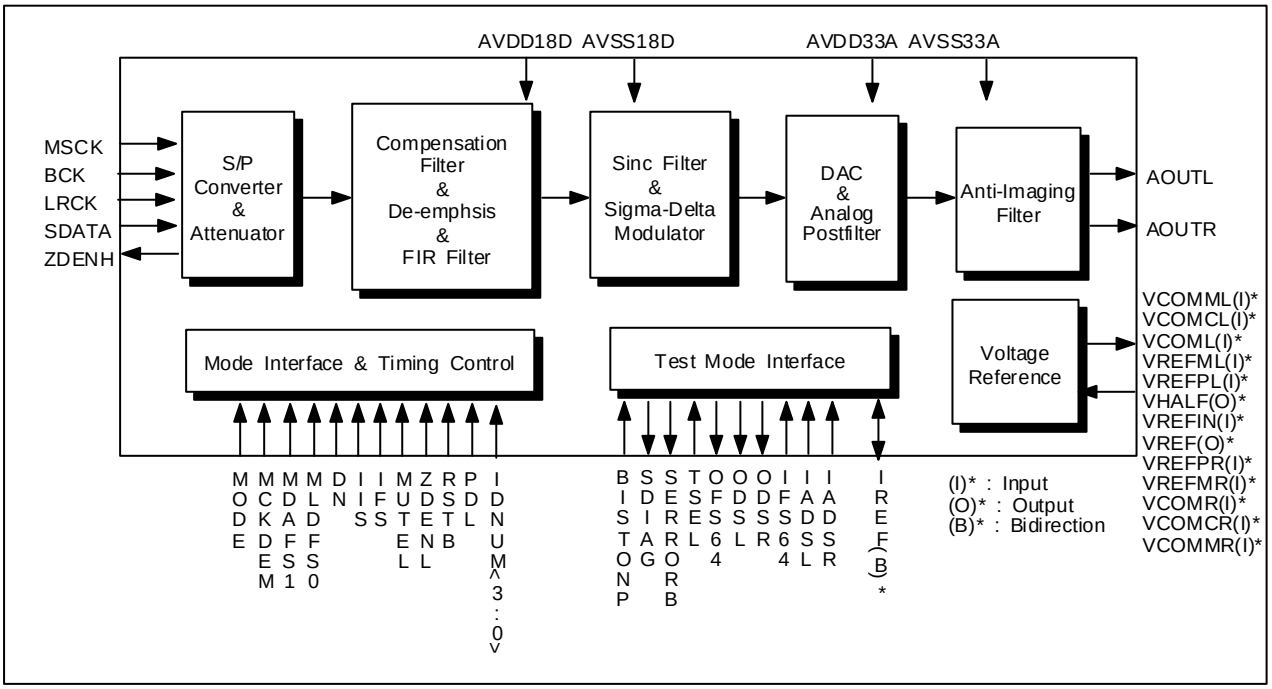
Features

-16/20/24bit Sigma-Delta Digital-to-Analog Converter
-Sampling Frequency Rate 32/44.1/48KHz
-Input Rate 1Fs or 2Fs by Normal Mode/Double Mode Selection
-On-Chip Compensation Filter
-On-Chip 4 times Oversampling Digital Filter
-On-Chip Analog Postfilter
-Filtered Line-Level Outputs, Linear Phase Filtering
-On-Chip Voltage Reference
-Low Clock Jitter Sensitivity
-96dB SNR
-L/R Independent Digital Soft Attenuation
-On-Chip De-Emphasis Filter (32/44.1/48KHz)
-Zero Input Detection Mute
-Soft Mute Control
-Mono/Stereo Setting
-Single 1.8V / 3.3V(Digital/Analog) Power Supply

Applications

CD Player, CD-ROM, MP3 Player, Video-CD, Mini-Disk, DVD etc

Block Diagram



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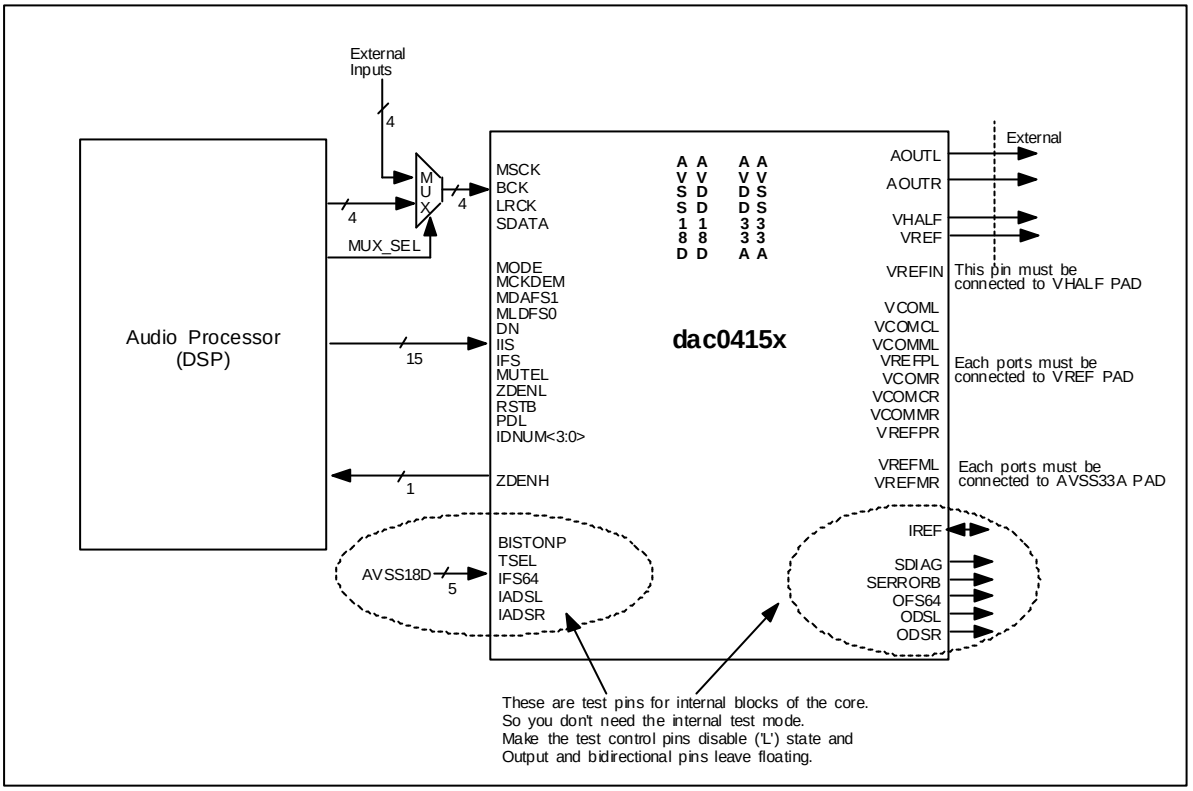
Embedded Core Block Diagram



Embedded Core User Guide

- Digital serial data input and clock input refer to digital input format.
- Digital control pins inform refer to pin description.
- Mode I/F pin inform refer to Mode Interface. IDNUM<3:0> are ID number setting pins for Mode Interface.
- External application of analog output pins refer to application circuit.
- If you want to test only embedded analog core block (Sigma-Delta DAC), you can do it just adding the 4 pins to supply digital serial input data (MSCK, BCK, LRCK, SDATA) and MUX block.
- Analog power(AVDD33A,AVSS33A) and digital power(AVDD18D,AVSS18D) should be separated.
- Bulk Power pin should be connected to analog ground(AVSS33A).
- Two pads should be dedicated to analog power(AVDD33A, AVSS33A)
- If you need not use test mode for the testability of internal core block, you make internal core block test pins disable state. (Test Input pins are 'L' state and Test output, bi-direction pins leave floating)

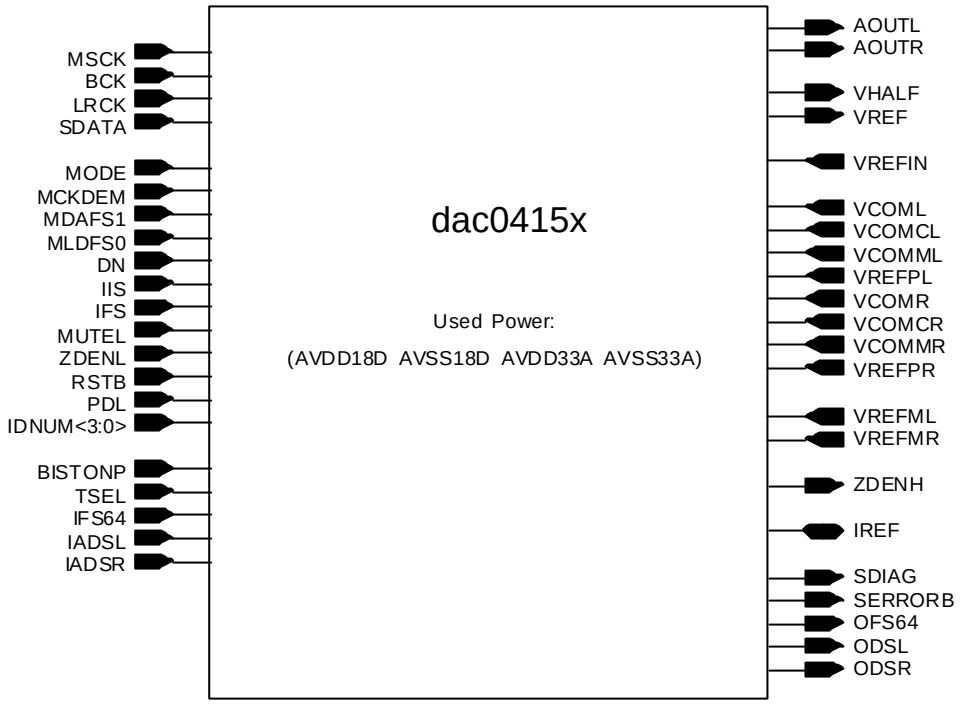
Core Pin Description

SYMBOL	I/O TYPE	I/O PAD	DESCRIPTION
POWER SUPPLY PINS			
AVDD18D	DP	vdd1t_abb	Digital Supply
AVSS18D	DG	vss1t_abb	Digital Ground
AVDD33A	AP	vdd3t_abb	Analog Supply
AVSS33A	AG	vss3t_abb	Analog Ground
DIGITAL PINS			
MSCK	DI	picc_abb	Master Clock Input.
BCK	DI	picc_abb	Bit Clock Input.
LRCK	DI	picc_abb	Sample Rate Clock Input. (Fs or 2Fs)
SDATA	DI	picc_abb	Serial Digital Input
ZDENH	DO	pob2_abb	Zero Data Detection Output When Input Data is continuously zero for more than 4096*sampling time(fs), ZDENH becomes to H
MODE	DI	picc_abb	SoftWare / HardWare Control Select ("H" / "L")
MCKDEM (MCLK / DEEM)	DI	picc_abb	Mode Interface Clock Input / De-Emphasis On/Off. "H" is enabled. "L" is disabled. (When MODE pin is "H", MCLK is active. When MODE pin is "L", DEEM is active)
MDAFS1 (MDATA / SFS1)	DI	picc_abb	Mode Interface Command Data Input / De-Emphasis Frequency Selection1 (When MODE pin is "H", MDATA is active. When MODE pin is "L", SFS1 is active)
MLDFS0 (MLD / SFS0)	DI	picc_abb	Mode Interface Command load Input(when low,load) / De-Emphasis Frequency Selection0 (When MODE pin is "H", MLD is active. When MODE pin is "L", SFS0 is active)
DN	DI	picc_abb	Input Rate Select. High is Double(2Fs) Mode, Low is Normal(Fs) Mode. (When MODE pin is "L" (Hardware mode), this pin is active)
IIS	DI	picc_abb	IIS / Standard Input Format Selection (When MODE pin is "L" (Hardware mode), this pin is active)
IFS	DI	picc_abb	Input Format Selection (When MODE pin is "L" (Hardware mode), this pin is active)
MUTEL	DI	picc_abb	Analog Output Mute. "L" enabled (When MODE pin is "L" (Hardware mode), this pin is active)
ZDENL	DI	picc_abb	Zero Input Detection Enable. "L" is enabled. "H" is disabled (When MODE pin is "L" (Hardware mode), this pin is active)
RSTB	DI	picc_abb	Reset Input. "L" Enabled
PDL	DI	picc_abb	Power Down. "L" enabled
IDNUM<3:0>	DI	picc_abb	Mode Interface ID Number Setting Input
ANALOG PINS			
AOUTL	AO	phoa_abb	Analog Output for L-CH
AOUTR	AO	phoa_abb	Analog Output for R-CH
VHALF	AO	phoa_abb	Reference Voltage Output for Bypass
VREF	AO	phoa_abb	Reference Voltage Output for Bypass
VREFIN	AI		Each ports must be connected to VHALF PAD
VCOML			Each ports must be connected to VREF PAD
VCOMCL			
VCOMML			
VREFPL			
VCOMR			
VCOMCR			
VCOMMR			
VREFPR			

I/O TYPE ABBR.
- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional
- AP : Analog Power
- AG : Analog Ground
- DP : Digital Power
- DG : Digital Ground

VREFML			Each ports must be connected to AVSS33A PAD
VREFMR			
CORE INTERNAL BLOCK TEST PINS			
BISTONP	DI	picc_abb	Memory Bist Test Mode. "H" enabled
SDIAG	DO	pob2_abb	Test Output pin for Embedded memory BIST (BISTONP="H")
SERRORB	DO	pob2_abb	Test Output Pin for Embedded memory BIST (BISTONP="H")
TSEL	DI	picc_abb	Test pin for Analog Postfilter Input Selection
IFS64	DI	picc_abb	64X Sampling Clock Input for Analog Postfilter (When TSEL=H)
IADSL	DI	picc_abb	Inputs for Analog Postfilter of L-CH (When TSEL=H)
IADSR	DI	picc_abb	Inputs for Analog Postfilter of R-CH (When TSEL=H)
OFS64	DO	pob2_abb	64X Sampling Clock output for Digital sigma-delta Modulator
ODSL	DO	pob2_abb	L-CH Output for Digital sigma-delta Modulator.
ODSR	DO	pob2_abb	R-CH Output for Digital sigma-delta Modulator.
IREF	AB	phoa_abb	Test Pin for Analog Supply Current

Core Configurtion



Absolute Maximum Ratings

CHARACTERISTICS	SYMBOL	VALUES		UNITS
DC Supply Voltage	V_{DD}	Digital Supply Voltage	2.7	V
		Analog Supply Voltage	3.8	V
Storage Temperature Range	Tstg	-65 to +150		℃

Recommended Operating Conditions

CHRACTERISTICS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	AVDD18D AVDD18A	1.65 3.0	1.8 3.3	1.95 3.6	V
Operating Temp.	Topr	0	25	70	℃

Electrical Characteristics

(AVDD18D=1.8v,AVDD33A=3.3V, Temp=25℃, Fs=44.1kHz, Signal Frequency=20~20kHz, Cload of AoutL, AoutR=10pF)

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION		24		bits
DYNAMIC PERFORMANCE (16Bit Data)				
SNR[1]	92	96		dB
THD[2]		0.01 -80.0	0.02 -74.0	% dB
SND(THD+Noise)[2]	72	76		dB
Dynamic Range[3]	85	90		dB
Crosstalk[1]	85	90		dB

ANALOG OUTPUT				
Reference Voltage Ouput		0.5 x AVDD33A		V
Frequency Responce		±0.1	±0.5	dB
Voltage Range		0.70 x AVDD33A		Vpp
Load Impedance	10K			Ω
DIGITAL FILTER				
Pass Band Ripple		±0.0072		dB
Stop Band Attenuation		62.7		dB
Pass Band		0.45		Fs
POWER SUPPLY				
Analog Current		5.0	7.0	mA
Digital Current		1.5	1.8	mA
Power Dissipation		19.2	26.34	mW
Power Down Current		20	40	uA

<1> 1kHz 0dB Sinewave Input, EIAJ

<2> 1kHz 0dB Sinewave Input, Not EIAJ

<3> 1kHz -60dB Sinewve Input, and then measured data + 60dB

AC Timing Characteristics (AVDD18D=1.8V, AVSS18D=0V, Fs=48KHz, MSCK=768*FS, 24Bit Input Format, Normal Operation Mode, Software Mode (MODE="High"), Temp=25℃)

CHRACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
MSCK Frequency	Fmsck	-	768*Fs	-	Hz
BCK Frequency	Fbck	-	48*Fs	-	Hz
LRCK Frequency	Flrck	-	1*Fs	-	Hz
MSCK Rising and LRCK Edge Dealay	Tmld	10	-	-	ns
MSCK Risng and LRCK Edge Setup Time	Tmlst	10	-	-	ns
BCK Rising and LRCK Edge Dealay	Tbld	10	-	-	ns
BCK Risng and LRCK Edge Setup Time	Tblst	10	-	-	ns
SDATA and BCK Rising Setup Time	Tsbst	10	-	-	ns
BCK Ring and SDATA Hold Time	Tbsht	10	-	-	ns
MCKDEM Frequency	Fmck	-	-	128*Fs	Hz
MLDFS0 Frequency	Fmld	-	-	1*Fs	Hz
MLDFS0 Load Time	Tload	550			ns

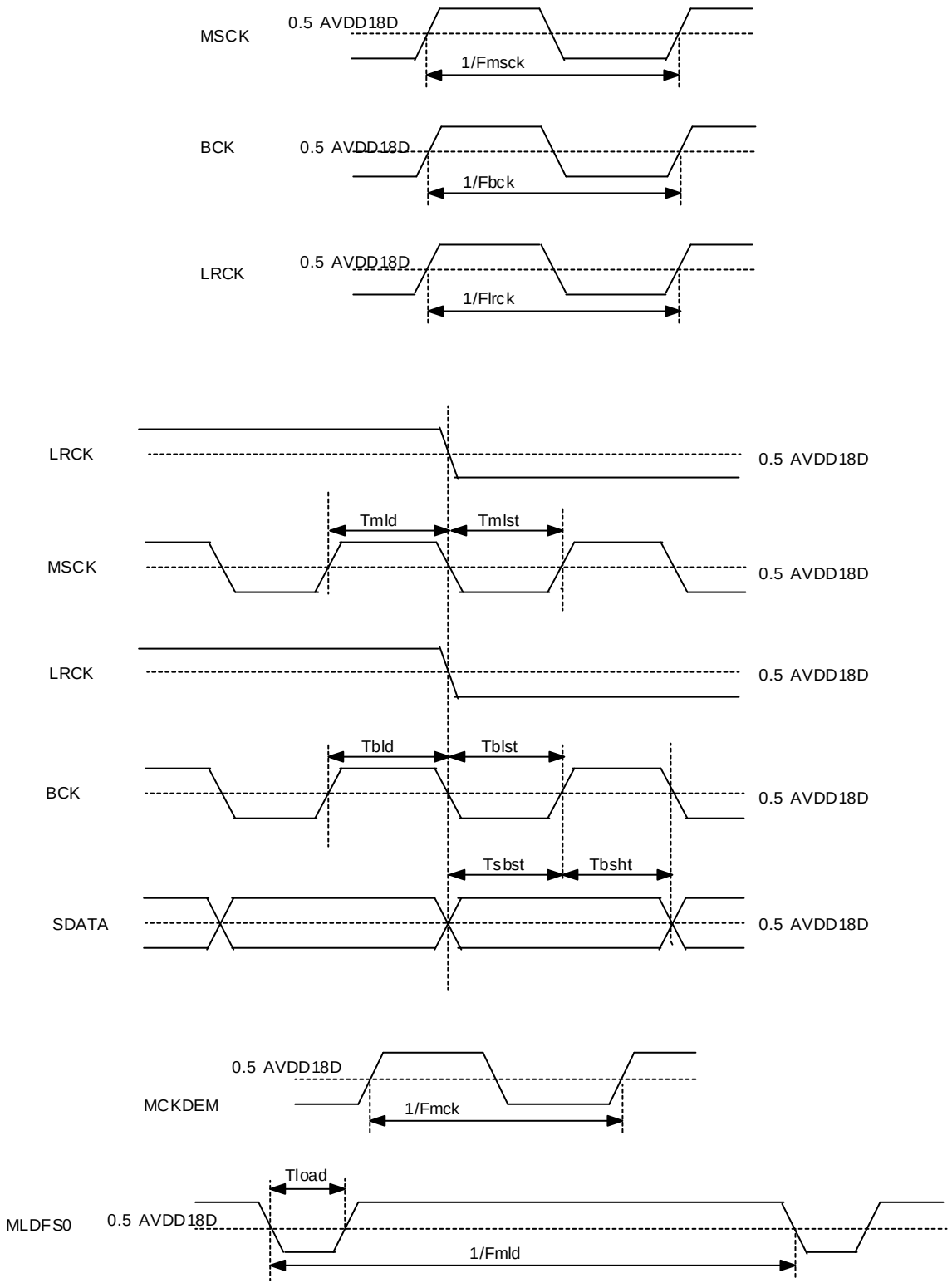


Fig 1. Timing Chart

System Clock Frequency

This Core has a system clock detection circuit which automatically senses if the system clock is operating at 256Fs ~ 768Fs. The system clock for this core must be either 256Fs, 384Fs, 512Fs or 768Fs, where Fs is the audio sampling frequency. The system clock should be synchronized with LRCK clock. LRCK operates at the sampling frequency Fs.

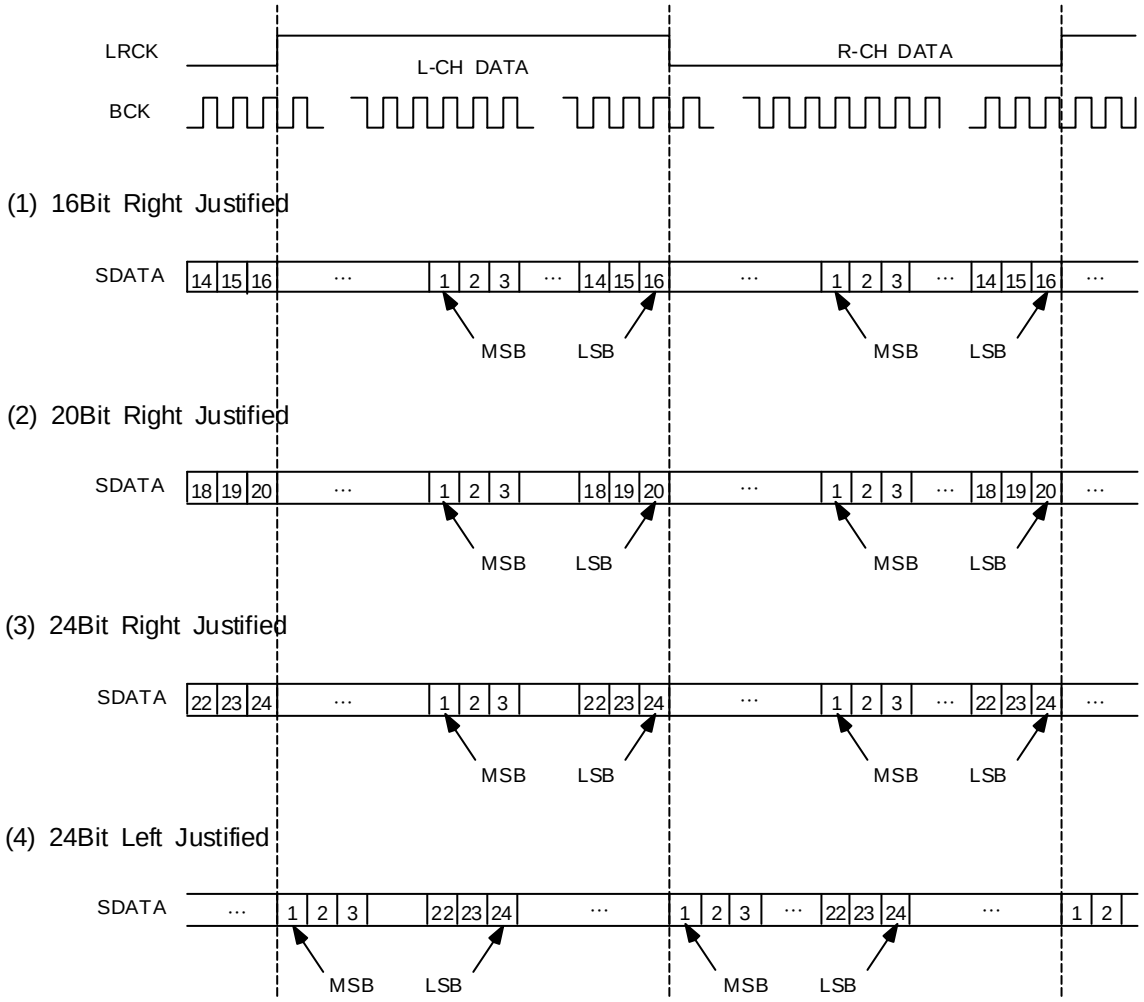
SAMPLING RATE FREQUENCY (Fs:LRCK)	System Clock Frequency				UNIT
	256fs	384fs	512Fs	768Fs	
32KHz	8.1920	12.2880	16.3840	24.5760	MHz
44.1KHz	11.2896	16.9344	22.5792	33.8688	MHz
48KHz	12.2880	18.4320	24.5760	36.8640	MHz

Input Clock and Serial Input Data Inform

DN pin is normal and double mode selection control pin. Refer to the following Table 1 for input clock inform.

	Normal Mode (DN='Low')	Double Mode (DN='High')
LRCK	44.1kHz(=1*Fs)	88.2kHz(=2*Fs)
MSCK(=384Fs)	16.9344MHz(=384*FS)	16.9344MHz(=384*Fs)
BCK	1.4112MHz(=32*Fs)	2.8224MHz(=64*Fs)

Table 1. Input Clock Informs (**Fs=44.1KHz, MSCk=384*Fs,16Bit Input Format Case**)



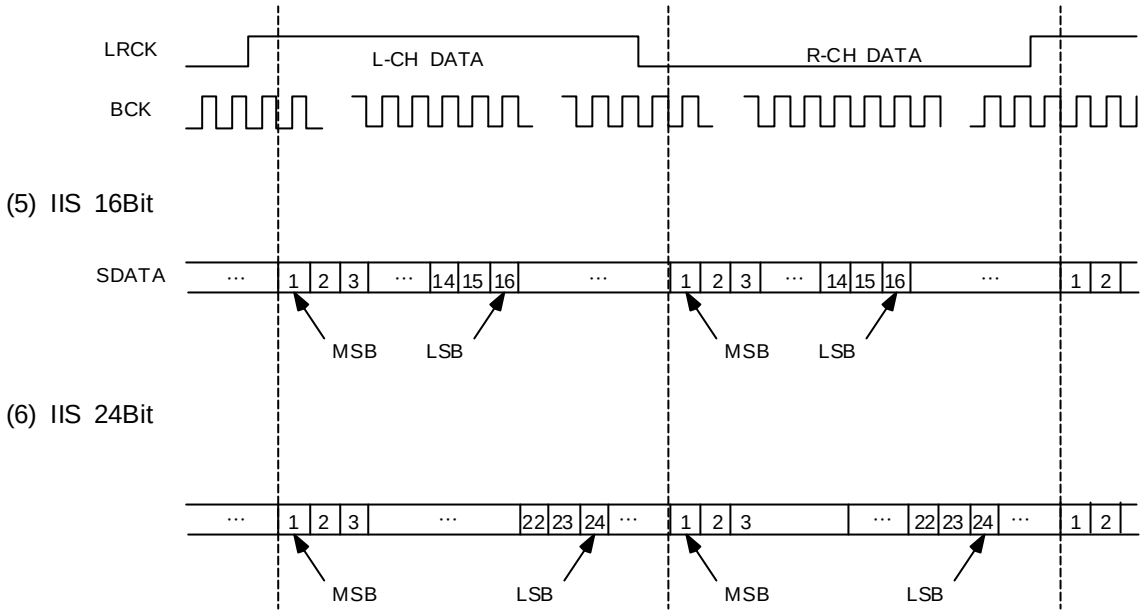


Fig 2. Digital Input Data Format

Digital audio data is interfaced to LRCK, SDATA and BCK Pins. **DAC0415X** can accept both standard, IIS, and left justified data formats. Figure 2 illustrates acceptable input data formats.

Mode Interface & Function Inform

This core can do several built-in functions including digital attenuation, digital de-emphasis, double/normal mode selection, input data format selection, soft mute, zero input detection, and others. These functions can be operated in two different modes, Software mode or Hardware mode. Software Mode is controlled by MCKDEM(MCLK), MDAFS1(MDATA), MLDFS0(MLD) signals from the Mode Interface. Hardware Mode is operated by MCKDEM(DEEM), MDAFS1(SFS1), MLDFS0(SFS0),DN, IIS, IFS, MUTEL, ZDENL pins. This basic operation mode as software or hardware can be selected by MODE Pin as Table shown in Table 2.

MODE = "High"	**Software Mode**
MODE = "Low"	**Hardware Mode**

Table 2. Mode Control

All of the functions shown are selectable within the software mode, but only de-emphasis control, double mode, input data format, soft mute and zero input detection may be selected when using it in the hardware mode.

- Hardware Mode (MODE = "Low")

1) De-Emphasis Control

De-Emphasis control can be selected by DEEM, SFS1 and SFS0 pins.

DEEM	SFS1	SFS0	De-Emphasis
L	X	X	De-Emphasis OFF
H	L	L	De-Emphasis ON (44.1KHz)
H	L	H	De-Emphasis ON (48KHz)
H	H	L	De-Emphasis ON (32KHz)
H	H	H	De-Emphasis ON (44.1KHz)

Table 3. De-Emphasis Control

2) Input Data Format Control

Input data format can be selected by IIS and IFS pins.

IIS	IFS	Data Format
L	L	16Bit Right Justified
L	H	20Bit Right Justified
H	L	IIS 16Bit
H	H	IIS 24Bit

Table 4. Input Data Format Control

3) Double / Normal Mode Control

DN pin is normal and double mode selection control pin.

DN	Function
"Low"	Normal Mode
" High"	Double Mode

Table 5. Double / Normal Mode Control

4) Soft Mute Control

Soft Mute control can be selected by MUTEL pin. Figure3 illustrates Soft Mute operation.

MUTEL	Function
"Low"	Soft mute On
" High:	Soft mute Off

Table 6. Soft Mute Control

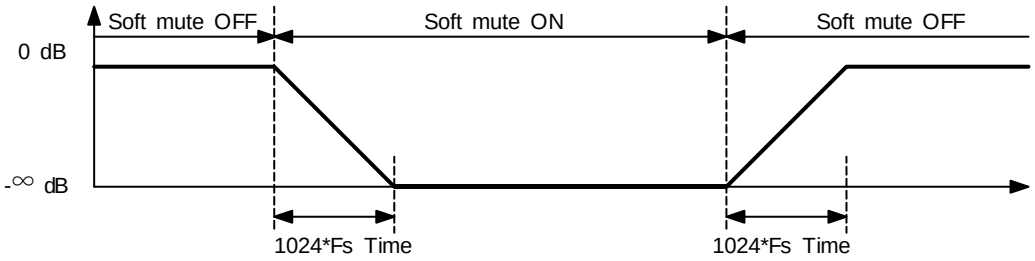


Fig 3. Soft Mute Timing Chart

5) Zero Input Detecton Enable Control

Zero Input Detection Enable control can be selected by ZDENL pin. If the input data has the condition where the lower 4bits of the input data are DC and the remaining upper bits are all "0" or all "1" has continued 8192 cycles of LRCK, Zero input is detected. Zero Input Detection is performed independently for the left and right channels. The Analog Postfilter output will be immediately forced to **VREF.**

ZDENL	Function
"Low"	Zero Input Detection Enable
" High"	Zero Input Detection not Enable

Table 7. Zero Input Detection Enable Control

- Software Mode (MODE = "High")

Software Mode functions are controlled by Mode Interface. When the 16-bit serial data is applied to the MCKDEM, MDAFS1,MLDFS0 pins in the form of Fig4. Software Mode is accomplished. The higher 4bits (MSB First Format-Bin) should be Mode Interface 4bit ID number, the middle 4bits are Address, and according to the lower 8 bits(MSB First Format-Bin) can be adjusted to Data. When RSTB is low state, Software Mode becomes default values. Digital Soft Attenuation (ATTL / ATTR) of Software Mode is attenuated by the same degree that Soft Mute Control does. In case of no Software Mode function needed, MDAFS1 should be "L", MCKDEM and MLDFS0 should be "H".

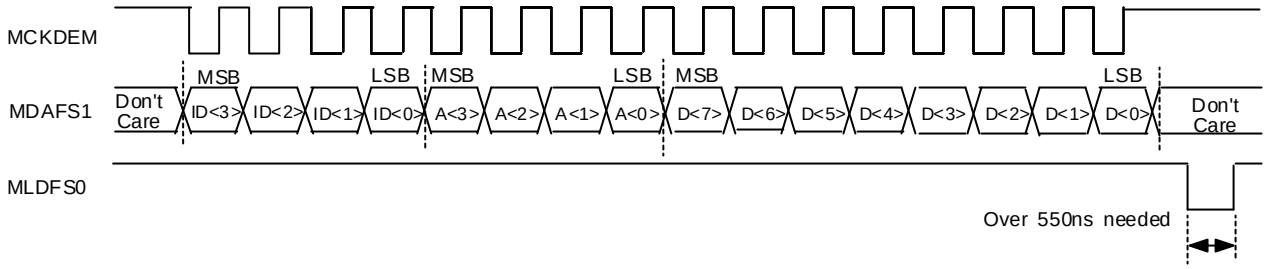


Fig 4. Mode Interface Timing Chart

This section contains information concerning the programmable control registers. Table 8 provides the default reset bar values for each index, and a bit map for each register.

ID NUMBER	ADDRESS	Mnemonic	DEFAULT VALUE	D<7:0>							
ID<3:0>	A<3:0>			7	6	5	4	3	2	1	0
IDNUM<3:0>	0000b	CMDA	00Hex	RES	ZEL	LRP	IIS	IF1	IF0	MON	MLR
IDNUM<3:0>	0001b	CMDB	00Hex	RES	RES	DNS	AIC	MUL	DEM	FS1	FS0
IDNUM<3:0>	0010b	ATTL	00Hex	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
IDNUM<3:0>	0011b	ATTR	00Hex	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Table 8. Mode Interface Register Map

Control Register A									
Address	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0000b	CMDA	RES	ZEL	LRP	IIS	IF1	IF0	MON	MLR

(* : Default value)

RES Reserved.

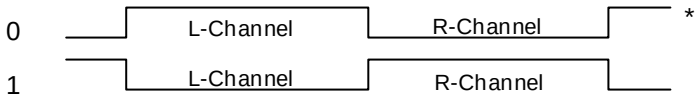
ZEL Zero Input Detection Enable Bar.

0 Zero input detection enable*.

1 Zero input detection disable.

LRP Polarity of LRCK Select.

LRP is used to select the polarity of LRCK. When bit 5 is "Low", left channel data is assumed when LRCK is in a "HIGH" phase and right channel data is assumed when LRCK is in a "LOW" phase. When bit 5 is "HIGH", the polarity assumption is reversed.



IIS Audio Data Format Select.

IIS is used to control the input data format. A "LOW" on bit 4 sets the format to (MSB-first, right-justified format) and a "HIGH" sets the format to IIS.

0 MSB-first, right-justified format.*

1 IIS format.

IF1,IF0 Input Format Select.

IIS	IF1	IF0	Input Data Format
0	0	0	16-Bit Standard (Right-Justified)*
0	0	1	20-Bit Standard (Right-Justified)
0	1	0	24-Bit Standard (Right-Justified)
0	1	1	24-Bit Left-Justified (MSB First)
1	0	0	16-Bit IIs
1	0	1	24-Bit IIS
1	1	0	Reserved
1	1	1	Reserved

MON Mono / Stereo Output Selection.

0 Stereo Output.*

1 Mono Output.

MLR Mono Channel Selection.

When **MON** is "HIGH", this bit is enabled.

0 R-Channel Mono Output.

1 L-Channel Mono Output*.

Control Register B									
Address	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0001b	CMDB	RES	RES	DNS	AIC	MUL	DEM	FS1	FS0

(* : Default value)

RES Reserved.

RES Reserved.

DNS Double / Normal Mode Selection.

0 Normal Mode Operation.*

1 Double Mode Operation.

AIC Individual / Common Attenuation Level Control.

AIC is used as an attenuation control. When this bit is "LOW", the attenuation data on Attenuation Register L is used for both channels, and data in Attenuation Register R is ignored. When this bit is set "HIGH", each channel has separate attenuation data.

0 Common Attenuation Level Control*.

1 Individual Attenuation Level Control.

MUL Soft Mute control.

0 Soft Mute ON.

1 Soft Mute OFF*.

DEM De-Emphasis Enable Control.

0 De-Emphasis OFF*.

1 De-Emphasis ON.

FS1, FS0 De-Emphasis Sampling Frequency Selection

DEM	FS1	FS0	De-Emphasis
0	X	X	De-Emphasis OFF
1	0	0	De-Emphasis ON (44.1KHz)*
1	0	1	De-Emphasis ON (48KHz)
1	1	0	De-Emphasis ON (32KHz)
1	1	1	De-Emphasis ON (44.1KHz)

Attenuation Register L									
Address	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0010b	ATTL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

(* : Default value)

AL7- AL0 L-Channel Attenuation Level Control.

Attenuation Register L is used to left channel attenuation. Bits7-0 (AL7 - AL0) are used determine the attenuation level. The level of attenuation is given by

Attenuation Level = -20 * $\log_{10}$(AL7 - AL0) dB

AL7 - AL0	Attenuation Level
00 Hex	0 dB*
01 Hex	-0.068 dB
02 Hex	-0.102 dB
03 Hex	-0.137 dB
04 Hex	-0.171 dB
…	…
FC Hex	-38.622 dB
FD Hex	42.144 dB
FE Hex	-48.165 dB
FF Hex	-∞ dB

Attenuation Register R									
Address	Mnemonic	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0011b	ATTR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

(* : Default value)

AR7- AR0 R-Channel Attenuation Level Control.

Attenuation Register L is used to left channel attenuation. Bits7-0 (AR7 - AR0) are used determine the attenuation level. The level of attenuation is given by

Attenuation Level = -20 * $\log_{10}$(AR7 - AR0) dB

AR7 - AR0	Attenuation Level
00 Hex	0 dB*
01 Hex	-0.068 dB
02 Hex	-0.102 dB
03 Hex	-0.137 dB
04 Hex	-0.171 dB
…	…
FC Hex	-38.622 dB
FD Hex	42.144 dB
FE Hex	-48.165 dB
FF Hex	-∞ dB

Functional Description

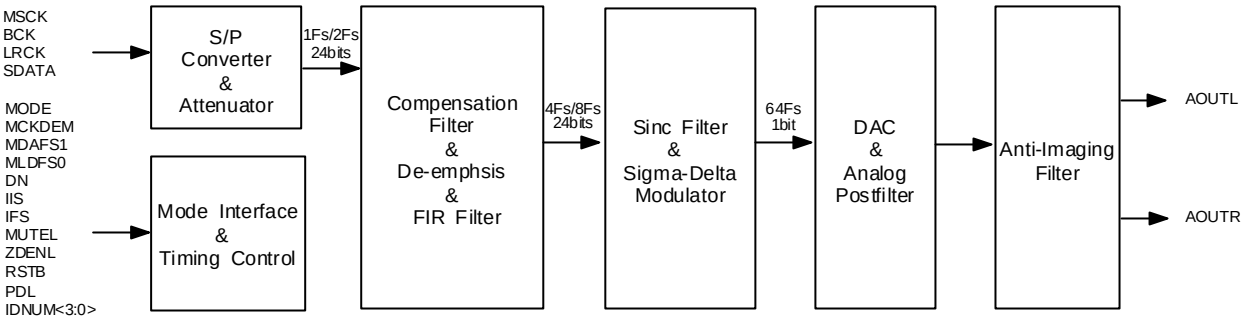


Fig 5. Funtional Block Diagram

Fig 5. is the 1bit 4th order sigma-delta DAC block diagram. S/P Converter converts serial 16/20/24bit input data to parallel 16/20/24bit data. Digital input data is attenuated by MODE interface pin control. Compensation Filter compensates gain droop in Passband by Sinc Filter and Sigma-Dellta Modulator Signal Transfer Function. De-emphasis Block de-emphasizes pre-emphasised input data to emphasize high frequency in audible band. FIR Filter performs 4X interpolation. And it outputs 4Fs(DN="Low") rate data or 8Fs(DN="High") rate data by variable input data rate. It also removes the images of the input signal that are present at multiples of the input sample frequency. And Sinc filter makes the constant 64Fs rate data by 16 times or 8 times up-sampling FIR Filter output data according to DN(Double/Normal Mode) Pin Selection. This operation introduces a sinc function response on the resulting frequency spectrum, which greatly attenuates the energy of images at the multiples of 4Fs(or 8Fs).

Digital sigma-delta modulator of bit-stream type has the IFL (Inverse-Follower-Leader) topology, and it performs a noise-shaping function. The modulator shapes the quantization noise by suppressing its in-band component and pushes the noise energy of outside the band-of-interest without deteriorating the audio input signal. The 64 times oversampled 1-bit PDM outputs from the modulator drives a analog postfilter.

The analog postfilter comprises SC-postfilter, anti-imaging filter. The SC-postfilter removes the quantization noise shaped to out-of-band by digital sigma-delta modulator. This analog filter has the good clock jitter characteristic and very linear characteristic. And following the CTF(continuous time filter) removes the sampling images and makes the high resolution analog output.

Application Circuit

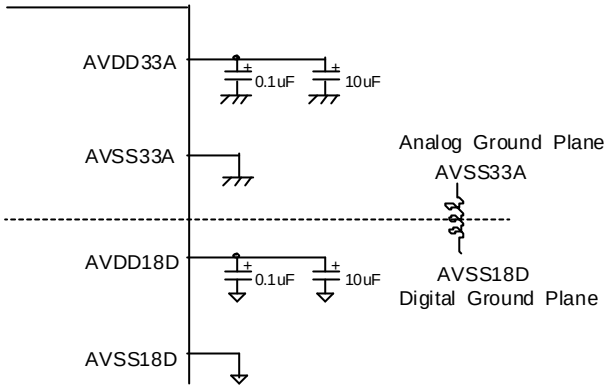


Fig 6. Bypass Capacitor for Power Supply Pins

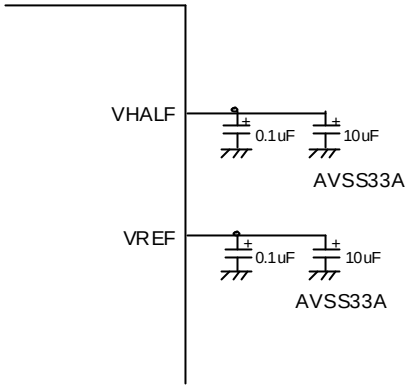


Fig 7. Bypass Capacitors for Reference Pins

Analog pins and digital pins must be separated, Analog pins should be located on the analog ground plane and digital pins should be located on the digital ground plane. Analog ground and digital ground connection is recommended to only one path through ferrite bead like Fig 6. Supply bypass capacitors should be located as close as possible to chip. Small bypass capacitor (0.1uF) should be positioned first to chip than large bypass capacitor (10uF).

Reference (VREF) bypass capacitors (Fig 7.) should be located as close as possible to chip.

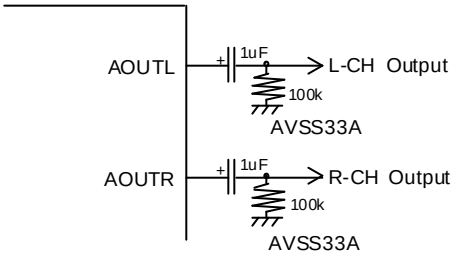


Fig 8. Analog output application

Fig8 is simple high pass filter circuit for analog output. It performs ac-coupling for analog output signal from analog common level to analog ground. Recommended component values are 1uF and 100kΩ

User Guide

- This analog Core Verilog behavioral-modeling will be supplied.

FEEDBACK REQUEST

Sigma-Delta DAC Specification

We appreciate your interest in our products. If you have further questions, please specify in the attached form. Thank you very much.

Parameter	Min	Typ	Max	Unit	Remarks
supply voltage				V	
Max master clock frequency				Hz	
Operating temperature				℃	
Sampling Frequency				Hz	
Dynamic range				dB	
Total harmonic distortion				dB	
Signal-to-noise ratio				dB	
Input format resolution (Serial/Parallel interface)				Bit	
Channel	Mono		Stereo		
Power dissipation				mW	
Full scale output voltage range				Vpp	
group delay				sec	
Phase linearity deviation for passband region				(Deg)	
Peak-to-peak frequency response ripple for passband region				dB	

- Could you explain external/internal pin configurations as required?

- Specially requested function list :

History Card

Version	Date	Modified Items	Comments
Ver 1.0	'00.Sep.	1. Original version published	
Ver 1.1	'01.Mar.	1. I/O pad type changed (Core Pin Description)	
Ver 2.0	'01.Feb	1. Data Sheet Up-date	
Ver3.0	`01.April	1. Data Sheet Up-Date 2. AOUTL,AOUTR GDS Port changed	
Ver4.0	`01.Dec	1. Final Data Sheet	