Eureka Technology

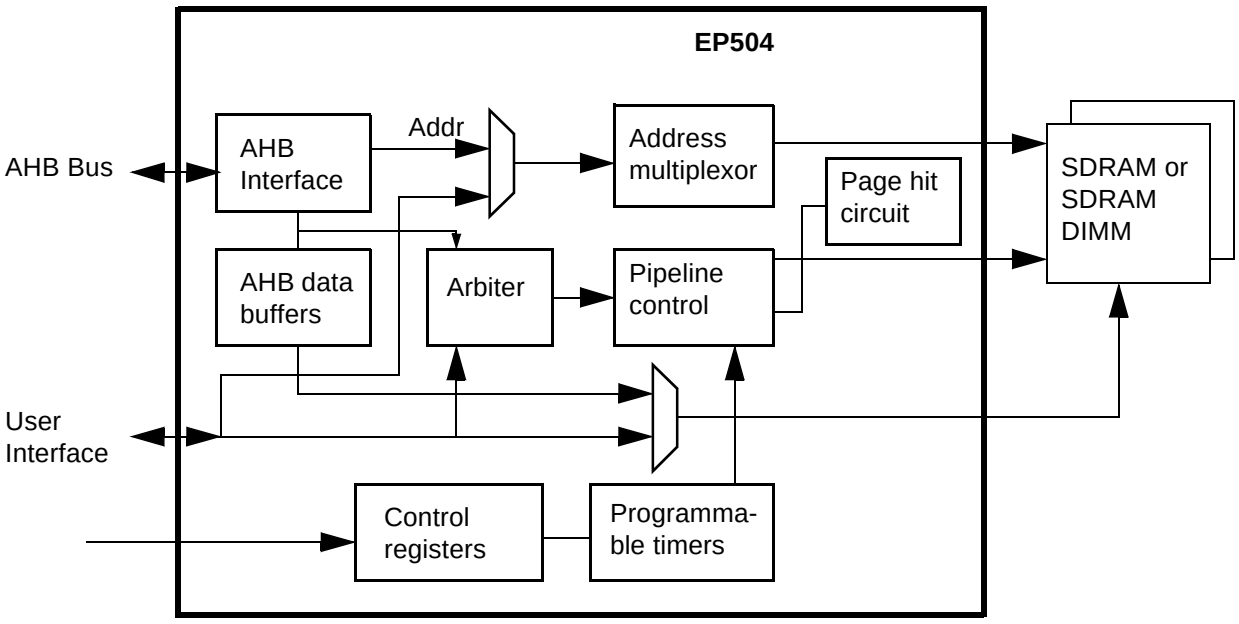
EP504 AHB Bus to SDRAM Controller

Product Summary

FEATURES

- SDRAM controller interfaces directly with AHB Bus and user interface.
- Built-in arbitration between two access ports.
- Second access port allows memory sharing with user logic devices.
- Dual write buffer for simultaneous write posting and SDRAM access.
- Dedicated read buffer with data width matching.
- Early burst termination and CPU master busy on the AHB bus are supported.
- Supports AHB bus data width of 8, 16 and 32 bits.
- Zero wait state burst data transfer on both AHB interface and SDRAM.
- Operates on both discrete SDRAM chips and PC100/133 SDRAM DIMM.
- Supports industrial standard SDRAM from 64Mbit to 256Mbit device sizes.
- Pipeline access allows continuous data transfer without wasted cycle.
- Fast page access on row address matching.
- Independent row address matching for each of the 4 SDRAM banks.
- Programmable memory size: 4, 8, 16 and 32 bits per SDRAM.
- Programmable SDRAM access timing parameters.
- Automatic refresh generation with programmable refresh intervals.
- Optimized for ASIC and PLD implementations, including Excalibur PLD.

BLOCK DIAGRAM



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DESCRIPTIONS

The AHB bus SDRAM controller provides high speed SDRAM for the system. It features two access ports. One port interfaces directly to the AHB bus and the other access port is optimized for system core logic such as DMA or PCI bus bridge.

The EP504 SDRAM controller contains built-in arbitration unit to allow both the AHB CPU and system core logic to share SDRAM access. Rotating priority scheme ensures equal sharing of the memory bandwidth.

The SDRAM controller is a high performance SDRAM controller designed for transferring data to and from any industry standard SDRAMs or PC100/133 SDRAM DIMMs at the highest possible data rate.

The pipeline feature of the SDRAM controller allows the user port to specify the next access address while the current data transfer is in progress. Multiple data transfers can be cascaded together to read or write data from the SDRAM continuously, without any wasted cycle between accesses.

Another performance enhancement features of the SDRAM controller is that it uses fast page access whether there is a row hit. For each of the four internal banks, the SDRAM controller keeps the previous accessed row open. If the new request hits the same row, a column access is performance thus eliminate row access time. The SDRAM controller simultaneously keeps track of four open rows, one for each bank.

The SDRAM controller can be programmed to support different sizes and configurations of SDRAMs. The SDRAM device sizes supported are 64Mbits, 128Mbits, and 256Mbits. The data width per SDRAM device can be programmed to 4, 8, 16 or 32 bits. The user can use multiple SDRAMs to build an wider memory subsystems.

The SDRAM controller is fully programmable. All access timing parameters such as CAS latency, row-to-column delay, refresh interval, etc., are programmable to support different speed grades of SDRAM devices and different operating frequencies. All the timing parameters can be modified during run-time by a separate access port. The timing parameters can also be set to the proper default values during compile time so that there is no need to program them during run-time.

The user interface of the SDRAM controller is a user-friendly synchronous bus, similar to the I960 microprocessor interface. The user provides the address for each access and the SDRAM controller automatically generate the row (RAS) and column (CAS) access cycles to transfer data. The user can specify single or burst data transfer. In burst data transfer, zero wait state data bursting is supported to maximize memory bandwidth. SDRAM refresh cycle is periodically issued by the SDRAM controller. The refresh cycles are transparent to the AHB bus or the user interface.

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