

Power Management LSI Series for Automotive Body Control

Regulators with Voltage Detector and Watchdog Timer

BD3004HFP, BD3005HFP



●Description

The BD3004HFP, BD3005HFP low bias current regulator and watchdog timer features a high 50 V breakdown voltage and is compatible with on-board vehicle microcontrollers. It offers an output current of 500 mA while limiting bias current to 80 μ A (Typ.). The series supports the use of ceramic capacitors as output phase compensation capacitors. The reset detection voltage can be changed by connecting a resistor to the Vs pin. (BD3004HFP) The watchdog timer can be switched on and off using the INH pin input logic. (BD3005HFP)

●Features

- 1) 5 V/500 mA regulators for microcontrollers
 BD3004HFP: Adjustable detection voltage (Vs pin)
 BD3005HFP: Built-in watchdog timer reset circuit (INH pin: watchdog timer on/off)
- 2) Super-low bias current: 80 μ A (Typ.)
- 3) Low-saturation voltage type P-channel DMOS output transistors
- 4) High precision output voltage: 5 V \pm 2%
- 5) Low-ESR ceramic capacitors can be used as output capacitors
- 6) Vcc Maximum applied voltage: 50 V
- 7) Built-in overcurrent protection circuit and thermal shutdown circuit
- 8) Built-in reverse connection breakdown prevention circuit
- 9) Back current flow protection during sudden battery failures, making it a highly reliable 5 V regulator.
- 10) HRP7 package

●Applications

Onboard devices (Vehicle equipment, Car stereos, Satellite navigation systems, etc.)

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Vcc applied voltage	Vcc	-15 to +50 ^{*1}	V
Vs pin voltage (BD3004HFP)	Vs	-0.3 to +15	V
INH pin voltage (BD3005HFP)	VINH	-0.3 to +15	V
Regulator output pin voltage	VOUT	-0.3 to +15	V
Reset output pin voltage	VRO	-0.3 to +15	V
Watchdog input pin voltage	VCLK	-0.3 to +15	V
Reset delay setting pin voltage	VCT	-0.3 to +15	V
Output current	IOUT	500	mA
Power dissipation	Pd	1.6 ^{*2}	W
Operating temperature range	Topr	-40 to +125	°C
Storage temperature range	Tstg	-55 to +150	°C
Maximum junction temperature	Tjmax	150	°C

*1 Must not exceed Pd.

*2 Reduced by 12.8 mW/°C over 25°C, when mounted on a glass epoxy board (70 mm \times 70 mm \times 1.6 mm).

●Operating power supply voltage range (Ta = 25°C)

Parameter	Min.	Max.	Unit
Operating power supply voltage range	5.5*	36**	V
Output current	—	500	mA

* For the output voltage, consider the voltage drop (min. I/O voltage differential) due to the output current.

** Must not exceed Pd.

●Electrical Characteristics (Unless otherwise specified, Ta = -40°C to 125°C, Vcc = 13.5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Overall]						
Total supply current 1	Icc1	—	80	130	μA	Io=0mA
Total supply current 2	Icc2	—	80	130	μA	Io=200mA
Total supply current 3(BD3005HFP)	Icc3	—	80	130	μA	VINH=0V
[Regulator]						
Output voltage	VOUT	4.90	5.00	5.10	V	
Input stability	Line.Reg	—	10	20	mV	Vcc=6.2~25 V
Load stability	Load.Reg	—	15	30	mV	Io=5~200mA
Min. I/O voltage differential	ΔVd	—	0.78	1.1	V	Vcc=4.75 V, Io=200mA
Output current	IOUT	500	—	—	mA	VOUT=4.9V
Ripple rejection	R.R.	45	55	—	dB	f=120Hz, ein=1Vrms, Io=200mA
[Reset]						
Detection voltage(BD3004HFP)	Vdet	4.02	4.10	4.18	V	
Detection voltage(BD3005HFP)	Vdet	4.40	4.50	4.60	V	
Hysteresis width	VHS	50	100	150	mV	
Output delay time Low → High	TdLH	12	21	40	mS	CT=0.1μF ^{*1}
Low output voltage	VRST	—	0.2	0.5	V	IRST=2mA
Min. operating voltage	VOPL	1.0	—	—	V	
[Watchdog timer]						
High-side switching threshold voltage	VthH	1.16	1.26	1.36	V	
Low-side switching threshold voltage	VthL	0.20	0.24	0.28	V	
Discharge current	Ictc	1	2	3	μA	
Charge current	Icto	3	6	10	μA	
Watchdog monitor time	TWH	32	51	90	mS	CT=0.1μF ^{*2}
Watchdog reset time	TWL	10	17	30	mS	CT=0.1μF ^{*3}
Clock input pulse width	TWCLK	500	—	—	nS	
[INH]						
WDT off voltage(BD3005HFP)	VUINH	3.2	—	8.0	V	
WDT on voltage(BD3005HFP)	VLINH	0	—	1.8	V	

*1 TdLH can be varied by changing the CT capacitance value.

$$TdLH (s) \approx (1.26 \times CT (\mu F)) / Icto (\mu A) \text{ (Calculation uses Typ. values)}$$

*2 TWH can be varied by changing the CT capacitance value.

$$TWH (s) \approx (1.02 \times CT (\mu F)) / Ictc (\mu A) \text{ (Calculation uses Typ. values)}$$

*3 TWL can be varied by changing the CT capacitance value.

$$TWL (s) \approx (1.02 \times CT (\mu F)) / Icto (\mu A) \text{ (Calculation uses Typ. values)}$$

Note: This IC is not designed to be radiation-resistant.

●Reference data (Unless otherwise specified, Ta = 25°C)

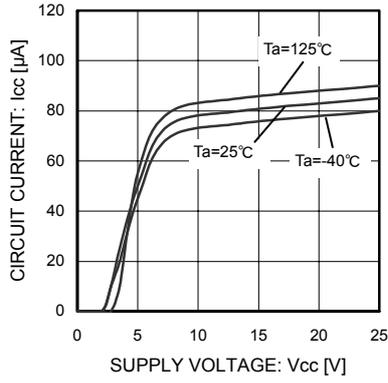


Fig. 1 Circuit Current

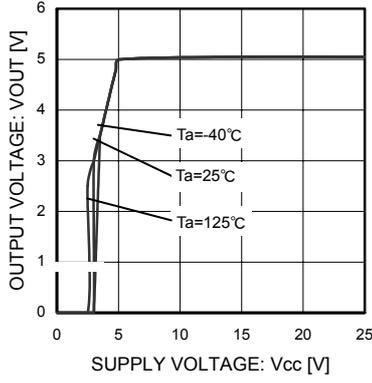


Fig. 2 Output Voltage vs Supply Voltage

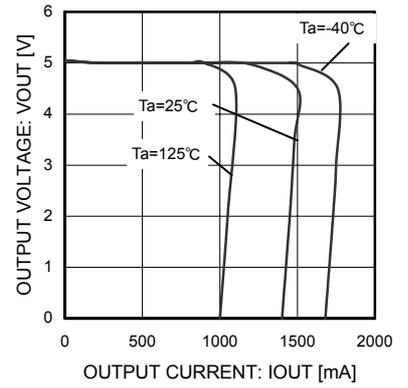


Fig. 3 Output Voltage vs Load

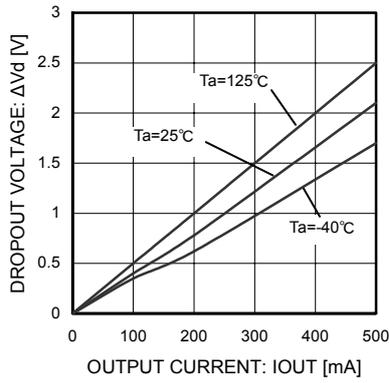


Fig. 4 I/O Voltage Difference

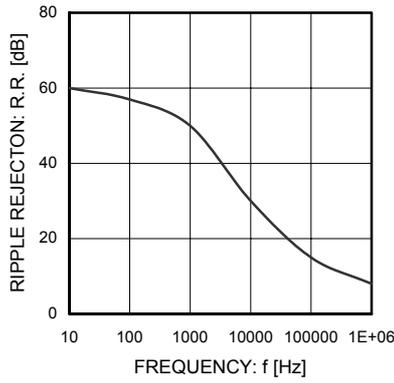


Fig. 5 Ripple Rejection

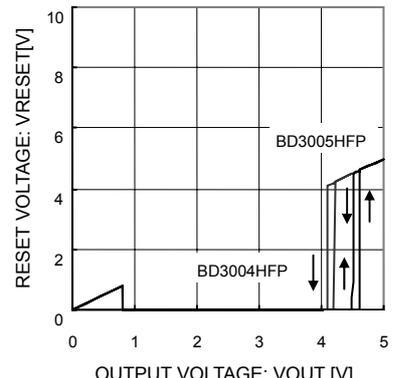


Fig. 6 Reset Detection Voltage

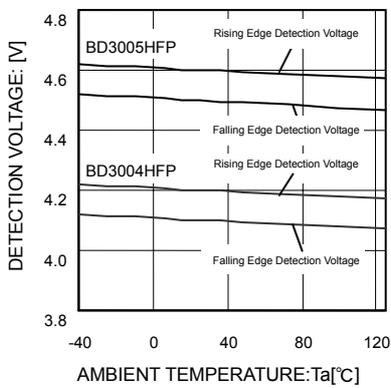


Fig. 7 Reset Detection Voltage Temperature

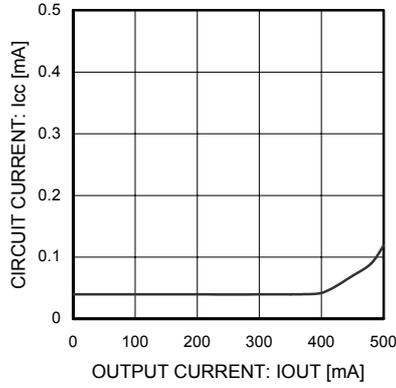


Fig. 8 Total Supply Current Classified by Load

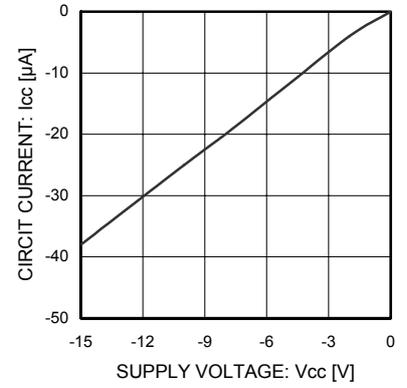


Fig. 9 Back Current

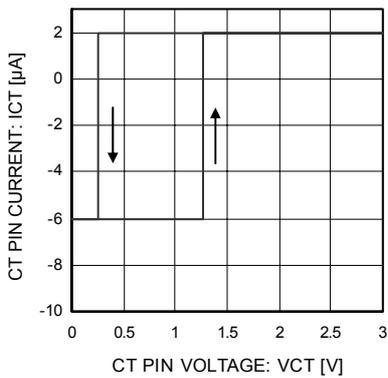


Fig. 10 CT Pin Charge vs Discharge Current

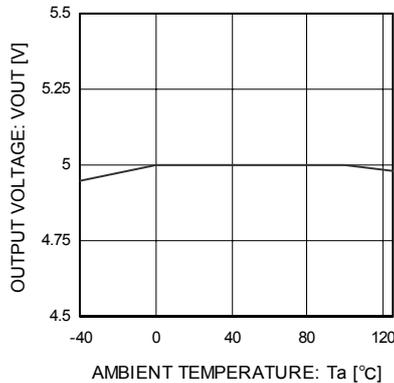


Fig. 11 Output Voltage vs Temperature

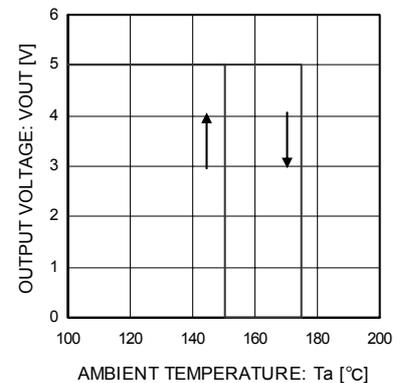


Fig. 12 Thermal Shutdown Circuit

●Block diagram

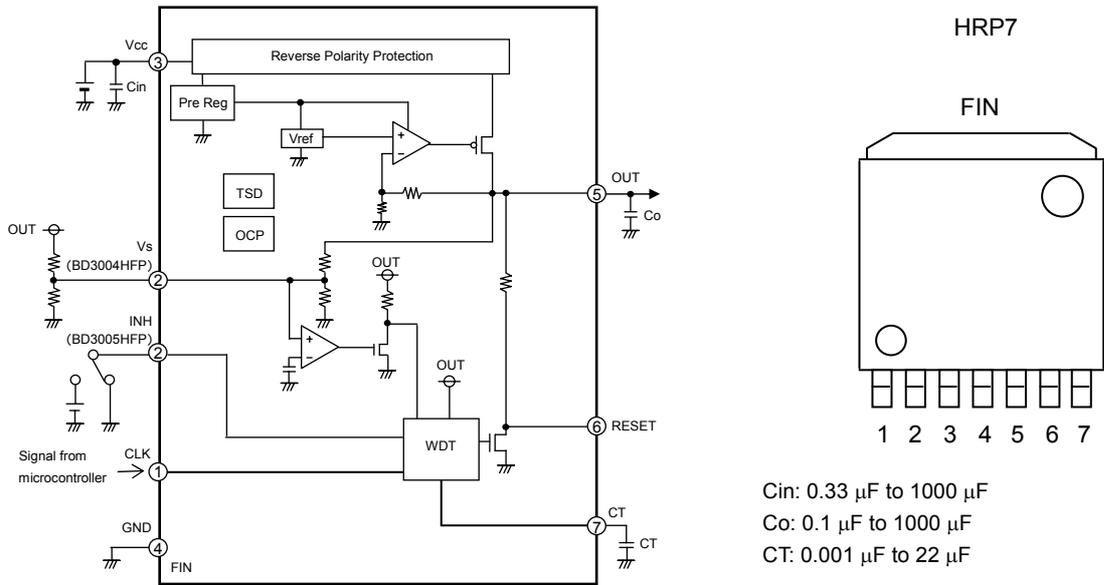


Fig.13

●Pin descriptions

Pin. No	Pin name	Function
1	CLK	Clock input from microcontroller
2	Vs(BD3004HFP)	Reset detection voltage adjustment function pin
	INH(BD3005HFP)	WDT on/off function pin (WDT off when INH = high; WDT on when INH = low)
3	Vcc	Power supply pin
4	GND	GND pin
5	OUT	Voltage output pin
6	RESET	Reset output pin
7	CT	Reset output delay time, WDT monitor time setting external capacitance connection pin
FIN	GND	GND pin

●I/O Circuit diagram

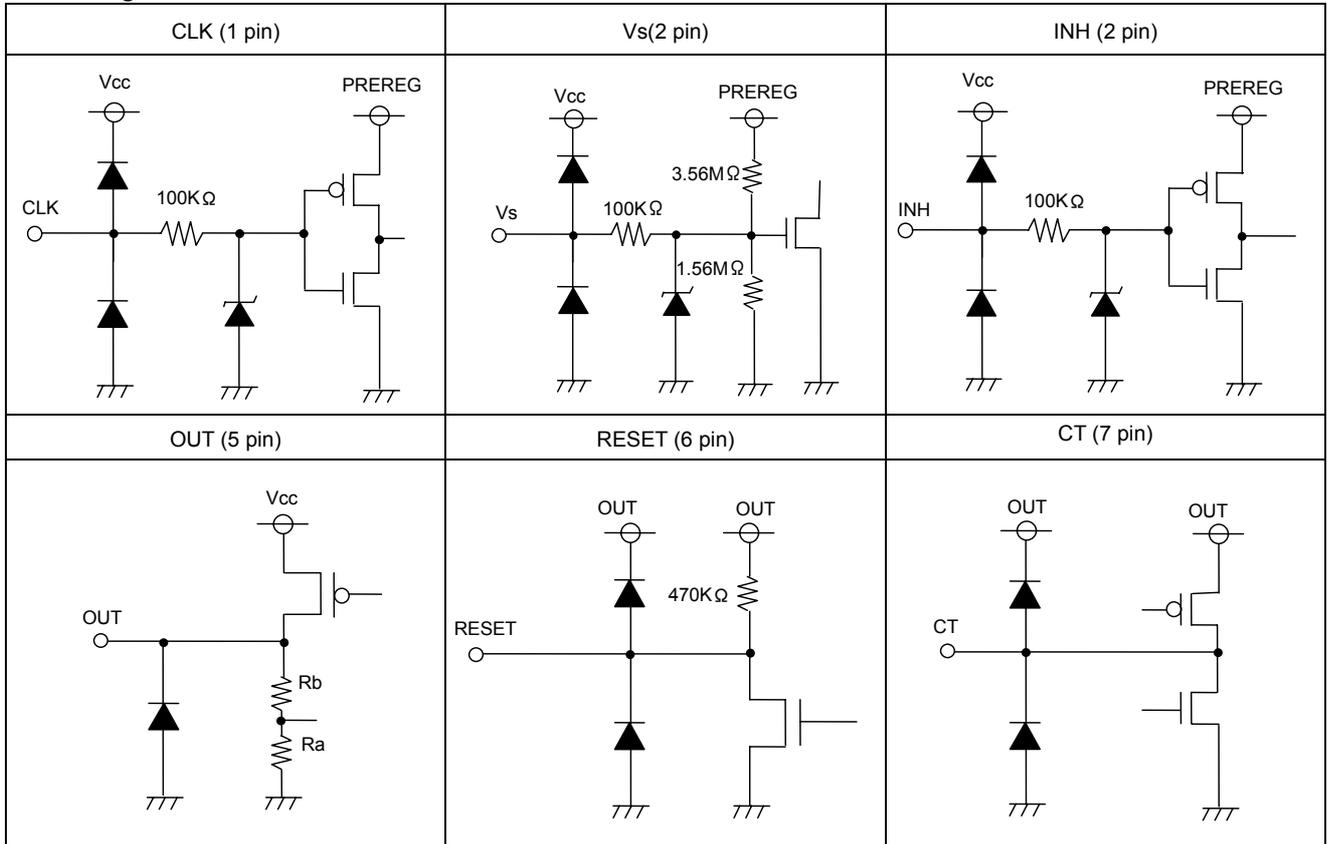
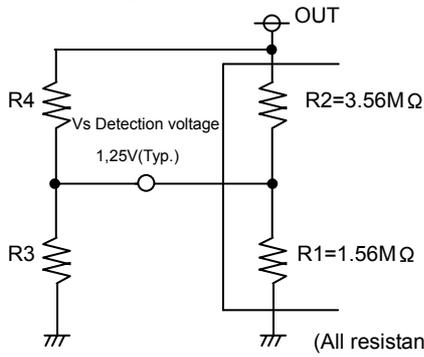


Fig.14

* All resistance values are typical ones.

● Detection voltage adjustment



For a basic detection voltage of 4.1 V,
 $V_{det} = V_s \times (R_1 + R_2 / R_1)$

To change the detection voltage,
 insert pull-down resistor R3 (with a resistance value lower than R1)
 between the Vs and GND pins, and pull-up resistor R4 (with a
 resistance value lower than R2) between the Vs and Vo pins.

$$V_{det} = V_s \times (R_3 + R_4 / R_3) \quad [R_3 \ll R_1, R_4 \ll R_2]$$

(All resistance values are typical ones.)

Fig.15

● Timing chart

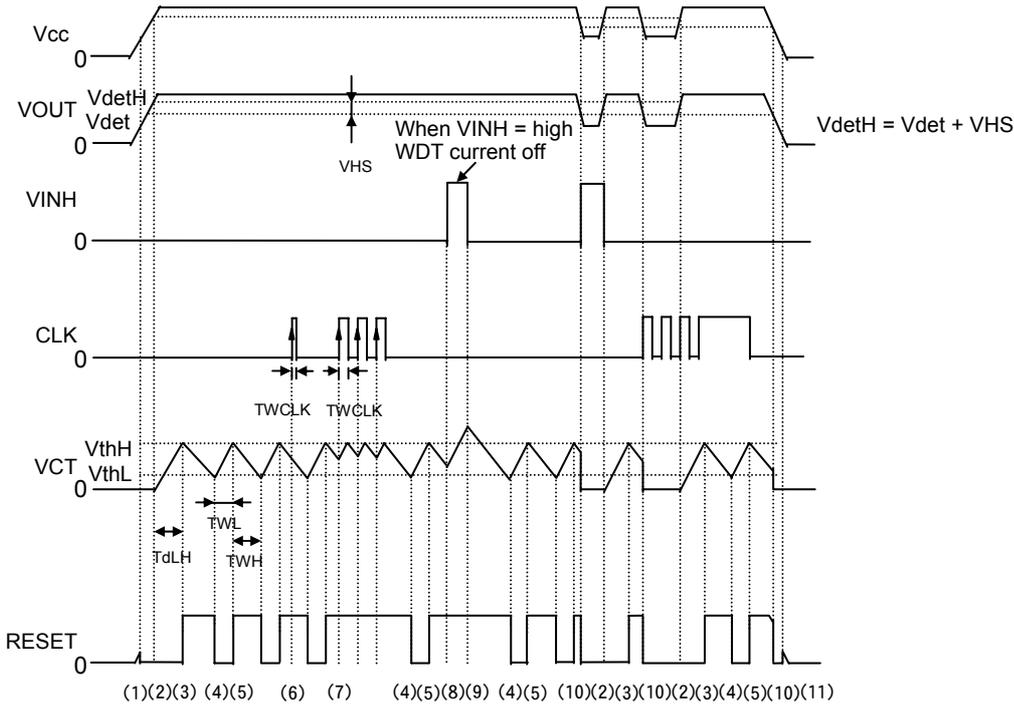


Fig.16

● Explanation

- (1) When the output voltage (VOUT) reaches 1.0 V, the reset pin voltage (RESET) will switch to low level.
- (2) When VOUT reaches or exceeds the reset clear voltage (VdetH), the external capacitor connected to the CT pin will begin to charge. When the CT pin voltage (VCT) reaches the upper switching threshold voltage (VthH), RESET will maintain a low-level signal. When VCT reaches the VthH voltage, RESET will switch from low to high level. The time from VCT reaching or exceeding the VdetH voltage until RESET reverses (the RESET transmission delay time: TdLH) is given by the following equation:
 $T_{dLH} (s) \approx (1.26 \times CT (\mu F)) / I_{cto} (\mu A) \dots [1]$
- (3) The watchdog timer operates when RESET rises.
- (4) When VCT reaches the lower switching threshold voltage (VthL), the CT pin switches from discharging to charging, and RESET switches from high level to low level. The watchdog timer reset time TWL is given by the following equation:
 $T_{WL}(s) \approx (1.02 \times CT (\mu F)) / I_{ctc} (\mu A) \dots [2]$
- (5) The CT pin state switches from charge to discharge when VCT reaches VthH, and RESET switches from low to high. The watchdog timer monitor time TWH is given by the following equation:
 $T_{WH}(s) \approx (1.02 \times CT (\mu F)) / I_{ctc} (\mu A) \dots [3]$
- (6) The CT pin state may not switch from charge to discharge when the CLK input pulse width (TWCLK) is short. Use a TWCLK input pulse width of at least 500 ns.
- (7) When a pulse (positive edge trigger) of at least 500 ns is input to the CLK pin while the CT pin is discharging, VCT switches from discharging to charging and then switches back to discharging once it charges to VthH.
- (8) Watchdog timer operation is forced off when the INH pin switches to high. At that time, only the watchdog timer will be turned off, and reset detection will operate normally.
- (9) The watchdog timer function turns on when the INH pin switches to low. At that time, the external capacitor on the CT pin will be discharged.
- (10) RESET switches from high to low when OUT falls to the RESET detection voltage (VDET) or lower.
- (11) When VOUT falls to 0 V, the RESET signal stays low until VOUT reaches 1.0 V

●Setting of heat

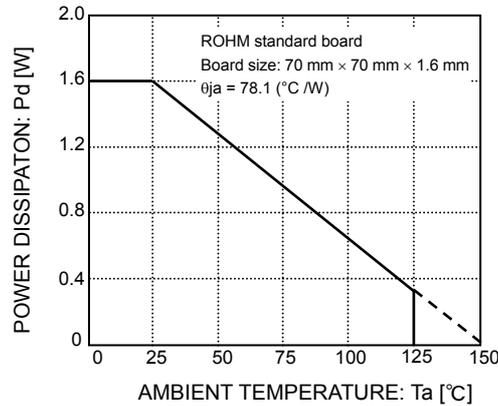


Fig.17

Refer to the dissipation reduction illustrated in Fig.17 when using the IC in an environment where $T_a \geq 25^\circ\text{C}$. The characteristics of the IC are greatly influenced by the operating temperature. If the temperature exceeds the maximum junction temperature T_{jmax} , the elements of the IC may be damaged. It is necessary to give sufficient consideration to the heat of the IC in view of two points, i.e., the protection of the IC from instantaneous damage and the maintenance of the reliability of the IC in long-time operation.

In order to protect the IC from thermal destruction, the operating temperature of the IC must not exceed the maximum junction temperature T_{jmax} . Fig.17 illustrates the power dissipation/heat mitigation characteristics for the HRP-7 package. Always operate the IC within the power dissipation (P_d). The following method is used to calculate the power consumption P_c (W).

$$P_c = (V_{cc} - V_{OUT}) \times I_{OUT} + V_{cc} \times I_{cc}$$

$$\text{Power dissipation } P_d \leq P_c$$

- V_{cc} : Input voltage
- V_{OUT} : Output voltage
- I_{OUT} : Load current
- I_{cc} : Total supply current

The load current I_o is obtained to operate the IC within the power dissipation.

$$I_{OUT} \leq \frac{P_d - V_{cc} \times I_{cc}}{V_{cc} - V_{OUT}} \quad \text{For } I_{cc}, \text{ see Fig. 1.}$$

From the above, the maximum load current I_{OUTmax} for the applied voltage V_{cc} can be calculated during the thermal design process.

Calculation example

Example: at $T_a = 85^\circ\text{C}$, $V_{cc} = 12\text{ V}$, $V_{OUT} = 5\text{ V}$

$$I_{OUT} \leq \frac{0.832 - 12 \times I_{cc}}{12 - 5}$$

$$I_{OUT} \leq 118\text{ mA} \quad (I_{cc} = 80\text{ }\mu\text{A})$$

$\theta_{ja} = 78.1^\circ\text{C/W} \rightarrow -12.8\text{ mW}/^\circ\text{C}$
 $25^\circ\text{C} = 1.6\text{ W} \rightarrow 85^\circ\text{C} = 0.832\text{ mW}$

Make a thermal calculation in consideration of the above equations so that the whole operating temperature range will be within the power dissipation. The power consumption P_c of the IC, in the event of shorting (i.e., if the V_o and GND pins are shorted), will be obtained from the following equation:

$$P_c = V_{cc} \times (I_{cc} + I_{short}) \quad I_{short} = \text{Short current}$$

●External settings for pins and precautions

1) V_{cc} pin

Insert capacitors with a capacitance of $0.33\text{ }\mu\text{F}$ to $1,000\text{ }\mu\text{F}$ between the V_{cc} and GND pins. The capacitance varies with the application. Be sure to design the capacitance with a sufficient margin.

2) Output pin

Capacitors for stopping oscillation must be placed between each output pin and the GND pin. Capacitor capacitance values can be used in a range between $0.1\text{ }\mu\text{F}$ and $1,000\text{ }\mu\text{F}$. Since oscillation does not occur even for ESR values from $0.001\text{ }\Omega$ to $100\text{ }\Omega$, a ceramic capacitor can be used. Abrupt input voltage and load fluctuations can affect output voltages. Output capacitor capacitance values should be determined after sufficient testing of the actual application

3) CT pin

Be sure to connect a capacitor to the CT pin. The reset output delay time is given by equation (1) on P. 5. The WDT time is given by equations (2) and (3) on P.5. The setting times are proportional to the capacitance value of CT pin from the equations, so the maximum and minimum setting times can be calculated from the electrical characteristics according to the capacitance. Note however that the electrical characteristics do not include the external capacitor's temperature characteristics. The recommended connection capacity for the CT pin is $0.001\text{ }\mu\text{F}$ to $22\text{ }\mu\text{F}$.

● **Operation Notes**

1. **Absolute maximum ratings**
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.
2. **GND voltage**
The potential of GND pin must be minimum potential in all operating conditions.
3. **Thermal design**
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
4. **Inter-pin shorts and mounting errors**
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.
5. **Actions in strong electromagnetic field**
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.
6. **Testing on application boards**
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

7. **Regarding input pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

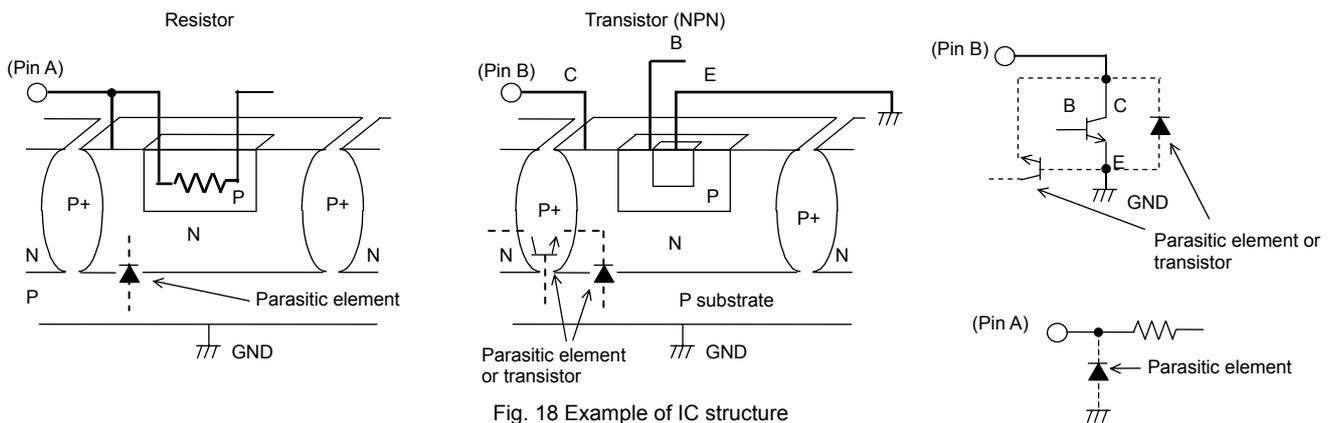
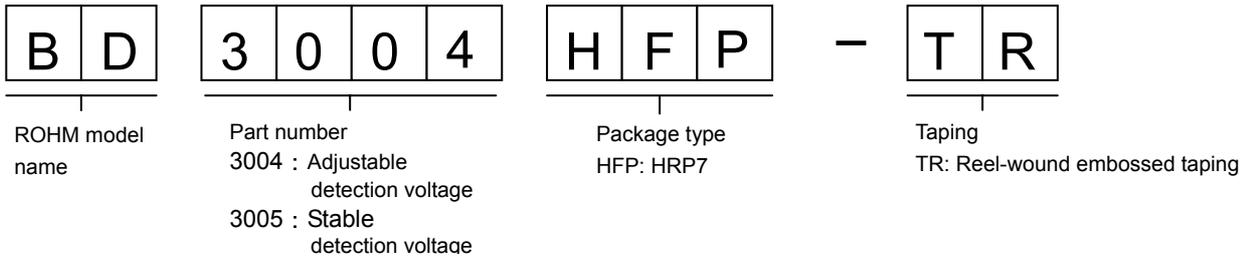


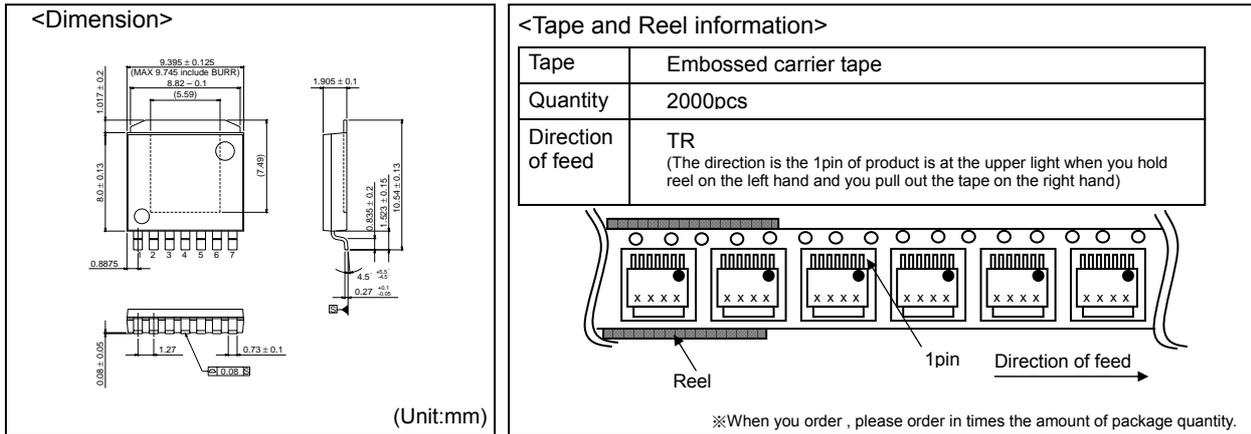
Fig. 18 Example of IC structure

8. **Ground Wiring Pattern**
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
9. **Thermal shutdown circuit (TSD)**
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.. (See Fig. 12)
10. **Overcurrent protection circuit (OCP)**
The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures. (See Fig. 3)
11. **Negative surge application to Vcc pin**
The IC incorporates a built-in reverse connection breakdown prevention circuit that prevents IC damage even if Vcc carries a lower voltage than the GND pin. However, note that the absolute maximum rating for the negative power supply voltage is -15 V.
12. **Back current flow when the Vcc power supply is suddenly interrupted**
These ICs limit generation of back current flow when the Vcc power supply is suddenly interrupted to protect the IC from damage. Sinking current is also limited, making the series compatible with designs where high-capacitance capacitors are used to lengthen the amount of time over which the output voltage can be maintained.

●Selecting a model name when ordering



HRP7



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