



# Low Cost, Dual, High Current Output Line Driver with Shutdown

## ADA4311-1

### FEATURES

#### High speed

–3 dB bandwidth: 310 MHz,  $G = +5$ ,  $R_{LOAD} = 50 \Omega$

Slew rate: 1050 V/ $\mu$ s,  $R_{LOAD} = 50 \Omega$

#### Wide output swing

20.6 V p-p differential,  $R_{LOAD}$  of 100  $\Omega$  from 12 V supply

#### High output current

#### Low distortion

–98 dBc typical at 1 MHz,  $V_{OUT} = 2$  V p-p,  $G = +5$ ,  $R_{LOAD} = 100 \Omega$

–72 dBc typical at 10 MHz,  $V_{OUT} = 2$  V p-p,  $G = +5$ ,  $R_{LOAD} = 100 \Omega$

#### Power management and shutdown

Control inputs CMOS level compatible

Shutdown quiescent current: 1 mA/amplifier

Selectable quiescent current: 1 mA to 11.8 mA/amplifier

### APPLICATIONS

Home networking line drivers

Twisted pair line drivers

Power line communications (PLC)

Video line drivers

ARB line drivers

I/Q channel amplifiers

### GENERAL DESCRIPTION

The ADA4311-1 is comprised of two high speed, current feedback operational amplifiers. The high output current, high bandwidth, and fast slew rate make it an excellent choice for broadband applications requiring high linearity performance while driving low impedance loads.

The ADA4311-1 incorporates a power management function that provides shutdown capabilities and the ability to optimize the quiescent current of the amplifiers. The CMOS-compatible, power-down control pins (PD1 and PD0) enable the ADA4311-1 to operate in four different modes: full power, medium power, low power, and complete power-down. In power-down mode, the quiescent current drops to only 1.0 mA/amplifier, while the outputs go to a high impedance state.

### PIN CONFIGURATION

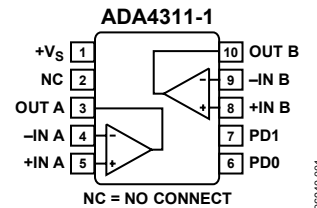


Figure 1. Thermally Enhanced, 10-Lead MINI\_SO\_EP

### TYPICAL APPLICATION

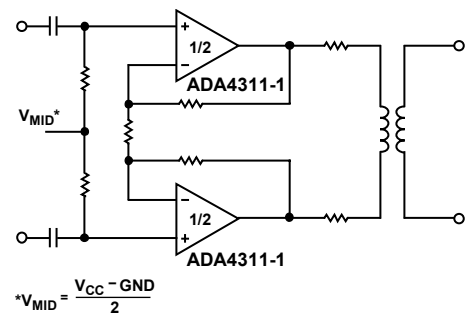


Figure 2. Typical PLC Driver Application

The ADA4311-1 is available in a thermally enhanced, 10-lead MSOP with an exposed paddle for improved thermal conduction. The ADA4311-1 is rated to work in the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

#### Rev. 0

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## REVISION HISTORY

8/07—Revision 0: Initial Version

## SPECIFICATIONS

$V_S = 12\text{ V}$ ,  $R_F = 499\ \Omega$  (@  $T_A = 25^\circ\text{C}$ ,  $G = +5$ ,  $R_L = 100\ \Omega$  to  $V_S/2$ ), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
–3 dB Bandwidth	$V_{OUT} = 0.1\text{ V p-p}$ , PD1 = 0, PD0 = 0, $R_{LOAD} = 50\ \Omega$		310		MHz
	$V_{OUT} = 0.1\text{ V p-p}$ , PD1 = 0, PD0 = 1, $R_{LOAD} = 50\ \Omega$		220		MHz
	$V_{OUT} = 0.1\text{ V p-p}$ , PD1 = 1, PD0 = 0, $R_{LOAD} = 50\ \Omega$		140		MHz
	$V_{OUT} = 10.2\text{ V p-p}$ , PD1 = 0, PD0 = 0, $R_{LOAD} = 50\ \Omega$		12.9		MHz
Full Power Bandwidth	$V_{OUT} = 2\text{ V p-p}$ , PD1 = 0, PD0 = 0		1050		V/ $\mu\text{s}$
Slew Rate	$V_{OUT} = 2\text{ V p-p}$ , PD1 = 0, PD0 = 1		1050		V/ $\mu\text{s}$
	$V_{OUT} = 2\text{ V p-p}$ , PD1 = 1, PD0 = 0		1000		V/ $\mu\text{s}$
<b>NOISE/DISTORTION PERFORMANCE</b>					
Differential Distortion (Worst Harmonic)	$f_C = 1\text{ MHz}$ , $V_{OUT} = 2\text{ V p-p}$				
	PD1 = 0, PD0 = 0		–98		dBc
	PD1 = 0, PD0 = 1		–95		dBc
	PD1 = 1, PD0 = 0		–86		dBc
	$f_C = 10\text{ MHz}$ , $V_{OUT} = 2\text{ V p-p}$				
	PD1 = 0, PD0 = 0		–72		dBc
	PD1 = 0, PD0 = 1		–63		dBc
	PD1 = 1, PD0 = 0		–52		dBc
	$f_C = 20\text{ MHz}$ , $V_{OUT} = 2\text{ V p-p}$				
	PD1 = 0, PD0 = 0		–56		dBc
	PD1 = 0, PD0 = 1		–49		dBc
	PD1 = 1, PD0 = 0		–43		dBc
Input Voltage Noise	$f = 100\text{ kHz}$		2.4		nV/ $\sqrt{\text{Hz}}$
Input Current Noise	$f = 100\text{ kHz}$		17		pA/ $\sqrt{\text{Hz}}$
<b>DC PERFORMANCE</b>					
Input Offset Voltage		–3	+1	+3	mV
Input Bias Current	Noninverting Input	–9	–2	+3	$\mu\text{A}$
	Inverting Input	–4	+4.5	+16	$\mu\text{A}$
Open-Loop Transimpedance	$R_{LOAD} = 50\ \Omega$	4	14		M $\Omega$
	$R_{LOAD} = 100\ \Omega$	15	35		M $\Omega$
Common-Mode Rejection		57	62		dB
<b>INPUT CHARACTERISTICS</b>					
Input Resistance	+IN, $f < 100\text{ kHz}$		500		k $\Omega$
<b>OUTPUT CHARACTERISTICS</b>					
Single-Ended, +Swing	$R_{LOAD} = 50\ \Omega$	11	11.1		$V_P$
Single-Ended, –Swing	$R_{LOAD} = 50\ \Omega$		0.9	1	$V_P$
Single-Ended, +Swing	$R_{LOAD} = 100\ \Omega$	11	11.1		$V_P$
Single-Ended, –Swing	$R_{LOAD} = 100\ \Omega$		0.8	0.9	$V_P$
Differential Swing	$R_{LOAD} = 100\ \Omega$	20.2	20.6		V p-p
<b>POWER SUPPLY</b>					
Single Supply			12		V
Supply Current	PD1 = 0, PD0 = 0	10.5	11.8	13	mA/amp
	PD1 = 0, PD0 = 1	7	7.9	9	mA/amp
	PD1 = 1, PD0 = 0	4.3	5.2	6.3	mA/amp
	PD1 = 1, PD0 = 1		0.9	1.3	mA/amp

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN PINS					
PD1, PD0 Threshold	Referenced to GND		1.5		V
High Level Input Voltage, $V_{IH}$		2		5	V
Low Level Input Voltage, $V_{IL}$		0		0.8	V
PD1, PD0 = 0 Pin Bias Current	PD1 or PD0 = 0 V	-1.5	-0.2	+1.5	$\mu$ A
PD1, PD0 = 1 Pin Bias Current	PD1 or PD0 = 3 V	40	63	80	$\mu$ A
Enable/Disable Time			130/116		ns
Power Supply Rejection Ratio		-63	-70		dB

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	13.6 V
Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Storage Temperature Range	-65°C to +125°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

Thermal resistance ( $\theta_{JA}$ ) is specified for the worst-case conditions, that is,  $\theta_{JA}$  is specified for device soldered in circuit board for surface-mount packages.

Table 3.

Package Type	$\theta_{JA}$	Unit
10-Lead MINI_SO_EP	44	°C/W

### Maximum Power Dissipation

The maximum safe power dissipation for the ADA4311-1 is limited by the associated rise in junction temperature ( $T_J$ ) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 10-lead MINI\_SO\_EP (44°C/W) on a JEDEC standard 4-layer board.  $\theta_{JA}$  values are approximations.

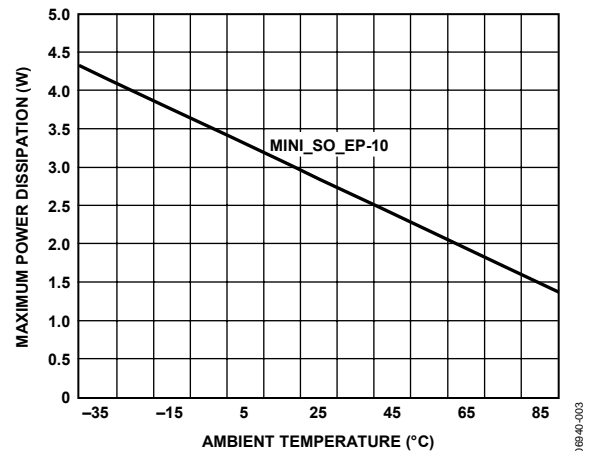


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

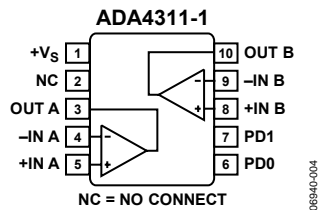
**ADA4311-1****PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**

Figure 4. Pin Configuration

**Table 4. Pin Function Description**

Pin No.	Mnemonic	Description
1	+Vs	Positive Power Supply Input.
2	NC	No Connection.
3	OUT A	Amplifier A Output.
4	-IN A	Amplifier A Inverting Input.
5	+IN A	Amplifier A Noninverting Input.
6	PD0	Power Dissipation Control.
7	PD1	Power Dissipation Control.
8	+IN B	Amplifier B Noninverting Input.
9	-IN B	Amplifier B Inverting Input.
10	OUT B	Amplifier B Output.
11 (Exposed Paddle)	GND	Ground (Electrical Connection Required).

# TYPICAL PERFORMANCE CHARACTERISTICS

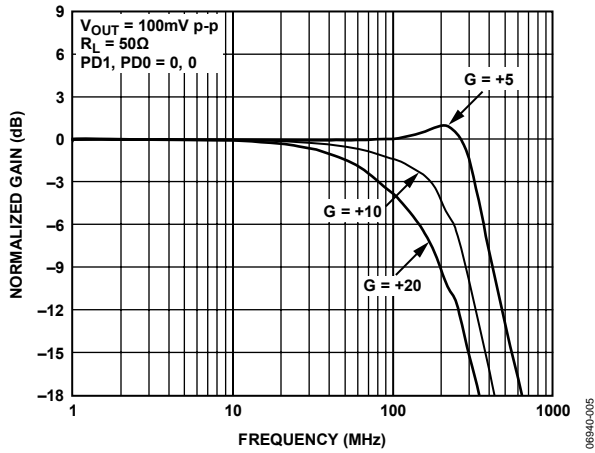


Figure 5. Small Signal Frequency Response for Various Closed-Loop Gains

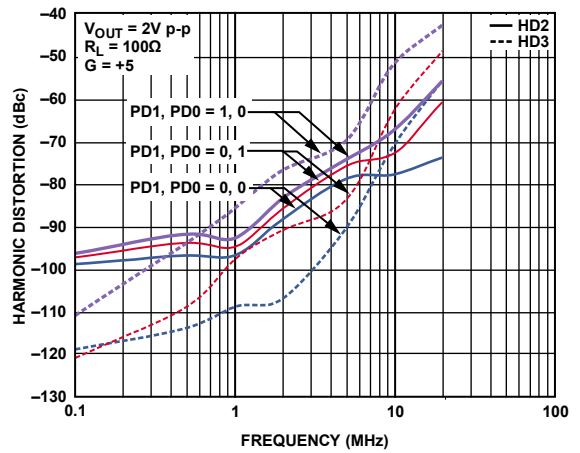


Figure 8. Differential Harmonic Distortion vs. Frequency

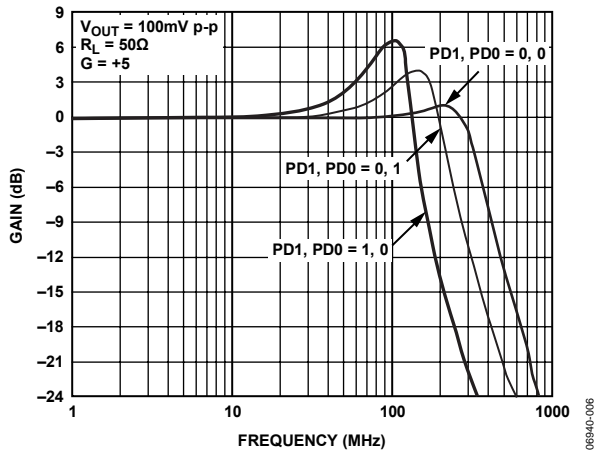


Figure 6. Small Signal Frequency Response for Various Modes

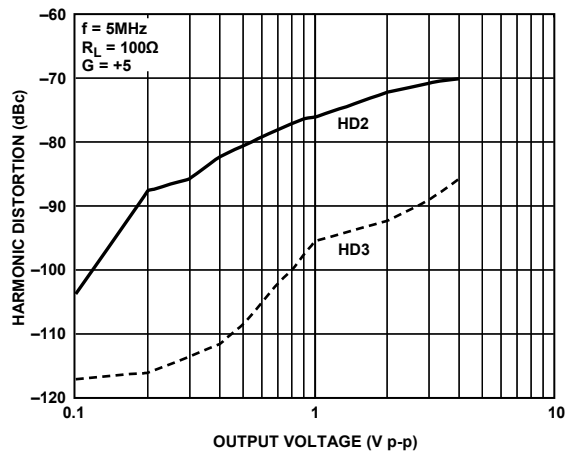


Figure 9. Differential Harmonic Distortion vs. Output Voltage

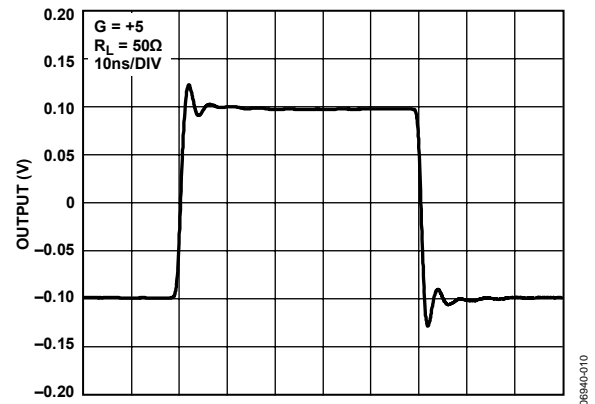


Figure 7. Small Signal Transient Response

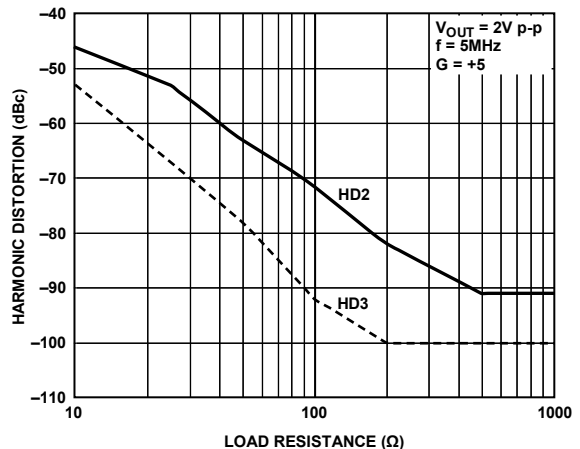


Figure 10. Differential Harmonic Distortion vs. Load Resistance

# ADA4311-1

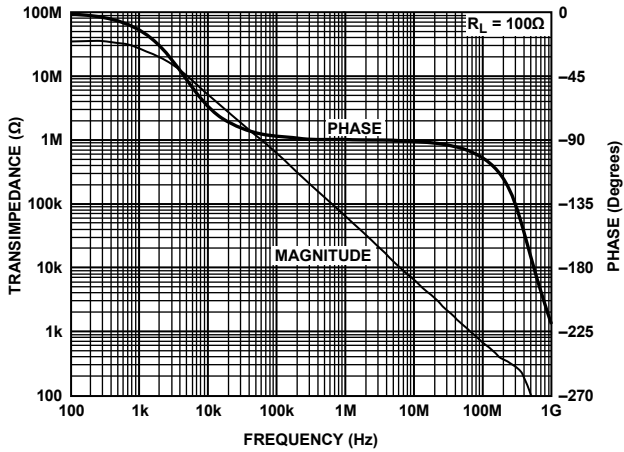


Figure 11. Open-Loop Transimpedance and Phase vs. Frequency

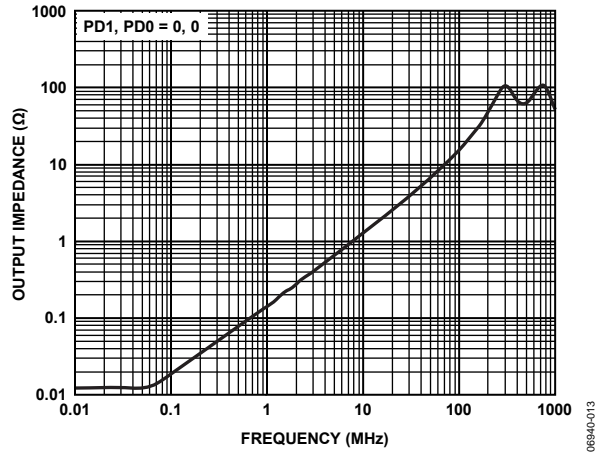


Figure 14. Closed-Loop Output Impedance vs. Frequency

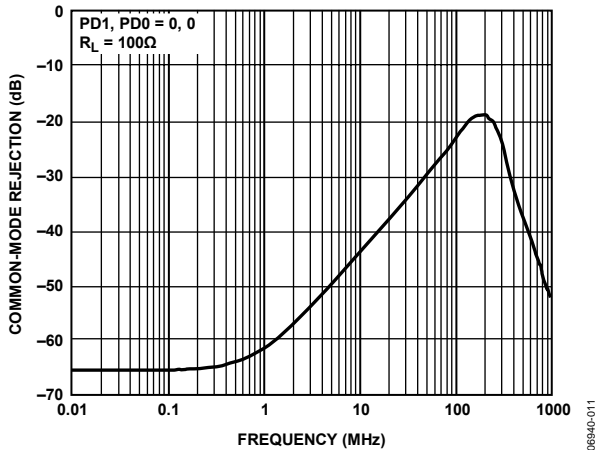


Figure 12. Common-Mode Rejection vs. Frequency

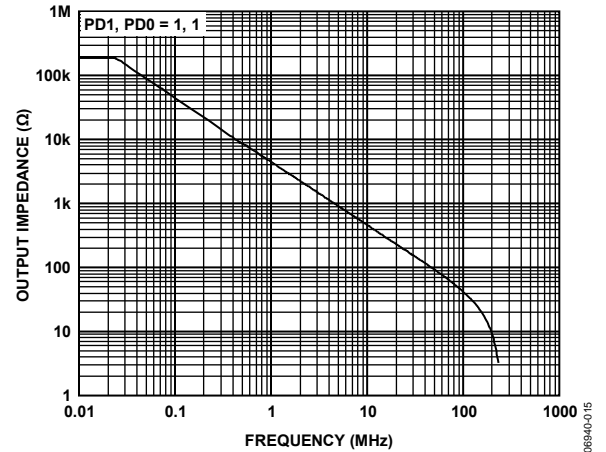


Figure 15. Output Impedance vs. Frequency (Disabled)

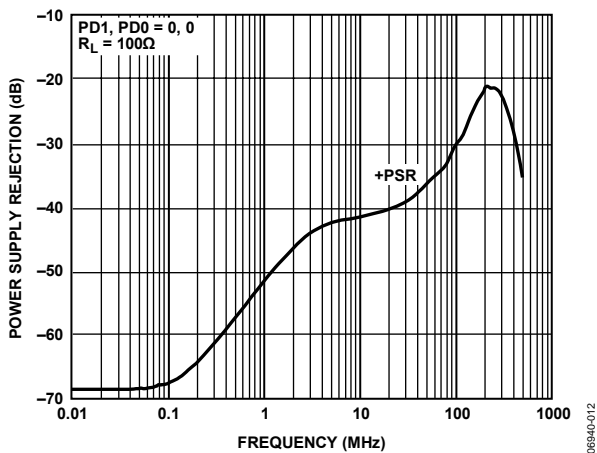


Figure 13. Power Supply Rejection vs. Frequency

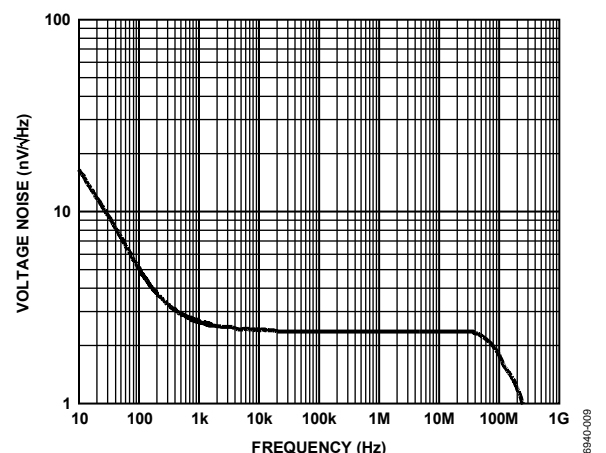


Figure 16. Voltage Noise vs. Frequency



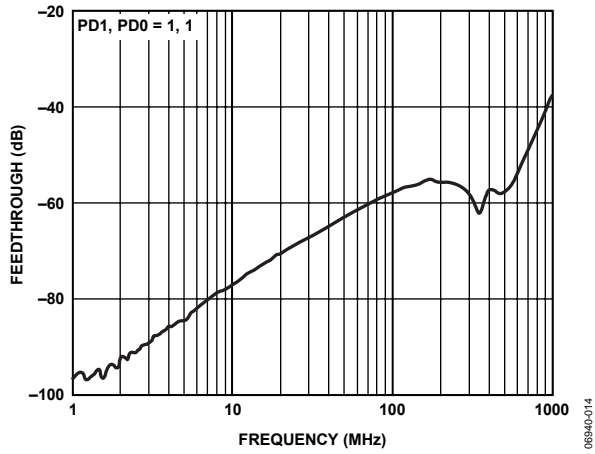


Figure 17. Feedthrough vs. Frequency

06940-014

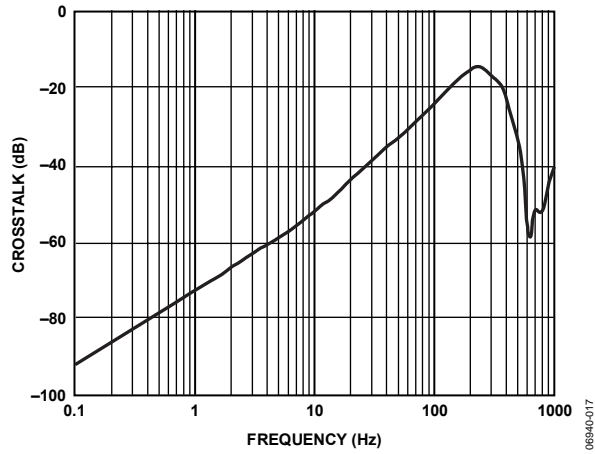


Figure 19. Crosstalk vs. Frequency

06940-017

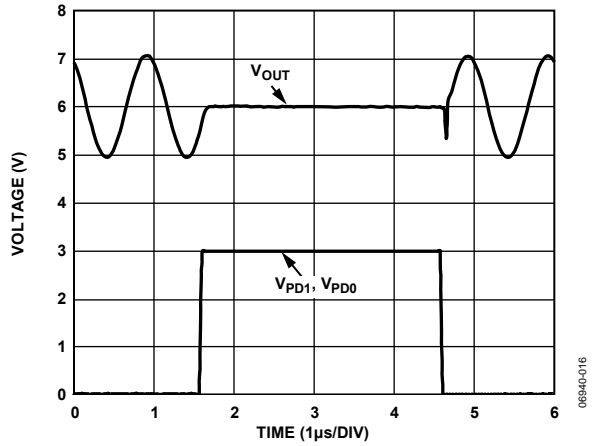


Figure 18. Power-Down Turn On/Turn Off

06940-016

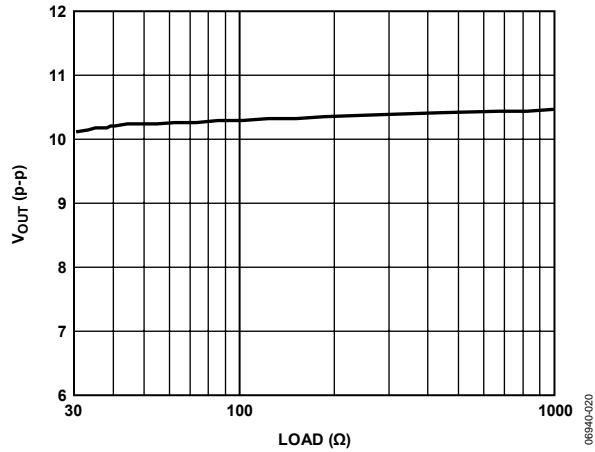


Figure 20. Single-Ended Output Swing vs. Load

06940-020

# ADA4311-1

## THEORY OF OPERATION

The ADA4311-1 is a dual-current feedback amplifier with high output current capability. With a current feedback amplifier, the current into the inverting input is the feedback signal, and the open-loop behavior is that of a transimpedance,  $dV_O/dI_{IN}$  or  $T_Z$ .

The open-loop transimpedance is analogous to the open-loop voltage gain of a voltage feedback amplifier. Figure 21 shows a simplified model of a current feedback amplifier. Because  $R_{IN}$  is proportional to  $1/g_m$ , the equivalent voltage gain is  $T_Z \times g_m$ , where  $g_m$  is the transconductance of the input stage. Basic analysis of the follower with gain circuit yields

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{T_Z(s)}{T_Z(s) + G \times R_{IN} + R_F}$$

where:

$$G = 1 + \frac{R_F}{R_G}$$

$$R_{IN} = \frac{1}{g_m} \approx 50 \Omega$$

Because  $G \times R_{IN} \ll R_F$  for low gains, a current feedback amplifier has relatively constant bandwidth vs. gain, the 3 dB point being set when  $|T_Z| = R_F$ .

For a real amplifier, there are additional poles that contribute excess phase, and there is a value for  $R_F$  below which the amplifier is unstable. Tolerance for peaking and desired flatness determines the optimum  $R_F$  in each application.

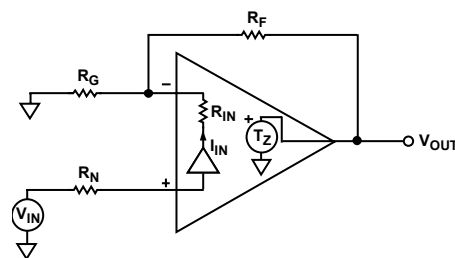


Figure 21. Simplified Block Diagram



# ADA4311-1

## BOARD LAYOUT

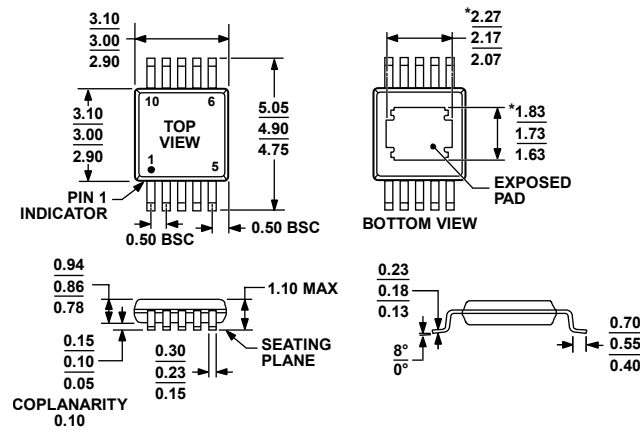
As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. Proper RF design technique is mandatory. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near the input and output pins reduces stray capacitance, particularly in the area of the inverting inputs. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize the inductance and stray capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) though the board. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize balanced performance. When running differential signals over a long distance, the traces on the PCB should be close. Doing this reduces the radiated energy and makes the circuit less susceptible to RF interference. Adherence to stripline design techniques for long signal traces (greater than about 1 inch) is recommended.

For more information on high speed board layout, see [A Practical Guide to High-Speed Printed-Circuit-Board Layout](#).

## POWER SUPPLY BYPASSING

The ADA4311-1 operates on supplies from 6 V to 12 V. The ADA4311-1 circuit should be powered with a well-regulated power supply. Careful attention must be paid to decoupling the power supply. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. In addition, 0.1  $\mu\text{F}$  MLCC decoupling capacitors should be located no more than  $\frac{1}{8}$ -inch away from each of the power supply pins. A large, usually tantalum, 10  $\mu\text{F}$  capacitor is required to provide good decoupling for lower frequency signals and to supply current for fast, large signal changes at the ADA4311-1 outputs. Bypassing capacitors should be laid out in such a manner as to keep return currents away from the inputs of the amplifiers, which minimizes any voltage drops that can develop due to ground currents flowing through the ground plane. A large ground plane also provides a low impedance path for the return currents.

# OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-187-BA-T EXCEPT FOR EXPOSED PAD DIMENSIONS.

Figure 23. 10-Lead Mini Small Outline Package with Exposed Pad [MINI\_SO\_EP] (RH-10-1)  
Dimensions shown in millimeters

073007-B

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADA4311-1ARHZ <sup>1</sup>	-40°C to +85°C	10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-10-1	1A
ADA4311-1ARHZ-RL <sup>1</sup>	-40°C to +85°C	10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-10-1	1A
ADA4311-1ARHZ-R7 <sup>1</sup>	-40°C to +85°C	10-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-10-1	1A

<sup>1</sup> Z = RoHS Compliant Part.

**ADA4311-1**

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