

### FEATURES

HDMI/DVI transmitter compatible with HDMI 1.1 and HDCP 1.1

Single 1.8 V power supply

Video/audio inputs are 3.3 V tolerant

Supports HDCP 1.1 with encrypted internal HDCP key storage

80-lead LQFP

Digital video

80 MHz operation supports all video formats from 480i to 1080i and 720p

Programmable 2-way color space converter

Supports RGB, YCbCr, DDR, ITU656 formats

Auto input video format detection

Digital audio

Supports standard S/PDIF for stereo or compressed audio up to 192 kHz

8-channel LPCM I<sup>2</sup>S audio up to 192 kHz

Special features for easy system design

On-chip MPU to perform HDCP operations

On-chip I<sup>2</sup>C® master to handle EDID reading

5 V tolerant I<sup>2</sup>C and MPD I/Os, no extra device needed

No audio master clock needed for S/PDIF support

### APPLICATIONS

DVD players and recorders

Digital set-top boxes

AV receivers

Digital cameras and camcorders

### GENERAL DESCRIPTION

The AD9389 is an 80 MHz high-definition multimedia interface (HDMI 1.1) transmitter. It supports HDTV formats up to 1080i and 720p, and graphic resolutions up to XGA (1024 × 768 @ 75 Hz). With the inclusion of HDCP, the AD9389 allows the secure transmission of protected content as specified by the HDCP 1.1 protocol.

The AD9389 supports both S/PDIF and 8-channel I<sup>2</sup>S audio. Its high fidelity 8-channel I<sup>2</sup>S can transmit either stereo or 7.1 surround audio at 192 kHz. The S/PDIF can carry stereo LPCM (linear pulse code modulation) audio or compressed audio including Dolby® Digital, DTS®, and THX®.

### FUNCTIONAL BLOCK DIAGRAM

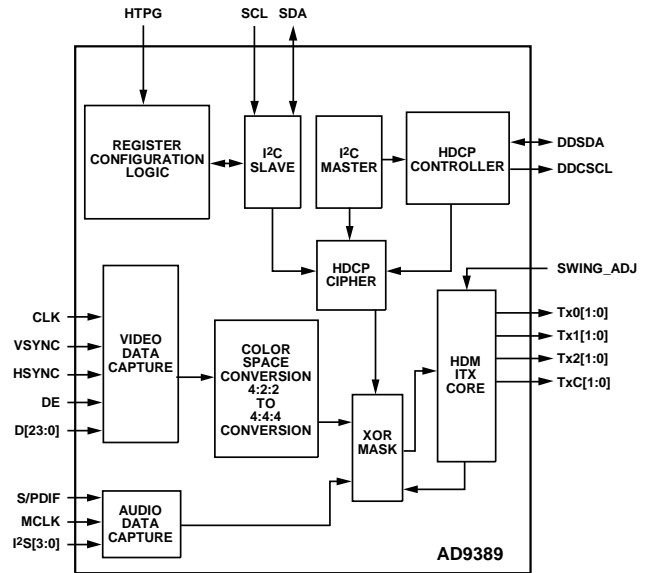


Figure 1.

The AD9389 helps to reduce system design complexity and cost by incorporating such features as HDCP master, I<sup>2</sup>C master for EDID reading, a single 1.8 V power supply, and 5 V tolerance on I<sup>2</sup>C and hot plug detect pins.

Fabricated in an advanced CMOS process, the AD9389 is provided in a space-saving, 80-lead, surface-mount, Pb-free plastic LQFP and is specified over the 0°C to 70°C temperature range.

### EVALUATION KITS AND OTHER RESOURCES

Evaluation kits, reference design schematics, software quick start guide, and codes are available from the Analog Devices local sales and marketing personnel.

#### Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

**TABLE OF CONTENTS**

|   |    |   |    |
|---|----|---|----|
| Features .....  | 1  | I <sup>2</sup> S Audio .....                                    | 16 |
| Applications .....                                      | 1  | S/PDIF Audio .....  | 16 |
| Functional Block Diagram .....                          | 1  | CTS Generation .....  | 16 |
| General Description .....                               | 1  | N Parameter .....   | 17 |
| Evaluation Kits and Other Resources .....               | 1  | CTS Parameter .....   | 17 |
| Revision History .....                                  | 2  | Packet Configuration .....                                      | 18 |
| Electrical Specifications .....                         | 3  | Pixel Repetition .....  | 18 |
| Absolute Maximum Ratings .....                          | 5  | HDCP Handling .....   | 19 |
| Explanation of Test Levels .....                        | 5  | EDID Reading .....  | 19 |
| ESD Caution .....                                       | 5  | Interrupts .....  | 19 |
| Pin Configuration and Function Descriptions .....       | 6  | Power Management .....  | 19 |
| I <sup>2</sup> C Addresses .....                        | 8  | 2-Wire Serial Register Map .....                                | 20 |
| List of Reference Documents .....                       | 8  | 2-Wire Serial Control Register Detail Chip Identification ..... | 33 |
| Format Standards .....                                  | 8  | Source Product Description (SPD) Infoframe .....                | 37 |
| Design Guide .....                                      | 9  | 2-Wire Serial Control Port .....                                | 40 |
| General Description .....                               | 9  | Data Transfer via Serial Interface .....                        | 40 |
| Video Data Capture .....                                | 9  | Serial Interface Read/Write Examples .....                      | 41 |
| Input Formats .....                                     | 9  | PCB Layout Recommendations .....                                | 42 |
| 4:2:2 to 4:4:4 Data Conversion .....                    | 14 | Power Supply Bypassing .....                                    | 42 |
| Horizontal Sync, Vertical Sync, and DE Generation ..... | 14 | Digital Inputs .....  | 42 |
| DE Generation .....                                     | 14 | Color Space Converter (CSC) Common Settings .....               | 43 |
| Hsync and Vsync Generation .....                        | 14 | Outline Dimensions .....  | 45 |
| Color Space Conversion Matrix (CSC) .....               | 15 | Ordering Guide .....  | 45 |
| Audio Data Capture .....                                | 16 |   |    |

**REVISION HISTORY****1/06—Revision 0: Initial Version**

## ELECTRICAL SPECIFICATIONS

Table 1.

| Parameter   | Temp | Test Level <sup>1</sup> | Min             | Typ       | Max  | Unit   |
|---|------|-------------------------|-----------------|-----------|------|--------|
| <b>DIGITAL INPUTS</b>   |      |                         |                 |           |      |        |
| Input Voltage, High ( $V_{IH}$ )  | Full | VI                      | 1.4             |           |      | V      |
| Input Voltage, Low ( $V_{IL}$ )   | Full | VI                      |                 |           | 0.7  | V      |
| Input Current, High ( $I_{IH}$ )  | Full | V                       |                 |           | -1.0 | mA     |
| Input Current, Low ( $I_{IL}$ )   | Full | V                       |                 |           | +1.0 | mA     |
| Input Capacitance   | 25°C | V                       |                 | 3         |      | pF     |
| <b>DIGITAL OUTPUTS</b>  |      |                         |                 |           |      |        |
| Output Voltage, High ( $V_{OH}$ )   | Full | VI                      | $AV_{DD} - 0.1$ |           |      | V      |
| Output Voltage, Low ( $V_{OL}$ )  | Full | VI                      |                 |           | 0.4  | V      |
| <b>THERMAL CHARACTERISTICS</b>  |      |                         |                 |           |      |        |
| $\theta_{JC}$ Junction-to-Case<br>Thermal Resistance  |      | V                       |                 |           | 25   | °C/W   |
| $\theta_{JA}$ Junction-to-Ambient<br>Thermal Resistance   |      | V                       |                 |           | 30   | °C/W   |
| Ambient Temperature   | Full | V                       | 0               | 25        | 70   | °C     |
| <b>DC SPECIFICATIONS</b>  |      |                         |                 |           |      |        |
| Input Leakage Current, $I_{IL}$   | 25°C | VI                      | -10             |           | +10  | μA     |
| Input Clamp Voltage (-16 mA)  | 25°C | V                       |                 | -0.8      |      | V      |
| Input Clamp Voltage (+16 mA)  | 25°C | V                       |                 | +0.8      |      | V      |
| Differential High Level Output Voltage  |      | V                       |                 | $AV_{CC}$ |      | V      |
| Differential Output Short-Circuit Current   |      | V                       |                 |           | 10   | μA     |
| <b>POWER SUPPLY</b>   |      |                         |                 |           |      |        |
| $V_{DD}$ (All) Supply Voltage   | Full | IV                      | 1.71            | 1.8       | 1.89 | V      |
| $V_{DD}$ Supply Voltage Noise   | Full | V                       |                 |           | 50   | mV p-p |
| Complete Power-Down Current<br>(Everything Except I <sup>2</sup> C)                                 | 25°C | IV                      |                 | 6         | 13   | mA     |
| Quiet Power Down Current<br>(Monitor Detect On)   | 25°C | VI                      |                 | 7         |      | mA     |
| Transmitter Supply Current<br>(27 MHz Typical Random Pattern)                                       | 25°C | VI                      |                 | 165       |      | mA     |
| Transmitter Supply Current<br>(80 MHz Typical Random Pattern)                                       | 25°C | IV                      |                 | 185       | 205  | mA     |
| Transmitter Total Power<br>(80 MHz Single Pixel Stripe Pattern; Worst<br>Case Operating Conditions) | Full | VI                      |                 |           | 430  | mW     |
| <b>AC SPECIFICATIONS</b>  |      |                         |                 |           |      |        |
| CLK Frequency   | 25°C | IV                      | 13.5            |           | 80   | MHz    |
| CLK Duty Cycle  | 25°C | VII                     | 40              |           | 60   | %      |
| Worst Case CLK Input Jitter   | Full | VI                      |                 |           | 1.0  | ns     |
| Setup Time to CLK Falling Edge  |      | VI                      | TBD             |           | TBD  | ns     |
| Hold Time to CLK Falling Edge   |      | VI                      | TBD             |           | TBD  | ns     |
| TMDS Differential Swing   |      | VII                     | 800             | 1000      | 1200 | mV     |
| VSYNC and HSYNC Delay from DE Falling Edge  |      | VI                      |                 | 1         |      | UI     |
| VSYNC and HSYNC Delay to DE Rising Edge   |      | VI                      |                 | 1         |      | UI     |
| DE High Time  | 25°C | VI                      |                 |           | 8191 | UI     |
| DE Low Time   | 25°C | VI                      |                 | 138       |      | UI     |
| Differential Output Swing Low-to-High<br>Transition Time  | 25°C | VII                     | 75              |           | 490  | ps     |
| Differential Swing Output High-to-Low<br>Transition Time  | 25°C | VII                     | 75              |           | 490  | ps     |

# AD9389

| Parameter                                 | Temp | Test Level <sup>1</sup> | Min | Typ | Max | Unit |
|---|------|-------------------------|-----|-----|-----|------|
| AUDIO AC TIMING                           |      |                         |     |     |     |      |
| Sample Rate (I <sup>2</sup> S and S/PDIF) | Full | IV                      | 32  |     | 192 | kHz  |
| I <sup>2</sup> S Cycle Time               | 25°C | IV                      |     |     | 1   | UI   |
| I <sup>2</sup> S Setup Time               | 25°C | IV                      |     | 15  |     | ns   |
| I <sup>2</sup> S Hold Time                | 25°C | IV                      |     | 0   |     | ns   |
| Audio Pipeline Delay                      | 25°C | IV                      |     | 75  |     | μs   |

<sup>1</sup> See Table 3.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter                    | Rating          |
|------------------------------|-----------------|
| Digital Inputs               | 5 V to 0.0 V    |
| Digital Output Current       | 20 mA           |
| Operating Temperature Range  | −40°C to +85°C  |
| Storage Temperature Range    | −65°C to +150°C |
| Maximum Junction Temperature | 150°C           |
| Maximum Case Temperature     | 150°C           |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## EXPLANATION OF TEST LEVELS

Table 3.

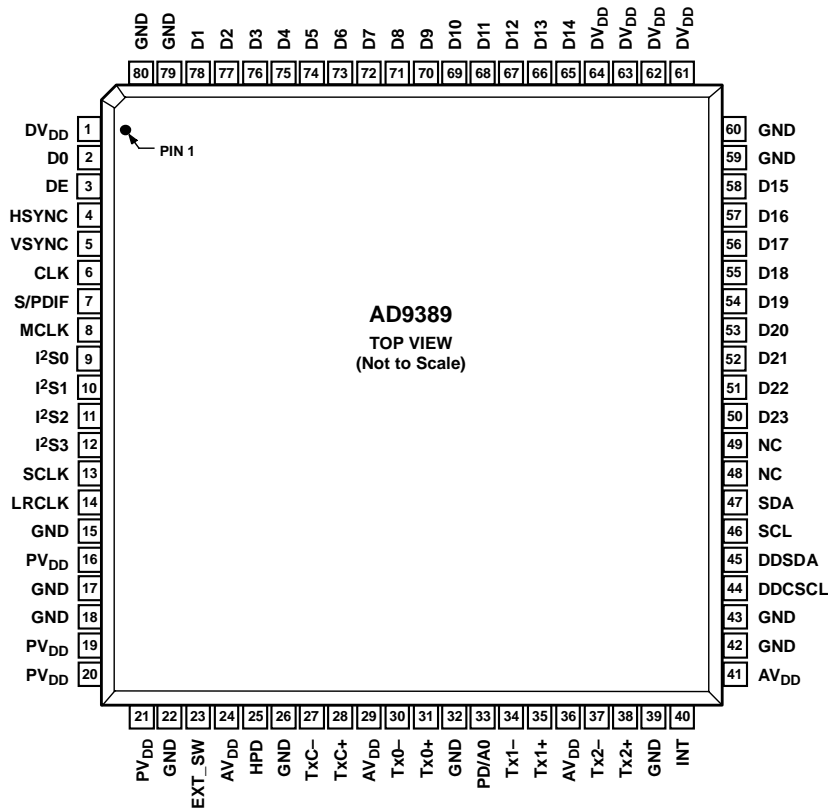
| Level | Test   |
|-------|--|
| I     | 100% production tested.  |
| II    | 100% production tested at 25°C and sample tested at specified temperatures.        |
| III   | Sample tested only.  |
| IV    | Parameter is guaranteed by design and characterization testing.                    |
| V     | Parameter is a typical value only.   |
| VI    | 100% production tested at 25°C; guaranteed by design and characterization testing. |
| VII   | Limits defined by HDMI specification.  |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



05724-002

Figure 2. Pin Configuration

Table 4. Complete Pinout List

| Pin Type | Pin No.                  | Mnemonic     | Description   | Value      |
|----------|--------------------------|--------------|---|------------|
| INPUTS   | 50 to 58,<br>65 to 78, 2 | D[23:0]      | Video Data Input  | 1.8 V CMOS |
|          | 6                        | CLK          | Video Clock Input   | 1.8 V CMOS |
|          | 3                        | DE           | Data Enable Bit for Digital Video   | 1.8 V CMOS |
|          | 4                        | HSYNC        | Horizontal SYNC Input   | 1.8 V CMOS |
|          | 5                        | VSYNC        | Vertical SYNC Input   | 1.8 V CMOS |
|          | 23                       | EXT_SW       | Differential Output Swing Adjustment                                      | 1.8 V CMOS |
|          | 25                       | HPD          | Hot Plug Detect Signal  | 1.8 V CMOS |
|          | 7                        | S/PDIF       | S/PDIF (Sony/Philips Digital Interface) Audio Input Pin                   | 1.8 V CMOS |
|          | 8                        | MCLK         | Audio Reference Clock, from $128 \times f_s$ to $512 \times f_s$          | 1.8 V CMOS |
|          | 12 to 9                  | I2S[3:0]     | I2S Audio Data Inputs   | 1.8 V CMOS |
|          | 13                       | SCLK         | I2S Audio Clock   | 1.8 V CMOS |
|          | 14                       | LRCLK        | Left/Right Channel Selection  | 1.8 V CMOS |
|          | 33                       | PD/A0        | Power-Down Control  | 1.8 V CMOS |
| OUTPUTS  | 28, 27                   | TxC+<br>TxC- | Differential Clock Output<br>Differential Clock Output Complement         | TMDS       |
|          | 38, 37                   | Tx2+<br>Tx2- | Differential Output Channel 2<br>Differential Output Channel 2 Complement | TMDS       |
|          | 35, 34                   | Tx1+<br>Tx1- | Differential Output Channel 1<br>Differential Output Channel 1 Complement | TMDS       |

| Pin Type     | Pin No.   | Mnemonic         | Description                              | Value      |
|--------------|---|------------------|--|------------|
|              | 31, 30  | Tx0+             | Differential Output Channel 0            | TMDS       |
|              |   | Tx0–             | Differential Output Channel 0 Complement |            |
|              | 40  | INT              | Interrupt                                | 1.8 V CMOS |
| POWER SUPPLY | 24, 29, 36, 41  | AV <sub>DD</sub> | Output Power Supply                      | 1.8 V      |
|              | 1, 61, 62, 63, 64   | DV <sub>DD</sub> | Digital and I/O Power Supply             | 1.8 V      |
|              | 16, 19, 20, 21  | PV <sub>DD</sub> | PLL Power Supply                         | 1.8 V      |
|              | 15, 17, 18, 22,<br>26, 32, 39, 42,<br>43, 59, 60, 79,<br>80 | GND              | Ground                                   | 0 V        |
| CONTROL      | 47  | SDA              | Serial Port Data I/O                     | 3.3 V CMOS |
|              | 46  | SCL              | Serial Port Data Clock (100 kHz Maximum) | 3.3 V CMOS |
|              | 45  | DDSDA            | Serial Port Data I/O to Receiver         | 3.3 V CMOS |
|              | 44  | DDCSCL           | Serial Port Data Clock to Receiver       | 3.3 V CMOS |
| NO CONNECT   | 48, 49  | NC               | No Connect.                              |            |

Table 5. Pin Function Descriptions

| Pin Mnemonic          | Description  |
|-----------------------|--|
| OUTPUTS               |  |
| TxC+                  | Differential Clock Output at Pixel Clock Rate; Transition Minimized Differential Signaling (TMDS).                             |
| TxC–                  | Differential Clock Output Complement.  |
| Tx2+                  | Differential Output of the Red Data at 10× the Pixel Clock Rate; TMDS.   |
| Tx2–                  | Differential Red Output Complement.  |
| Tx1+                  | Differential Output of the Green Data at 10× the Pixel Clock Rate; TMDS.   |
| Tx1–                  | Differential Green Output Complement.  |
| Tx0+                  | Differential Output of the Blue Data at 10× the Pixel Clock Rate; TMDS.  |
| Tx0–                  | Differential Blue Output Complement.   |
| INT                   | Interrupt.   |
| SERIAL PORT (2-WIRE)  |  |
| SDA                   | Serial Port Data I/O.  |
| SCL                   | Serial Port Data Clock.  |
| DDSDA                 | Serial Port Data I/O Master to Receiver.   |
| DDCSCL                | Serial Port Data Clock Master to Receiver.   |
|                       | For a full, functional description of the 2-wire serial register, refer to the 2-Wire Serial Control Port section.             |
| INPUTS                |  |
| D[23:0]               | Digital Input in RGB or YCbCr Format.  |
| CLK                   | Video Clock Input.   |
| DE                    | Data Enable for Video Data.  |
| HSYNC                 | Horizontal Sync Input.   |
| VSYNC                 | Vertical Sync Input. This is the input for vertical sync.  |
| EXT_SW                | Place an 887 Ω resistor (1% tolerance) between this pin and ground.  |
| HPD                   | Hot Plug Detect. This indicates to the interface whether the receiver is connected.  |
| S/PDIF                | S/PDIF Audio Input. This is the audio input from a Sony/Philips Digital Interface.   |
| MCLK                  | Audio Reference Clock. Can be set from 128 × f <sub>s</sub> to 512 × f <sub>s</sub> .  |
| I <sup>2</sup> S[3:0] | I <sup>2</sup> S Audio Inputs. These represent the eight channels of audio (two per input) available through I <sup>2</sup> S. |
| I <sup>2</sup> S CLK  | I <sup>2</sup> S Audio Clock.  |
| LRCLK                 | Left/Right Channel Selection.  |
| PD/A0                 | Power Down.  |

# AD9389

| Pin Mnemonic     | Description  |
|------------------|--|
| POWER SUPPLY     |  |
| DV <sub>DD</sub> | Main Power Supply. These pins supply power to the main elements of the circuit. They should be filtered and as quiet as possible.  |
| AV <sub>DD</sub> | Output Power Supply.   |
| PV <sub>DD</sub> | Clock Generator Power Supply. The most sensitive portion of the AD9389 is the clock generation circuitry. These pins provide power to the clock PLL (phase-locked loop) and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins. |
| GND              | Ground. The ground return for all circuitry on-chip. It is recommended that the AD9389 be assembled on a single solid ground plane, with careful attention given to ground current paths.  |

## I<sup>2</sup>C ADDRESSES

The SDA/SCL programming address can be 0x72 or 0x7A based on whether the PD/A0 pin is pulled high (10 k $\Omega$  resistor = 0x7A) or pulled low (10 k $\Omega$  resistor = 0x72).

The EDID EEPROM on the receiver is expected to have an address of 0xA0.

## LIST OF REFERENCE DOCUMENTS

Table 6.

| Document       | Description  |
|----------------|--|
| EIA/CEA-861B   | Describes audio and video infoframes as well as the E-EDID structure for HDMI.   |
| HDMI v1.1      | Defining document for HDMI Version 1.1. Can be located at <a href="http://www.hdmi.org">www.hdmi.org</a> .             |
| HDCPv1.1       | Defining document for HDCP Version 1.1. Can be located at <a href="http://www.digital-cp.com">www.digital-cp.com</a> . |
| ITU-R BT.656-3 | Defining document for BT656.   |

## FORMAT STANDARDS

In this document, data is represented in a variety of ways.

Table 7.

| Data Type | Format   |
|-----------|--|
| 0xNN      | Hexadecimal (base-16) numbers are represented using the C language notation, preceded by 0x.                                   |
| 0bNN      | Binary (base-2) numbers are represented using the C language notation, preceded by 0b.   |
| NN        | Decimal (base-10) numbers are represented using no additional prefixes or suffixes.  |
| Bit       | Bits are numbered in little-endian format, that is, the least significant bit (LSB) of a byte or word is referred to as Bit 0. |



## DESIGN GUIDE

### GENERAL DESCRIPTION

The AD9389 HDMI transmitter provides a high bandwidth digital content protected (HDCP) digital link between a wide range of digital input formats—both audio and video (see Table 8) and output formats (see Table 9). Video and audio data are captured and prepared for transmission while two separate I<sup>2</sup>C buses (one of which is a master) are used to program and provide content protection for the data to be transmitted.

### VIDEO DATA CAPTURE

The AD9389 can accept video data from as few as eight pins (YCbCr DDR) representing 8-bit data or as many as 24 pins representing 12-bit data. The AD9389 is capable of detecting all of the 34 video formats defined in the EIA/CEA-861B specification. If video ID (VID) 32, 33, or 34 is present, the user needs to set Register 0x15[0] to 0b1, as these modes have  $V_{REF}$  frequencies of 30 Hz or less. The user can read the detected video format at 0x3E[7:2]. Formats outside the EIA/CEA-861B specification can be read in 0x3F[7:5]. Detailed line count differences for 240p and 288p modes can be read from 0x3F[4:3]. In order to distinguish between an aspect ratio of 4:3 and one of 16:9, 0x17[1] should be set accordingly.

Table 8. Input Formats Supported

| No. of Bits | Input Format          |
|-------------|-----------------------|
| 12          | RGB (DDR)             |
| 12          | YCbCr 4:4:4 (DDR)     |
| 24          | RGB 4:4:4             |
| 24          | YCbCr 4:4:4           |
| 16          | YCbCr 4:2:2 (ITU.601) |
| 20          | YCbCr 4:2:2 (ITU.601) |
| 24          | YCbCr 4:2:2 (ITU.601) |
| 8           | YCbCr (DDR)           |
| 10          | YCbCr (DDR)           |
| 12          | YCbCr (DDR)           |
| 8           | YCbCr 4:2:2 (ITU.656) |
| 10          | YCbCr 4:2:2 (ITU.656) |
| 12          | YCbCr 4:2:2 (ITU.656) |

Table 9. Output Formats Supported

| No. of Bits | Output Format |
|-------------|---------------|
| 24          | RGB 4:4:4     |
| 24          | YCbCr 4:4:4   |
| 16          | YCbCr 4:2:2   |
| 20          | YCbCr 4:2:2   |
| 24          | YCbCr 4:2:2   |

### INPUT FORMATS

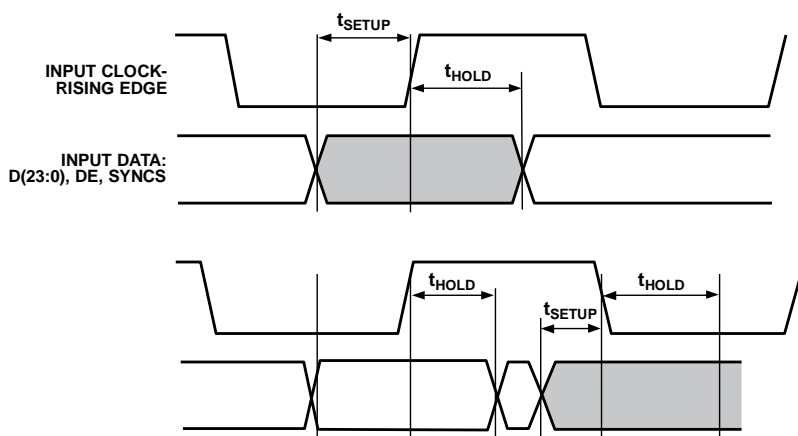


Figure 3. Timing for Data Input

05724-013

# AD9389

## Normal 4:4:4 Input Format (RGB or YCbCr) Input ID = 0

An input format of RGB 4:4:4 or YCbCr 4:4:4 can be selected by setting the input ID (0x15[3:1]) to 0b000. The input color space (CS) must be selected by setting 0x16[0] to 0b0 for RGB or 0b1 for YCbCr. There is no need to set the input style (0x16[3:2]).

Table 10.

| Input Format | Data[23:0] |    |    |    |    |    |    |        |    |    |    |    |    |    |         |   |   |   |   |   |   |   |   |
|--------------|------------|----|----|----|----|----|----|--------|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|
|              | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16     | 15 | 14 | 13 | 12 | 11 | 10 | 9       | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| RGB 4:4:4    | R[7:0]     |    |    |    |    |    |    | G[7:0] |    |    |    |    |    |    | B[7:0]  |   |   |   |   |   |   |   |   |
| YCbCr 4:4:4  | Cr[7:0]    |    |    |    |    |    |    | Y[7:0] |    |    |    |    |    |    | Cb[7:0] |   |   |   |   |   |   |   |   |

## YCbCr 4:2:2 Formats (24 bits, 20 bits, or 16 bits) with Separate Sync, Input ID = 1

An input with YCbCr 4:2:2 with separate syncs can be selected by setting the Input ID (0x15[3:1]) to 0b001. The input CS (0x16[0]) must be set to 0b1 for proper operation. The data bit width (24 bits, 20 bits, or 16 bits) must be set with 0x16[5:4]. The three input pin assignment styles are shown in Table 11. The input style can be set in 0x16[3:2].

Table 11.

| Input Format                   | Data[23:0] |    |    |    |    |    |    |         |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
|--------------------------------|------------|----|----|----|----|----|----|---------|----|---------|----|----------|----|----|---------|---|--------|--------|---|---|---|---|---|---|
|                                | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16      | 15 | 14      | 13 | 12       | 11 | 10 | 9       | 8 | 7      | 6      | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Style 1</b>                 |            |    |    |    |    |    |    |         |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Sync (24 bit) | Cb[11:4]   |    |    |    |    |    |    | Y[11:4] |    |         |    |          |    |    | Cb[3:0] |   |        | Y[3:0] |   |   |   |   |   |   |
|                                | Cr[11:4]   |    |    |    |    |    |    | Y[11:4] |    |         |    |          |    |    | Cr[3:0] |   |        | Y[3:0] |   |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Sync (20 bit) | Cb[9:2]    |    |    |    |    |    |    | Y[9:2]  |    |         |    |          |    |    | Cb[1:0] |   | Y[1:0] |        |   |   |   |   |   |   |
|                                | Cr[9:2]    |    |    |    |    |    |    | Y[9:2]  |    |         |    |          |    |    | Cr[1:0] |   | Y[1:0] |        |   |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Sync (20 bit) | Cb[7:0]    |    |    |    |    |    |    | Y[7:0]  |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Cr[7:0]    |    |    |    |    |    |    | Y[7:0]  |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| <b>Style 2</b>                 |            |    |    |    |    |    |    |         |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| 24-bit                         | Cb[11:0]   |    |    |    |    |    |    |         |    |         |    | Y[11:0]  |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Cr[11:0]   |    |    |    |    |    |    |         |    |         |    | Y[11:0]  |    |    |         |   |        |        |   |   |   |   |   |   |
| 20-bit                         | Cb[9:0]    |    |    |    |    |    |    |         |    | Y[9:0]  |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Cr[9:0]    |    |    |    |    |    |    |         |    | Y[9:0]  |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| 16-bit                         | Cb[7:0]    |    |    |    |    |    |    | Y[7:0]  |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Cr[7:0]    |    |    |    |    |    |    | Y[7:0]  |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| <b>Style 3</b>                 |            |    |    |    |    |    |    |         |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| 24-bit                         | Y[11:0]    |    |    |    |    |    |    |         |    |         |    | Cb[11:0] |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Y[11:0]    |    |    |    |    |    |    |         |    |         |    | Cr[11:0] |    |    |         |   |        |        |   |   |   |   |   |   |
| 20-bit                         | Y[9:0]     |    |    |    |    |    |    |         |    | Cb[9:0] |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Y[9:0]     |    |    |    |    |    |    |         |    | Cr[9:0] |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
| 16-bit                         | Y[7:0]     |    |    |    |    |    |    | Cb[7:0] |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |
|                                | Y[7:0]     |    |    |    |    |    |    | Cr[7:0] |    |         |    |          |    |    |         |   |        |        |   |   |   |   |   |   |

**YCbCr 4:2:2 Formats (24 bits, 20 bits, or 16 bits) with Embedded Syncs, Input ID = 2**

An input with YCbCr 4:2:2 with embedded syncs can be selected by setting the input ID (0x15[3:1]) to 0b010. HSYNC and VSYNC are embedded as Start of Active Video (SAV) and End of Active Video (EAV). The input CS (0x16[0]) must be set to 0b1 for proper operation. The data bit width (24 = 12 bits, 20 = 10 bits, or 16 = 8 bits) must be set with 0x16[5:4]. The three input pin assignment styles are shown in Table 12. The input style can be set in 0x16[3:2]. The only difference between Input ID 1 and Input ID 2 is that the syncs on ID 2 are embedded in the data much like ITU 656 running at 1× clock and double width.

**Table 12.**

| Input Format                   | Data[23:0]           |    |    |    |    |    |    |                    |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |
|--------------------------------|----------------------|----|----|----|----|----|----|--------------------|----|--------------------|----|----------------------|----|----|---------|---|--------|--------|---|---|---|---|---|
|                                | 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16                 | 15 | 14                 | 13 | 12                   | 11 | 10 | 9       | 8 | 7      | 6      | 5 | 4 | 3 | 2 | 1 |
| <b>Style 1</b>                 |                      |    |    |    |    |    |    |                    |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Sync (24 bit) | Cb[11:4]             |    |    |    |    |    |    | Y[11:4]            |    |                    |    |                      |    |    | Cb[3:0] |   |        | Y[3:0] |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Sync (20 bit) | Cb[9:2]              |    |    |    |    |    |    | Y[9:2]             |    |                    |    |                      |    |    | Cb[1:0] |   | Y[1:0] |        |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Sync (16 bit) | Cb[7:0]              |    |    |    |    |    |    | Y[7:0]             |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| <b>Style 2</b>                 |                      |    |    |    |    |    |    |                    |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| 24-bit                         | Cb[11:0]<br>Cr[11:0] |    |    |    |    |    |    |                    |    |                    |    | Y[11:0]<br>Y[11:0]   |    |    |         |   |        |        |   |   |   |   |   |
| 20-bit                         | Cb[9:0]<br>Cr[9:0]   |    |    |    |    |    |    |                    |    | Y[9:0]<br>Y[9:0]   |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| 16-bit                         | Cb[7:0]<br>Cr[7:0]   |    |    |    |    |    |    | Y[7:0]<br>Y[7:0]   |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| <b>Style 3</b>                 |                      |    |    |    |    |    |    |                    |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| 24-bit                         | Y[11:0]<br>Y[11:0]   |    |    |    |    |    |    |                    |    |                    |    | Cb[11:0]<br>Cr[11:0] |    |    |         |   |        |        |   |   |   |   |   |
| 20-bit                         | Y[9:0]<br>Y[9:0]     |    |    |    |    |    |    |                    |    | Cb[9:0]<br>Cr[9:0] |    |                      |    |    |         |   |        |        |   |   |   |   |   |
| 16-bit                         | Y[7:0]<br>Y[7:0]     |    |    |    |    |    |    | Cb[7:0]<br>Cr[7:0] |    |                    |    |                      |    |    |         |   |        |        |   |   |   |   |   |

**YCbCr 4:2:2 Formats (Double Data Rate) Formats (12 bits, 10 bits, or 8 bits) with Separate Syncs, Input ID = 3**

An input with YCbCr 4:2:2 DDR data and separate syncs can be selected by setting the input ID (0x15[3:1]) to 0b011. The Input CS (0x16[0]) must be set to 0b1. The data bit width (12 bits, 10 bits, or 8 bits) must be set with 0x16[5:4]. The two input pin assignment styles are shown in Table 13. The input style can be set in 0x16[3:2].

**Table 13.**

| Input Format   | Data[23:0] |    |    |    |    |    |    |    |    |    |    |                 |    |    |   |   |   |   |   |   |   |   |   |       |
|----------------|------------|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|---|---|---|---|---|---|---|---|---|-------|
|                | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12              | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| <b>Style 1</b> |            |    |    |    |    |    |    |    |    |    |    |                 |    |    |   |   |   |   |   |   |   |   |   |       |
| 12-bit         |            |    |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[11:4] |    |    |   |   |   |   |   |   |   |   |   |       |
| 10-bit         |            |    |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[9:2]  |    |    |   |   |   |   |   |   |   |   |   | [3:0] |
| 8-bit          |            |    |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[7:0]  |    |    |   |   |   |   |   |   |   |   |   | [1:0] |
| <b>Style 2</b> |            |    |    |    |    |    |    |    |    |    |    |                 |    |    |   |   |   |   |   |   |   |   |   |       |
| 12-bit         |            |    |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[11:0] |    |    |   |   |   |   |   |   |   |   |   |       |
| 10-bit         |            |    |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[9:0]  |    |    |   |   |   |   |   |   |   |   |   |       |
| 8-bit          |            |    |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[7:0]  |    |    |   |   |   |   |   |   |   |   |   |       |

# AD9389

## YCbCr 4:2:2 DDR (Double Data Rate) Formats (12 bits, 10 bits, or 8 bits) with Embedded Syncs, Input ID = 4

An input with YCbCr 4:2:2 DDR data and embedded syncs (ITU 656) can be selected by setting the input ID (0x15[3:1]) to 0b100. The Input CS (0x16[0]) must be set to 0b1. The data bit width (12 bits, 10 bits, or 8 bits) must be set with 0x16[5:4]. The two input pin assignment styles are shown in Table 14. The input style can be set in 0x16[3:2]. The order of data input is the order in the table (for example, 12 bit data is accepted as: Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3).

Table 14.

| Input Format   | Data[23:0] |    |    |    |    |    |    |    |    |    |                 |    |    |    |   |   |   |   |   |       |   |   |   |   |
|----------------|------------|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|---|---|---|---|---|-------|---|---|---|---|
|                | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13              | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |
| <b>Style 1</b> |            |    |    |    |    |    |    |    |    |    |                 |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 12-bit         |            |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[11:4] |    |    |    |   |   |   |   |   | [3:0] |   |   |   |   |
| 10-bit         |            |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[9:2]  |    |    |    |   |   |   |   |   | [1:0] |   |   |   |   |
| 8-bit          |            |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[7:0]  |    |    |    |   |   |   |   |   |       |   |   |   |   |
| <b>Style 2</b> |            |    |    |    |    |    |    |    |    |    |                 |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 12-bit         |            |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[11:0] |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 10-bit         |            |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[9:0]  |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 8-bit          |            |    |    |    |    |    |    |    |    |    | Cb/Y/Cr/Y[7:0]  |    |    |    |   |   |   |   |   |       |   |   |   |   |

## Normal 4:4:4 Input Format (RGB or YCbCr) Clocked at Double Data Rate (DDR), Input ID = 5

An input with YCbCr 4:4:4 DDR data and separate syncs can be selected by setting the input ID (0x15[3:1]) to 0b011. The input CS (0x16[0]) must be set to 0b1. The data bit width (12 bits, 10 bits, or 8 bits) must be set with 0x16[5:4]. The three input pin assignment styles are shown in Table 15. The input style can be set in 0x16[3:2].

Table 15.

| Input Format   | Data[23:0] |    |    |    |    |    |    |    |    |    |         |    |    |    |   |   |         |   |   |   |   |   |   |   |
|--|------------|----|----|----|----|----|----|----|----|----|---------|----|----|----|---|---|---------|---|---|---|---|---|---|---|
|  | 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13      | 12 | 11 | 10 | 9 | 8 | 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Style 1</b>   |            |    |    |    |    |    |    |    |    |    |         |    |    |    |   |   |         |   |   |   |   |   |   |   |
| RGB 4:4:4 (DDR)<br>(1 <sup>st</sup> edge,<br>2 <sup>nd</sup> edge)   |            |    |    |    |    |    |    |    |    |    | G[3:0]  |    |    |    |   |   | B[7:0]  |   |   |   |   |   |   |   |
|  |            |    |    |    |    |    |    |    |    |    | R[7:0]  |    |    |    |   |   | G[7:4]  |   |   |   |   |   |   |   |
| YCbCr 4:4:4 (DDR)<br>(1 <sup>st</sup> edge,<br>2 <sup>nd</sup> edge) |            |    |    |    |    |    |    |    |    |    | Y[3:0]  |    |    |    |   |   | Cb[7:0] |   |   |   |   |   |   |   |
|  |            |    |    |    |    |    |    |    |    |    | Cr[7:0] |    |    |    |   |   | Y[7:4]  |   |   |   |   |   |   |   |
| <b>Style 2</b>   |            |    |    |    |    |    |    |    |    |    |         |    |    |    |   |   |         |   |   |   |   |   |   |   |
| RGB 4:4:4 (DDR)<br>(1 <sup>st</sup> edge,<br>2 <sup>nd</sup> edge)   |            |    |    |    |    |    |    |    |    |    | R[7:0]  |    |    |    |   |   | G[7:4]  |   |   |   |   |   |   |   |
|  |            |    |    |    |    |    |    |    |    |    | G[3:0]  |    |    |    |   |   | B[7:0]  |   |   |   |   |   |   |   |
| YCbCr 4:4:4 (DDR)<br>(1 <sup>st</sup> edge,<br>2 <sup>nd</sup> edge) |            |    |    |    |    |    |    |    |    |    | Cr[7:0] |    |    |    |   |   | Y[7:4]  |   |   |   |   |   |   |   |
|  |            |    |    |    |    |    |    |    |    |    | Y[3:0]  |    |    |    |   |   | Cb[7:0] |   |   |   |   |   |   |   |
| <b>Style 3</b>   |            |    |    |    |    |    |    |    |    |    |         |    |    |    |   |   |         |   |   |   |   |   |   |   |
| YCbCr 4:4:4 (DDR)<br>(1 <sup>st</sup> edge,<br>2 <sup>nd</sup> edge) |            |    |    |    |    |    |    |    |    |    | Y[7:0]  |    |    |    |   |   | Cb[7:4] |   |   |   |   |   |   |   |
|  |            |    |    |    |    |    |    |    |    |    | Cb[3:0] |    |    |    |   |   | Cr[7:0] |   |   |   |   |   |   |   |

**YCbCr 4:2:2 Formats (24 bits, 20 bits, or 16 bits) DDR with Separate Sync, Input ID = 6**

An input format of YCbCr 4:2:2 DDR can be selected by setting the input ID (0x15[3:1]) to 0b110. The three different input pin assignment styles are shown in Table 16. The input style can be set in 0x16[3:2]. The input CS (0x16[0]) must be set to 0b1. The data bit width (12 bits, 10 bits, or 8 bits) must be set to with 0x16[5:4].

The 1<sup>st</sup> or the 2<sup>nd</sup> edge can be the rising or falling edge. The data input edge is defined in 0x16[1]. 0b0 = rising edge; 0b1 = falling edge. Pixel 0 is the first pixel of the 4:2:2 word and should be where DE starts.

**Table 16.**

| Input Format                        | Data[23:0]            |    |                      |    |                      |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|-------------------------------------|-----------------------|----|----------------------|----|----------------------|----|---------|----|----------|----|---------|----|----------|----|--------|---|---|---|---|---|---|---|---|---|
|                                     | 23                    | 22 | 21                   | 20 | 19                   | 18 | 17      | 16 | 15       | 14 | 13      | 12 | 11       | 10 | 9      | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>Style 1</b>                      |                       |    |                      |    |                      |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Syncs (DDR) 12-bit | 1 <sup>st</sup> Pixel |    | 2 <sup>nd</sup> Edge |    | 1 <sup>st</sup> Edge |    | Y[7:4]  |    |          |    | Cb[3:0] |    |          |    | Y[3:0] |   |   |   |   |   |   |   |   |   |
|                                     |                       |    |                      |    | Cb[11:4]             |    |         |    | Y[11:8]  |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | 2 <sup>nd</sup> Pixel |    | Y[7:4]               |    |                      |    | Cr[3:0] |    |          |    | Y[3:0]  |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     |                       |    | Cr[11:4]             |    |                      |    | Y[11:8] |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Syncs (DDR) 10-bit | Y[5:4]                |    |                      |    | Cb[3:0]              |    |         |    | Y[3:0]   |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[9:4]               |    |                      |    | Y[9:6]               |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[5:4]                |    |                      |    | Cr[3:0]              |    |         |    | Y[3:0]   |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cr[9:4]               |    |                      |    | Y[9:6]               |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
| YCbCr 4:2:2 Sep. Syncs (DDR) 8-bit  | Cb[3:0]               |    |                      |    | Y[3:0]               |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[7:4]               |    |                      |    | Y[7:4]               |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cr[3:0]               |    |                      |    | Y[3:0]               |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cr[7:4]               |    |                      |    | Y[7:4]               |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
| <b>Style 2</b>                      |                       |    |                      |    |                      |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
| 12-bit                              | Y[11:0]               |    |                      |    | Cb[11:0]             |    |         |    | Y[11:0]  |    |         |    | Cr[11:0] |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[9:0]                |    |                      |    | Cb[9:0]              |    |         |    | Y[9:0]   |    |         |    | Cr[9:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[7:0]                |    |                      |    | Cb[7:0]              |    |         |    | Y[7:0]   |    |         |    | Cr[7:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[5:0]                |    |                      |    | Cb[5:0]              |    |         |    | Y[5:0]   |    |         |    | Cr[5:0]  |    |        |   |   |   |   |   |   |   |   |   |
| 10-bit                              | Y[9:0]                |    |                      |    | Cb[9:0]              |    |         |    | Y[9:0]   |    |         |    | Cr[9:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[7:0]                |    |                      |    | Cb[7:0]              |    |         |    | Y[7:0]   |    |         |    | Cr[7:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[5:0]                |    |                      |    | Cb[5:0]              |    |         |    | Y[5:0]   |    |         |    | Cr[5:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[3:0]                |    |                      |    | Cb[3:0]              |    |         |    | Y[3:0]   |    |         |    | Cr[3:0]  |    |        |   |   |   |   |   |   |   |   |   |
| 8-bit                               | Y[7:0]                |    |                      |    | Cb[7:0]              |    |         |    | Y[7:0]   |    |         |    | Cr[7:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[5:0]                |    |                      |    | Cb[5:0]              |    |         |    | Y[5:0]   |    |         |    | Cr[5:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[3:0]                |    |                      |    | Cb[3:0]              |    |         |    | Y[3:0]   |    |         |    | Cr[3:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Y[1:0]                |    |                      |    | Cb[1:0]              |    |         |    | Y[1:0]   |    |         |    | Cr[1:0]  |    |        |   |   |   |   |   |   |   |   |   |
| <b>Style 3</b>                      |                       |    |                      |    |                      |    |         |    |          |    |         |    |          |    |        |   |   |   |   |   |   |   |   |   |
| 12-bit                              | Cb[11:0]              |    |                      |    | Y[11:0]              |    |         |    | Cr[11:0] |    |         |    | Y[11:0]  |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[9:0]               |    |                      |    | Y[9:0]               |    |         |    | Cr[9:0]  |    |         |    | Y[9:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[7:0]               |    |                      |    | Y[7:0]               |    |         |    | Cr[7:0]  |    |         |    | Y[7:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[5:0]               |    |                      |    | Y[5:0]               |    |         |    | Cr[5:0]  |    |         |    | Y[5:0]   |    |        |   |   |   |   |   |   |   |   |   |
| 10-bit                              | Cb[9:0]               |    |                      |    | Y[9:0]               |    |         |    | Cr[9:0]  |    |         |    | Y[9:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[7:0]               |    |                      |    | Y[7:0]               |    |         |    | Cr[7:0]  |    |         |    | Y[7:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[5:0]               |    |                      |    | Y[5:0]               |    |         |    | Cr[5:0]  |    |         |    | Y[5:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[3:0]               |    |                      |    | Y[3:0]               |    |         |    | Cr[3:0]  |    |         |    | Y[3:0]   |    |        |   |   |   |   |   |   |   |   |   |
| 8-bit                               | Cb[7:0]               |    |                      |    | Y[7:0]               |    |         |    | Cr[7:0]  |    |         |    | Y[7:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[5:0]               |    |                      |    | Y[5:0]               |    |         |    | Cr[5:0]  |    |         |    | Y[5:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[3:0]               |    |                      |    | Y[3:0]               |    |         |    | Cr[3:0]  |    |         |    | Y[3:0]   |    |        |   |   |   |   |   |   |   |   |   |
|                                     | Cb[1:0]               |    |                      |    | Y[1:0]               |    |         |    | Cr[1:0]  |    |         |    | Y[1:0]   |    |        |   |   |   |   |   |   |   |   |   |

## 4:2:2 TO 4:4:4 DATA CONVERSION

The AD9389 has the ability to convert YCbCr video from 4:4:4 to 4:2:2 and 4:2:2 to 4:4:4. To convert from 4:4:4 to 4:2:2, the video data goes through a filter first to remove any artificial downsampling noise. To convert from 4:2:2 to 4:4:4, the AD9389 utilizes either the zero-order upconversion (pixel repetition) or first-order upconversion (linear interpolation). The upconversion and downconversions are used when the video output timing format does not match the video input timing format. The video output format is set by Register 0x16[7:6]. The video input format is set by the video ID (0x15[3:1]) and video color space (0x16[0]). The default mode for upconversion is pixel repetition. To use linear interpolation, set Register 0x17[2] to 1.

## HORIZONTAL SYNC, VERTICAL SYNC, AND DE GENERATION

When transmitting video data across the TMDS interface, it is necessary to have an HSYNC, VSYNC, and data enable (DE) defined for the image. ITU-656 based sources have start of active video (SAV) and end of active video (EAV) signals built in, but the HSYNC and VSYNC must be generated (the DE is implied by the SAV and EAV signals). Other sources (with separate syncs) have HSYNC, VSYNC, and DE supplied at the same time as the pixel data.

## DE GENERATION

The AD9389 offers a choice of DE from an external pin, or an internally generated DE. To activate the internal DE generation, set Register 0x17[0] to 1. Registers 0x35 to 0x3A are used to define the DE. 0x35 and 0x36[7:6] define the number of pixels from the HS leading edge to the DE leading edge. 0x36[5:0] are the number of HSYNCs between the leading edge of VS and DE. 0x37[7:5] defines the difference of HS counts during VS blanking for interlace video. 0x37[4:0] and 0x38[7:1] indicate the width of the DE. 0x39 and 0x3A[7:4] are the number of lines of active video (see Figure 4).

## HSYNC AND VSYNC GENERATION

For video with embedded HSYNC and VSYNC, such as EAV and SAV, found in ITU 656 format, it is necessary to reconstruct HSYNC and VSYNC. This is done with registers 0x30 to 0x34. 0x30 and 0x31[7:6] specify the number of pixels between the HSYNC leading edge and the trailing edge of DE. Register 0x31[5:0] and Register 0x32[7:4] are the duration of the HSYNC in pixel clocks. 0x32[3:0] and 0x33[7:2] are the number of HS pulses between the trailing edge of the last DE and the leading edge of the VSYNC pulse. Register 0x33[1:0] and 0x34[7:0] are the duration of VSYNC in units of HSYNCs. HSYNC and VSYNC polarity can be specified by setting 0x17[6] (for VSYNC) and 0x17[5] (for HSYNC).

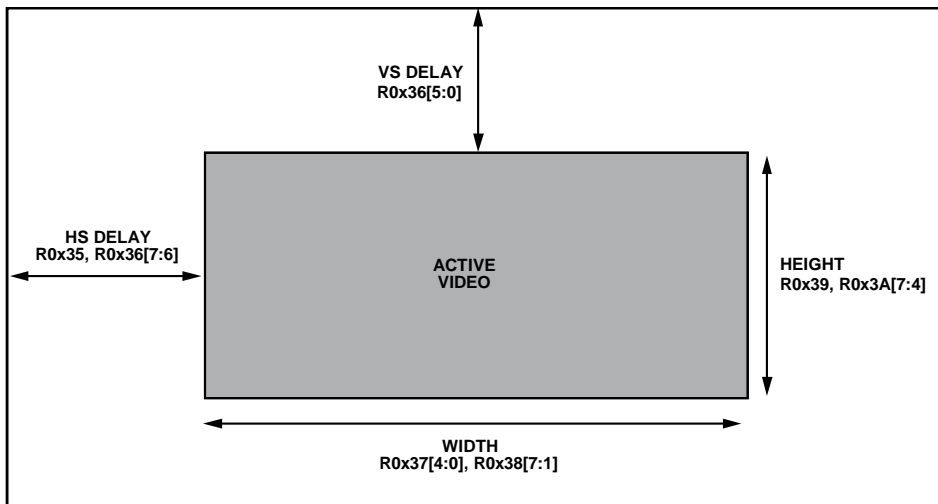


Figure 4. Active Video

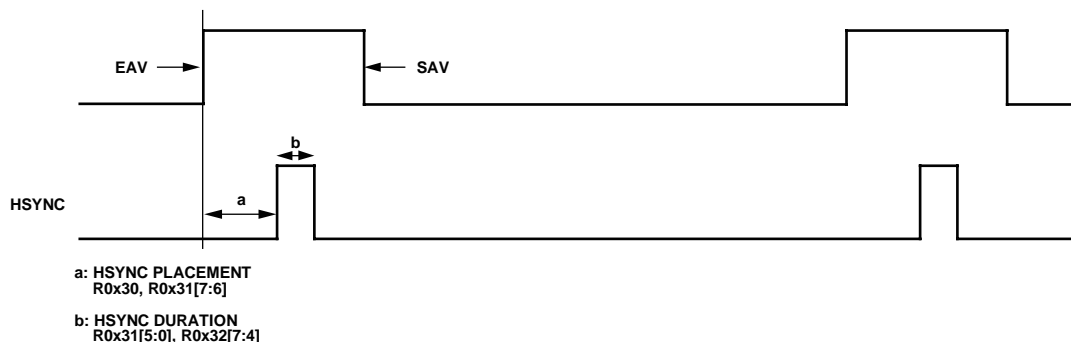


Figure 5. HSYNC Reconstruction

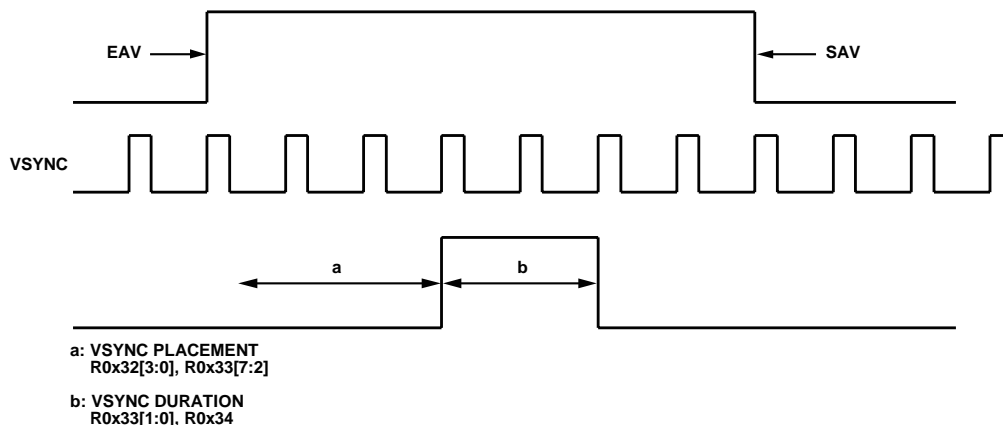


Figure 6. VSYNC Reconstruction

05724-006

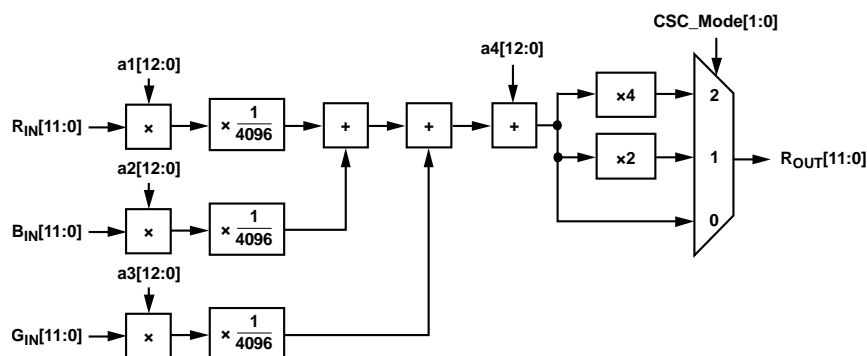


Figure 7. Single CSC Channel

05724-008

### COLOR SPACE CONVERSION MATRIX (CSC)

The color space conversion matrix in the AD9389 consists of three identical processing channels. In each channel, three input values are multiplied by three separate coefficients. Also included are an offset value for each row of the matrix and a scaling multiple for all values. Each value is 13-bit, two's complement resolution to ensure the signal integrity is maintained. The CSC is designed to run at speeds up to 80 MHz supporting resolutions up to 1080i at 60 Hz and UXGA at 60 Hz. With any-to-any color space support, RGB, YUV, YCbCr, and other formats are supported by the CSC.

The main inputs,  $R_{IN}$ ,  $G_{IN}$ , and  $B_{IN}$  come from the 8-bit to 12-bit inputs from each channel. These inputs are based on the input format detailed in Table 10 to Table 16. The mapping of these inputs to the CSC inputs is shown in Table 17.

Table 17. CSC Port Mapping

| Input Channel | CSC Input Channel |
|---------------|-------------------|
| R/Cr          | $R_{IN}$          |
| Gr/Y          | $G_{IN}$          |
| B/Cb          | $B_{IN}$          |

One of the three channels is represented in Figure 7. In each processing channel, the three inputs are multiplied by three separate coefficients marked  $a_1$ ,  $a_2$ , and  $a_3$ . These coefficients are divided by 4096 to obtain nominal values ranging from  $-0.9998$  to  $+0.9998$ . The variable labeled  $a_4$  is used as an offset control. The  $CSC\_Mode$  setting is the same for all three processing channels. This multiplies all coefficients and offsets by a factor of  $2^{CSC\_Mode}$ .

The functional diagram for a single channel of the CSC, as per Figure 7, is repeated for the remaining G and B channels. The coefficients for these channels are  $b_1$ ,  $b_2$ ,  $b_3$ ,  $b_4$ ,  $c_1$ ,  $c_2$ ,  $c_3$ , and  $c_4$ .

Register settings for several common conversions are listed in the Color Space Converter (CSC) Common Settings section.

For a detailed functional description and more programming examples, refer to [AN-795, The AD9880 Color Space Converter User's Guide](#).

## AUDIO DATA CAPTURE

The AD9389 is capable of receiving audio data in either I<sup>2</sup>S or S/PDIF format for packetization and transmission over the HDMI interface.

### I<sup>2</sup>S AUDIO

The AD9389 can accommodate from two to eight channels of I<sup>2</sup>S audio at up to a 192 kHz sampling rate. Selection of I<sup>2</sup>S audio mode (vs. S/PDIF) is set with 0x0A[4] = 0. The detected sampling frequency (from 32 kHz to 192 kHz) can be read in 0x04[7:4]. The output sampling frequency (from 32 kHz to 192 kHz) can be selected with 0x15[7:4]. The number of channels and the specific channels can be selected in 0x0C[5:2] and 0x50[7:5]. If all eight channels (I<sup>2</sup>S0 to I<sup>2</sup>S3) are required, setting all bits or 0x0C[5:2] to 1 selects eight channels. If I<sup>2</sup>S0 only is needed, setting 0x0C[2] to 1 selects this. The placement of these packets with respect to their output can be specified in Register 0x0E to Register 0x11. Default settings place all channels in their respective position (I<sup>2</sup>S0 left channel in Channel 0 left position, I<sup>2</sup>S3 right channel in Channel 3 right position), but this mapping is completely programmable.

The AD9389 supports standard I<sup>2</sup>S, left-justified I<sup>2</sup>S, and right-justified I<sup>2</sup>S formats via 0x0C[1:0] and sample word lengths between 16 bits and 24 bits (0x14[3:0]).

### S/PDIF AUDIO

The AD9389 is capable of accepting two channel LPCM and encoded audio up to a 192 kHz sampling rate via the S/PDIF. S/PDIF audio input is selected by setting 0x0A[4] = 1. The AD9389 is capable of accepting S/PDIF with or without an MCLK input. When no MCLK is present, the AD9389 makes the determination of the CTS value (N/CTS determines the MCLK frequency).

### CTS GENERATION

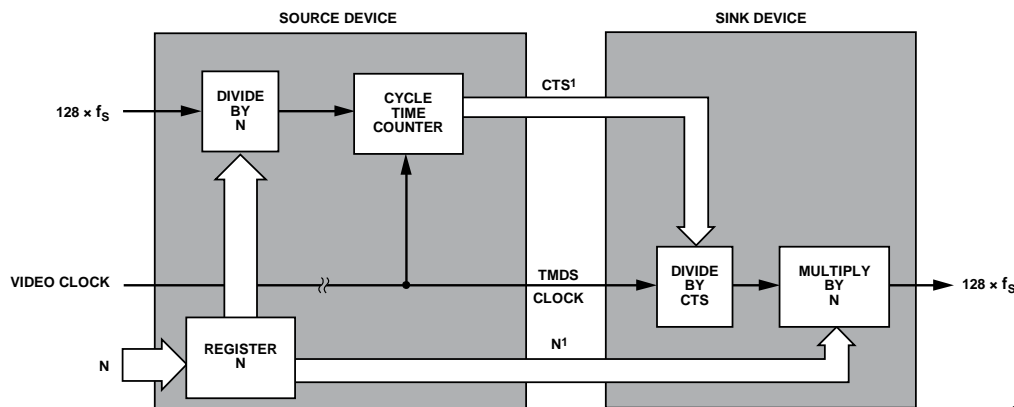
Audio data being carried across the HDMI link, which is driven by a TMDS (video) clock only, does not retain the original audio sample clock.

The task of recreating this clock at the sink is called audio clock regeneration. There are a variety of clock regeneration methods that can be implemented in an HDMI sink, each with a different set of performance characteristics. The HDMI specification does not attempt to define exactly how these mechanisms operate. It does, however, present a possible configuration and it does define the data items that the HDMI source supplies to the HDMI sink in order to allow the HDMI sink to adequately regenerate the audio clock. It also defines how that data is generated. In many video source devices, the audio and video clocks are generated from a common clock (coherent clocks). In this situation, there exists a rational (integer divided by integer) relationship between these two clocks. The HDMI clock regeneration architecture can take advantage of this rational relationship and can also work in an environment where there is no such relationship between these two clocks, that is, where the two clocks are truly asynchronous or where their relationship is unknown.

Figure 8 shows the system architecture model used by HDMI for audio clock regeneration. The source determines the fractional relationship between the video clock and an audio reference clock ( $128 \times$  audio sample rate) and passes the numerator and denominator for that fraction to the sink across the HDMI link. The sink can then recreate the audio clock from the TMDS clock by using a clock divider and a clock multiplier. The exact relationship between the two clocks is

$$128 \times f_s = f_{TMDS\_clock} \times N/CTS$$

The source determines the value of the numerator N as stated in Section 7.2.1 of the HDMI specification. Typically, this value N is used in a clock divider to generate an intermediate clock that is slower than the  $128 \times f_s$  clock by the factor N. The source typically determines the value of the denominator cycle time stamp (CTS) by counting the number of TMDS clocks in each of the  $128 \times f_s/N$  clocks.



<sup>1</sup>N AND CTS VALUES ARE TRANSMITTED USING THE "AUDIO CLOCK REGENERATION" PACKET. VIDEO CLOCK IS TRANSMITTED ON TMDS CLOCK CHANNEL.

Figure 8. Audio Clock Regeneration



**N PARAMETER**

N shall be an integer number that meets the following restriction:  $128 \times f_s/1500 \text{ Hz} \leq N \leq 128 \times f_s/300 \text{ Hz}$  with a recommended optimal value of  $128 \times f_s/1000 \text{ Hz}$  equals N. For coherent audio and video clock sources, use Table 18 to Table 20 to determine the value of N. For noncoherent sources or sources where coherency is not known, use the equations previously described.

**CTS PARAMETER**

CTS is an integer number that satisfies the following:

$$(\text{Average CTS Value}) = (f_{\text{TMDs\_clock}} \times N) / (128 \times f_s)$$

**Recommended N and Expected CTS Values**

The recommended value of N for several standard pixel clocks is given in Table 18 to Table 20. It is recommended that sources with noncoherent clocks use the values listed for the pixel clock type labeled Other.

**Table 18. Recommended N and Expected CTS Values for 32 kHz Audio**

| Pixel Clock (MHz) | 32 kHz |                               |
|-------------------|--------|-------------------------------|
|                   | N      | CTS                           |
| 25.1/1.001        | 4576   | 28125                         |
| 25.2              | 4096   | 25200                         |
| 27                | 4096   | 27000                         |
| 27 × 1.001        | 4096   | 27027                         |
| 54                | 4096   | 54000                         |
| 54 × 1.001        | 4096   | 54054                         |
| 74.25/1.001       | 11648  | 210937 to 210938 <sup>1</sup> |
| 74.25             | 4096   | 74250                         |
| 148.5/1.001       | 11648  | 421875                        |
| 148.5             | 4096   | 148500                        |
| Other             | 4096   | Measured                      |

<sup>1</sup> This value alternates because of the restriction on N.

**Table 19. Recommended N and Expected CTS Values for 44.1 kHz Audio and Multiples**

| Pixel Clock (MHz) | 44.1 kHz |          | 88.2 kHz |          | 176.4 kHz |          |
|-------------------|----------|----------|----------|----------|-----------|----------|
|                   | N        | CTS      | N        | CTS      | N         | CTS      |
| 25.1/1.001        | 7007     | 31250    | 14014    | 31250    | 28028     | 31250    |
| 25.2              | 6272     | 28000    | 12544    | 28000    | 25088     | 28000    |
| 27                | 6272     | 3000     | 12544    | 30000    | 25088     | 30000    |
| 27 × 1.001        | 6272     | 30030    | 12544    | 30030    | 25088     | 30030    |
| 54                | 6272     | 60000    | 12544    | 60000    | 25088     | 60000    |
| 54 × 1.001        | 6272     | 60060    | 12544    | 60060    | 25088     | 60060    |
| 74.25/1.001       | 17836    | 234375   | 35672    | 234375   | 71344     | 234375   |
| 74.25             | 6272     | 82500    | 12544    | 82500    | 25088     | 82500    |
| 148.5/1.001       | 8918     | 234975   | 17836    | 234375   | 35672     | 123375   |
| 148.5             | 6272     | 165000   | 12544    | 16500    | 25088     | 162000   |
| Other             | 6272     | Measured | 15244    | Measured | 25088     | Measured |

**Table 20. Recommended N and Expected CTS Values for 48 kHz Audio and Multiples**

| Pixel Clock (MHz) | 44.1 kHz |          | 88.2 kHz |          | 176.4 kHz |          |
|-------------------|----------|----------|----------|----------|-----------|----------|
|                   | N        | CTS      | N        | CTS      | N         | CTS      |
| 25.1/1.001        | 6864     | 28125    | 13728    | 28125    | 27456     | 28125    |
| 25.2              | 6144     | 25200    | 12288    | 25200    | 24576     | 25200    |
| 27                | 6144     | 27000    | 12288    | 27027    | 24576     | 27027    |
| 27 × 1.001        | 6144     | 27027    | 12288    | 27027    | 24576     | 27027    |
| 54                | 6144     | 54000    | 12288    | 54000    | 24576     | 54000    |
| 54 × 1.001        | 6144     | 54054    | 12288    | 54054    | 24576     | 74250    |
| 74.25/1.001       | 11648    | 140625   | 23296    | 140625   | 46592     | 140625   |
| 74.25             | 6144     | 74250    | 12288    | 74250    | 24576     | 74250    |
| 148.5/1.001       | 5824     | 140625   | 11648    | 140625   | 23296     | 140625   |
| 148.5             | 6144     | 148500   | 12288    | 148500   | 24576     | 148500   |
| Other             | 6144     | Measured | 12288    | Measured | 24576     | Measured |

# AD9389

The AD9389 has two modes for CTS generation: manual mode and auto mode. In manual mode, the user can program the CTS number directly into the chip (0x07 to 0x09) and select this external mode by setting 0x0A[7] to 1. In auto mode, the chip computes the CTS based on the actual audio and video rates. This can be selected by setting 0x0A[7] to 0, and the results can be read from 0x04 to 0x06. Manual mode is good for coherent audio and video, where the audio and video clock are generated from the same crystal; thus CTS should be a fixed number. The auto mode is appropriate for incoherent audio-video, where there is no simple integer ratio between the audio and video clock. A filter is available (0x0A[6:5]) to stabilize the chip generated CTS. The 20-bit N value can be programmed into the AD9389 in Register 0x01 to Register 0x03.

## PACKET CONFIGURATION

The AD9389 supports all the packets listed in the HDMI 1.1 specification. Each packet can be separately enabled and disabled. Based on the audio and video input, the packets are added to the HDMI link at the earliest time, so that a minimum delay is incurred. Notice the ISRC1 packet has one bit to enable the ISRC2 packet. For the general control packet, remember to clear or reset the bits to avoid system lock-up.

## PIXEL REPETITION

Due to HDMI specification and bandwidth requirements, sometimes it is necessary to set clock multiplication by 2× and 4× in order to maintain the minimum TMDS clock frequency. The AD9389 offers three choices for the user to implement this function: auto mode, manual mode, and max mode (0x3B[6:5]).

For the auto mode (0x3B[6:5] = 00), based on the input video format (either programmed by user, or chip detection) and audio sampling rate, the AD9389 automatically sets the pixel repetition factor (0x3D[7:6]).

For manual mode (0x3B[6:5] = 1×), the user programs the pixel repetition factor in 0x3B[4:3].

For max mode (0x3B[6:5] = 01), based on the input video format, the AD9389 selects the maximum repetition factor. The advantage of the max mode is that it is independent of the audio sampling rate.

**Table 21. Pixel Repetition—Valid Pixel Repeat Values for Each Format**

| Video Code | Video Description             | EIA/CEA-861B Pixel Repeat Values | HDMI Pixel Repeat Values             |
|------------|-------------------------------|----------------------------------|--------------------------------------|
| 1          | 640 × 480p @ 60 Hz            | No repetition                    | No repetition                        |
| 2, 3       | 720 × 480p @ 59.94/60 Hz      | No repetition                    | No repetition                        |
| 4          | 1280 × 720p @ 59.94/60 Hz     | No repetition                    | No repetition                        |
| 5          | 1920 × 1080i @ 59.94/60 Hz    | No repetition                    | No repetition                        |
| 6, 7       | 720/1440 × 480i @ 59.94/60 Hz | Pixel sent 2 times               | Pixel sent 2 times                   |
| 8, 9       | 720/1440 × 240p @ 59.94/60 Hz | Pixel sent 2 times               | Pixel sent 2 times                   |
| 10, 11     | 2880 × 480i @ 59.94/60 Hz     | Pixel sent 0 to 10 times         | Pixel sent 1 to 10 times             |
| 12, 13     | 2880 × 240p @ 59.94/60 Hz     | Pixel sent 1 to 10 times         | Pixel sent 1 to 10 times             |
| 14, 15     | 1440 × 480p @ 59.94/60 Hz     | No repetition                    | Pixel sent 1 to 2 times <sup>1</sup> |
| 16         | 1920 × 1080p @ 59.94/60 Hz    | No repetition                    | No repetition                        |
| 17, 18     | 720 × 576p @ 50 Hz            | No repetition                    | No repetition                        |
| 19         | 1280 × 720p @ 50 Hz           | No repetition                    | No repetition                        |
| 20         | 1920 × 1080i @ 50 Hz          | No repetition                    | No repetition                        |
| 21, 22     | 720/1440 × 576i @ 50 Hz       | Pixel sent 2 times               | Pixel sent 2 times                   |
| 23, 24     | 720/1440 × 288p @ 50 Hz       | Pixel sent 2 times               | Pixel sent 2 times                   |
| 25, 26     | 2880 × 576i @ 50 Hz           | Pixel sent 1 to 10 times         | Pixel sent 1 to 10 times             |
| 27, 28     | 2880 × 288 @ 50 Hz            | Pixel sent 1 to 10 times         | Pixel sent 1 to 10 times             |
| 29, 30     | 1440 × 576p @ 50 Hz           | No repetition                    | Pixel sent 1 to 2 times <sup>1</sup> |
| 31         | 1920 × 1080p @ 50 Hz          | No repetition                    | No repetition                        |
| 32         | 1920 × 1080p @ 23.97/24 Hz    | No repetition                    | No repetition                        |
| 33         | 1920 × 1080p @ 25 Hz          | No repetition                    | No repetition                        |
| 34         | 1920 × 1080p @ 29.9/30 Hz     | No repetition                    | No repetition                        |

<sup>1</sup> Denotes change from EIA/CEA-861B valid values. Pixel repetition is required to support some audio formats at 720 × 480p and 720 × 576p video format timings.

## HDCP HANDLING

The AD9389 has a built-in microcontroller to handle HDCP transmitter states, including handling downstream HDCP repeaters. To activate HDCP from a system level, the main controller needs to set 0xAF[7] to 1 to inform AD9389 that the video stream should be encrypted. The AD9389 takes control from there, and implements all remaining tasks defined by the HDCP 1.1 specification.

The system controller should monitor the status of HDCP by reading Register 0xB8[6] (indicating the HDCP link has been established). There are also some error flags (0xC5[7] and 0xC8[7:4]) to help debug the system.

The AD9389 also supports AV functions to suspend HDCP temporarily. To set AV mute, clear 0x45[7] and set 0x45[6] to 1. To clear AV mute, clear 0x45[6] and set 0x45[7] to 1. (Note that it is invalid to set the two mute bits at the same time.)

For more information, refer to application note AN-810, EDID and HDCP Controller User Guide for the AD9889.

## EDID READING

The AD9389 has an I<sup>2</sup>C master (DDC Pin 44 and Pin 45) to read the EDID based on system need. It buffers segment 0 once HPD is detected. The system can request other segments by programming Register 0xC4. An interrupt bit (0x96[2]) indicates the completion of EDID rebuffering.

To read the EDID data from the AD9389, use the AD9389 programming bus (Pin 46 and Pin 47) with I<sup>2</sup>C Address 0x7E. This is the default address but can be changed by writing the desired address into Register 0x43.

For more information, refer to Application Note AN-810, *EDID and HDCP Controller User Guide for the AD9889*.

## INTERRUPTS

The AD9389 has interrupts to help with the system design: hot plug detection, receiver sense, VS detection, audio FIFO overflow, ITU 656 error, EDID ready, HDCP error, and BKS ready. Interrupts can be cleared by writing 1 into the interrupt register (0x96, 0x97). There are read-only registers (0xC5, 0xC6) to show the state of these signals. Masks (0x94, 0x95) are available to let the user selectively activate each interrupt. To enable a specific interrupt register, write 1 to the corresponding mask bit.

## POWER MANAGEMENT

The AD9389 power-down pin polarity depends on the AD9389's I<sup>2</sup>C address selection. To use 0x72, the PD pin is high active. To use 0x7A, the PD pin is low active. The power-down pin polarity can be verified by reading Register 0x42[7].

The AD9389 can be powered down or reset either by Pin 33 or by Register 0x41[6]. During power-down mode, all the circuits are inactive except the I<sup>2</sup>C slave and some circuits related to mode and activity detection. During power-down mode, the chip status can still be read through the I<sup>2</sup>C slave. To enter normal power-down mode, either drive Pin 33 to 1, or set 0x41[6] to 1. To further reduce power consumption, disable the receiver sense detection by setting Register 0xA4[2] to 1.

For HDCP security reasons, the I<sup>2</sup>C power-down bit is also reset by the power-down pin. Anytime after power down, the user needs to drive the PD pin back to 0, and set 0x41[6] to 0 to activate the chip.

## 2-WIRE SERIAL REGISTER MAP

The AD9389 is initialized and controlled by a set of registers that determine the operating modes. An external controller is employed to write and read the control registers through the two-line serial interface port.

**Table 22. Control Register Map**

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name         | Description   |
|-------------|-------------------------|-------|---------------|-----------------------|---|
| 0x00        | Read                    | [7:0] | 00000000      | Chip Revision         | Revision of the chip, start from 0.   |
| 0x01        | Read/Write              | [3:0] | ****0000      | N[19:16]              | 20-bit N used with cycle time stamp (CTS) (see Table 18 to Table 20 for appropriate settings) to regenerate the audio clock in the receiver. For remaining bits, see 0x02 and 0x03. Used only with I <sup>2</sup> S audio, not S/PDIF.  |
| 0x02        | Read/Write              | [7:0] | 00000000      | N[15:8]               | The middle byte of N.   |
| 0x03        | Read/Write              | [7:0] | 00000000      | N[7:0]                | The lower byte of N.  |
| 0x04        | Read                    | [7:4] | 0000****      | S/PDIF_SF             | S/PDIF sampling frequency for S/PDIF audio decoded from hardware. This information is used both by the audio Rx and the pixel repetition.<br>0011 = 32 kHz.<br>0000 = 44.1 kHz.<br>0010 = 48 kHz.<br>1000 = 88.2 kHz.<br>1010 = 96 kHz.<br>1100 = 176.4 kHz.<br>1110 = 192 kHz.<br>Default = 0x0. |
|             |                         | [3:0] | ****0000      | CTS_Int[19:16]        | CTS measured (internal). This 20-bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits, see 0x05 and 0x06.  |
| 0x05        | Read                    | [7:0] | 00000000      | CTS_Int[15:8]         | Middle byte of measured CTS.  |
| 0x06        | Read                    | [7:0] | 00000000      | CTS_Int[7:0]          | Low byte of measured CTS.   |
| 0x07        | Read/Write              | [3:0] | ****0000      | CTS_Ext[19:16]        | CTS (external). This 20-bit value is used in the receiver with the N value to regenerate an audio clock. For remaining bits, see 0x08 and 0x09.   |
| 0x08        | Read/Write              | [7:0] | 00000000      | CTS_Ext[15:8]         | Middle byte of external CTS.  |
| 0x09        | Read/Write              | [7:0] | 00000000      | CTS_Ext[7:0]          | Low byte of external CTS.   |
| 0x0A        | Read/Write              | [7]   | 0*****        | CTS_Sel               | CTS source select.<br>0 = internal CTS.<br>1 = external CTS.<br>Default = 0.  |
|             |                         | [6:5] | *10*****      | Avg_Mode              | CTS filter mode.<br>00 = no filter.<br>01 = divide by 4.<br>10 = divide by 8.<br>11 = divide by 16.<br>Default = 10.  |
|             |                         | [4]   | ***0****      | Audio_Sel             | Audio type select.<br>0 = I <sup>2</sup> S.<br>1 = S/PDIF.<br>Default = 0.  |
|             |                         | [3]   | ****0***      | MCLK_SP               | MCLK for S/PDIF.<br>1 = MCLK active.<br>0 = MCLK inactive.<br>Default = 0.  |
|             |                         | [2]   | *****0**      | MCLK_I <sup>2</sup> S | MCLK for I <sup>2</sup> S.<br>1 = I <sup>2</sup> S MCLK active.<br>0 = I <sup>2</sup> S MCLK inactive.<br>Default = 0.  |
|             |                         | [1:0] | *****01       | MCLK_Ratio            | MCLK ratio.   |

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name              | Description  |
|-------------|-------------------------|-------|---------------|----------------------------|--|
|             |                         |       |               |                            | 00 = $\times 128 f_s$ .<br>01 = $\times 256 f_s$ .<br>10 = $\times 384 f_s$ .<br>11 = $\times 512 f_s$ .<br>Default = 01.  |
| 0x0B        | Read/Write              | [6]   | **0*****      | MCLK_Pol                   | MCLK polarity.<br>0 = rising edge.<br>1 = falling edge.<br>Default = 0.  |
|             |                         | [5]   | **0*****      | Flat_Line                  | Flat line.<br>1 = flat line audio (audio sample not valid).<br>0 = normal.<br>Default = 0.   |
|             |                         | [4:0] | ****0111      | Test bits                  | Must be set to 0x7 for proper operation.   |
| 0x0C        | Read/Write              | [5:2] | **1111**      | I <sup>2</sup> S enable    | I <sup>2</sup> S enable for the four I <sup>2</sup> S pins (active).<br>0001 = I <sup>2</sup> S0.<br>0010 = I <sup>2</sup> S1.<br>0100 = I <sup>2</sup> S2.<br>1000 = I <sup>2</sup> S3.<br>Default = 1111 for all.        |
|             |                         | [1:0] | *****00       | I <sup>2</sup> S Format    | I <sup>2</sup> S format.<br>00 = standard I <sup>2</sup> S mode.<br>01 = right-justified I <sup>2</sup> S mode.<br>10 = left-justified I <sup>2</sup> S mode.<br>11 = raw IEC60958 mode.<br>Default = 0.                   |
| 0x0D        | Read/Write              | [4:0] | ***11000      | I <sup>2</sup> S_bit_width | I <sup>2</sup> S bit width. For right justified audio only. Default is 24. Not valid for widths greater than 24.   |
| 0x0E        | Read/Write              | [5:3] | **000***      | SUBPKT0_L_src              | Registers 0x0E to 0x11 should be set based on the speaker mapping information obtained from EDID. Source of sub packet 0, left channel. Default = 000.   |
|             |                         | [2:0] | *****001      | SUBPKT0_R_src              | Source of sub packet 0, right channel. Default = 001.  |
| 0x0F        | Read/Write              | [5:3] | **010***      | SUBPKT1_L_src              | Source of sub packet 1, left channel. Default = 010.   |
|             |                         | [2:0] | *****011      | SUBPKT1_R_src              | Source of sub packet 1, right channel. Default = 011.  |
| 0x10        | Read/Write              | [5:3] | **100***      | SUBPKT2_L_src              | Source of sub packet 2, left channel. Default = 100.   |
|             |                         | [2:0] | *****101      | SUBPKT2_R_src              | Source of sub packet 2, right channel. Default = 101.  |
| 0x11        | Read/Write              | [5:3] | **110***      | SUBPKT3_L_src              | Source of sub packet 3, left channel. Default = 110.   |
|             |                         | [2:0] | *****111      | SUBPKT3_R_src              | Source of sub packet 3, right channel. Default = 111.  |
| 0x12        | Read/Write              | [5]   | **0*****      | CR_bit                     | Copyright bit.<br>0 = copyright.<br>1 = not copyright protected.   |
|             |                         | [4:2] | ***000**      | a_info                     | Additional information for channel status bits.<br>000 = 2 audio channels without pre-emphasis.<br>100 = 2 audio channels with 50/15 $\mu$ s pre-emphasis.<br>010 = reserved.<br>110 = reserved.<br>Default = 000.         |
|             |                         | [1:0] | *****00       | Clk_Acc                    | Clock accuracy.<br>00 = Level II, normal accuracy $\pm 1000 \times 10^{-6}$ .<br>01 = Level III, variable pitch shifted clock.<br>10 = Level I, high accuracy $\pm 50 \times 10^{-6}$ .<br>11 = reserved.<br>Default = 00. |
| 0x13        | Read/Write              | [7:0] | 00000000      | Category Code              | Category code for audio infoframe; see IEC 60958.  |

# AD9389

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name       | Description   |
|-------------|-------------------------|-------|---------------|---------------------|---|
| 0x14        | Read/Write              | [7:4] | 0000****      | Source Number       | Source number.  |
|             |                         | [3:0] | ****0000      | Word Length         | Audio word length.<br>0000 = not specified.<br>0100 = 16 bits.<br>0011 = 17 bits.<br>0010 = 18 bits.<br>0001 = 19 bits.<br>0101 = 20 bits.<br>1000 = not specified.<br>1100 = 20 bits.<br>1011 = 21 bits.<br>1010 = 22 bits.<br>1001 = 23 bits.<br>1101 = 24 bits.<br>Default = 0x0.  |
| 0x15        | Read/Write              | [7:4] | 0000****      | I <sup>2</sup> S_SF | Sampling frequency for I <sup>2</sup> S audio. This information is used both by the audio Rx and the pixel repetition.<br>0011 = 32 kHz.<br>0000 = 44.1 kHz.<br>0010 = 48 kHz.<br>1000 = 88.2 kHz.<br>1010 = 96 kHz.<br>1100 = 176.4 kHz.<br>1110 = 192 kHz.<br>Default = 0x0.  |
|             |                         | [3:1] | ****000*      | VFE_input_id        | Input video format.<br>000 = RGB and YCbCr 4:4:4 (Y on Green).<br>001 = YCbCr 4:2:2; 16-bit, 20-bit, and 24-bit.<br>010 = Same as 001 with HS and VS embedded as SAV and EAV.<br>011 = ITU656 with separated syncs.<br>100 = ITU656 with embedded syncs.<br>101 = DDR RGB 4:4:4 or YCbCr 4:4:4.<br>110 = DDR YCbCr 4:2:2.<br>111 = undefined.<br>Default = 000. |
|             |                         | [0]   | *****0        | low_frq_video       | Video refresh rate.<br>0 = V <sub>REF</sub> > 30 Hz.<br>1 = V <sub>REF</sub> ≤ 30 Hz refresh rate video.<br>Default = 0.  |
| 0x16        | Read/Write              | [7:6] | 00*****       | VFE_out_fmt         | Video output format. This should be written along with 0x45[5:4].<br>00 = RGB 4:4:4.<br>01 = YCbCr 4:4:4.<br>1x = YCbCr 4:2:2.<br>Default = 00.   |
|             |                         | [5:4] | **00****      | VFE_422_width       | 4:2:2 input, could be either 8-bit, 10-bit, or 12-bit.<br>x0 = 12 bits.<br>01 = 10 bits.<br>11 = 8 bits.<br>Default = 00.   |
|             |                         | [3:2] | ****00**      | VFE_input_style     | Styles refer to the input pin assignments. See Table 23 to Table 28.<br>x0 = Style 1.<br>01 = Style 2.<br>11 = Style 3.   |

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name        | Description  |
|-------------|-------------------------|-------|---------------|----------------------|--|
|             |                         | [1]   | *****0*       | VFE_input_edge       | Video data input edge. Defines the first clock edge of video word clocked.<br>0 = rising edge.<br>1 = falling edge.<br>Default = 0 (in reference to DDR).  |
|             |                         | [0]   | *****0        | VFE_input_cs         | Video input color space.<br>0 = RGB.<br>1 = YCbCr.<br>Default = 0.   |
| 0x17        | Read/Write              | [7]   | 0*****        | itu_error_correct_en | ITU656 error correction. This must be enabled if using ITU656 format.<br>0 = disable.<br>1 = enable.<br>Default = 0.   |
|             |                         | [6]   | *0*****       | itu_vsync_pol        | VS polarity from regenerated ITU 656 input.<br>0 = high polarity.<br>1 = low polarity.<br>Default = 0.   |
|             |                         | [5]   | **0*****      | itu_hsync_pol        | HS polarity from regenerated ITU 656 input.<br>0 = high polarity.<br>1 = low polarity.<br>Default = 0.   |
|             |                         | [4:3] | ***00***      | csc_mode             | Sets the fixed point position of the CSC coefficients, including the a4, b4, and c4 offsets.<br>00 = $\pm 1.0$ , (from $-4096$ to $+4095$ ).<br>01 = $\pm 2.0$ , (from $-8192$ to $+8190$ ).<br>1x = $\pm 4.0$ , (from $-16,384$ to $+16,380$ ).<br>Default = 000.                                       |
|             |                         | [2]   | *****0**      | gen_444_en           | 4:2:2 to 4:4:4 upconversion mode.<br>1 = uses interpolation.<br>0 = no interpolation.<br>Default = 0.  |
|             |                         | [1]   | *****0*       | ASP_ratio            | Aspect ratio of input video.<br>0 = 4:3.<br>1 = 16:9.<br>Default = 0.  |
|             |                         | [0]   | *****0        | deGen_en             | Enable DE generator. The DE generator should be enabled when a DE input is not provided.<br>1 = enable DE generator.<br>Default = 0 (see Register 0x30 to Register 0x3A).  |
| 0x18        | Read/Write              | [4:0] | ***00110      | CSC_A1_MSB           | MSB of 0x19.   |
| 0x19        | Read/Write              | [7:0] | 01100010      | CSC_A1_LSB           | Color space converter (CSC) coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x1A        | Read/Write              | [4:0] | ***00100      | CSC_A2_MSB           | MSB of 0x1B.   |
| 0x1B        | Read/Write              | [7:0] | 10101000      | CSC_A2_LSB           | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$                         |
| 0x1C        | Read/Write              | [4:0] | ***00000      | CSC_A3_MSB           | MSB of 0x1D.   |
| 0x1D        | Read/Write              | [7:0] | 00000000      | CSC_A3_LSB           | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$                         |
| 0x1E        | Read/Write              | [4:0] | ***11100      | CSC_A4_MSB           | MSB of 0x1F.   |

# AD9389

| Hex Address | Read/Write or Read Only | Bits           | Default Value        | Register Name                    | Description  |
|-------------|-------------------------|----------------|----------------------|----------------------------------|--|
| 0x1F        | Read/Write              | [7:0]          | 10000100             | CSC_A4_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x20        | Read/Write              | [4:0]          | ***11100             | CSC_B1_MSB                       | MSB of 0x21.   |
| 0x21        | Read/Write              | [7:0]          | 10111111             | CSC_B1_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x22        | Read/Write              | [4:0]          | ***00100             | CSC_B2_MSB                       | MSB of 0x23.   |
| 0x23        | Read/Write              | [7:0]          | 10101000             | CSC_B2_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x24        | Read/Write              | [4:0]          | ***11110             | CSC_B3_MSB                       | MSB of 0x25.   |
| 0x25        | Read/Write              | [7:0]          | 01110000             | CSC_B3_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x26        | Read/Write              | [4:0]          | ***00010             | CSC_B4_MSB                       | MSB of 0x27.   |
| 0x27        | Read/Write              | [7:0]          | 00011110             | CSC_B4_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x28        | Read/Write              | [4:0]          | ***00000             | CDC_C1_MSB                       | MSB of 0x29.   |
| 0x29        | Read/Write              | [7:0]          | 00000000             | CSC_C1_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x2A        | Read/Write              | [4:0]          | ***00100             | CSC_C2_MSB                       | MSB of 0x2B.   |
| 0x2B        | Read/Write              | [7:0]          | 10101000             | CSC_C2_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x2C        | Read/Write              | [4:0]          | ***01000             | CSC_C3_MSB                       | MSB of 0x2D.   |
| 0x2D        | Read/Write              | [7:0]          | 00010010             | CSC_C3_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x2E        | Read/Write              | [4:0]          | ***11011             | CSC_C4_MSB                       | MSB of 0x2F.   |
| 0x2F        | Read/Write              | [7:0]          | 10101100             | CSC_C4_LSB                       | CSC coefficient for equation:<br>$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$<br>$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$<br>$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$ |
| 0x30        | Read/Write              | [7:0]          | 00000000             | VFE_hs_pla_MSB                   | Most significant 8 bits for HSYNC placement for ITU 656 HSYNC regeneration.  |
| 0x31        | Read/Write              | [7:6]<br>[5:0] | 00*****<br>**000000  | VFE_hs_pla_LSB<br>VFE_hs_dur_MSB | HSYNC placement lower 2 bits (see 0x30).<br>Most significant 6 bits for HSYNC duration.  |
| 0x32        | Read/Write              | [7:4]<br>[3:0] | 0000****<br>***00000 | VFE_hs_dur_LSB<br>VFE_vs_pla_MSB | HSYNC duration lower 4 bits (see 0x31).<br>Most significant 4 bits for VSYNC placement for ITU 656 VSYNC regeneration.   |
| 0x33        | Read/Write              | [7:2]<br>[1:0] | 000000**<br>*****00  | VFE_vs_pla_LSB<br>VFE_vs_dur_MSB | VSYNC placement lower 6 bits (see 0x32).<br>Most significant 2 bits for VSYNC duration.  |
| 0x34        | Read/Write              | [7:0]          | 00000000             | VFE_vs_dur_LSB                   | VSYNC duration lower 8 bits (see 0x33).  |
| 0x35        | Read/Write              | [7:0]          | 00000000             | VFE_hsDelayIn_MSB                | Most significant 8 bits for HSYNC delay in for ITU 656 HSYNC regeneration.   |



| Hex Address | Read/Write or Read Only | Bits                                  | Default Value  | Register Name   | Description   |
|-------------|-------------------------|---------------------------------------|--|---|---|
| 0x36        | Read/Write              | [7:6]<br>[5:0]                        | 00*****<br>**000000                                  | VFE_hsDelayIn_LSB<br>VFE_vsDelayIn                                  | HSYNC delay in lower 2 bits (see 0x35).<br>VSYNC delay in for DE generation.  |
| 0x37        | Read/Write              | [7:5]<br>[4:0]                        | 000*****<br>***00000                                 | Interlace Offset<br>VFE_width_MSB                                   | Sets the difference (in HSYNCs) in field length between Field 0 and Field 1.<br>Most significant 5 bits for frame width.  |
| 0x38        | Read/Write              | [7:1]                                 | 0000000*   | VFE_width   | Lower 7 bits for frame width (see 0x37).  |
| 0x39        | Read/Write              | [7:0]                                 | 00000000   | VFE_height_MSB  | Most significant 8 bits for frame height.   |
| 0x3A        | Read/Write              | [7:4]                                 | 0000****   | VFE_height  | Lower 4 bits for frame height (see 0x39).   |
| 0x3B        | Read/Write              | [7]<br>[6:5]<br>[4:3]<br>[2:1]<br>[0] | 1*****<br>*00*****<br>***00***<br>*****00*<br>*****0 | ext_audioSF_sel<br>pr_mode<br>ext_PLL_pr<br>ext_target_pr<br>csc_en | Audio sampling frequency select.<br>Valid when using S/PDIF input.<br>0 = $f_s$ extracted from SPDIF.<br>1 = $f_s$ set via 0x15[7:4].<br>Default = 1 (only used during pixel repetition mode).<br>Pixel repetition mode selection. Set to b00 unless nonstandard video is supported.<br>00 = auto mode.<br>01 = max mode.<br>1x = manual mode (see 0x3B Bits [4:3]).<br>Default = 00.<br>External value for PLL pixel repetition.<br>00 = $\times 1$ .<br>01 = $\times 2$ .<br>10 = $\times 4$ .<br>11 = $\times 4$ .<br>Default = 00.<br>User programmed pixel repetition number to send to Rx. Default = 00.<br>CSC enable.<br>0 = no CSC.<br>1 = enable CSC.<br>Default = 0. |
| 0x3C        | Read/Write              | [5:0]                                 | **000000   | ext_VID_to_Rx   | User programmed VID to send to Rx. See Table 24 for full VID formats. Default = 0x00.   |
| 0x3D        | Read                    | [7:6]<br>[5:0]                        | 00*****<br>**000000                                  | pr_to_Rx<br>VID_to_Rx   | The actual pixel repetition sent to Rx.<br>The actual VID sent to HDMI Rx (see Table 24).   |
| 0x3E        | Read                    | [7:2]                                 | 000000**   | VFE_fmt_VID   | VID detected by video FE (see Table 24).  |
| 0x3F        | Read                    | [7:5]<br>[4:3]                        | 000*****<br>***00***                                 | VFE_aux_vid<br>VFE_prog_mode  | This register is for video input formats that are not inside the 861B table.<br>000 = 480i not active.<br>001 = 240p not active.<br>010 = 576i not active.<br>011 = 288p not active.<br>100 = 480i active.<br>101 = 240p active.<br>110 = 576i active.<br>111 = 288p active.<br>Default = 000.<br>Information about 240p and 288p.<br>240p – 01 = 262 lines.<br>240p – 10 = 263 lines.<br>288p – 01 = 312 lines.<br>288p – 10 = 313 lines.<br>288p – 11 = 314 lines.<br>Default = 00.   |

# AD9389

| Hex Address | Read/Write or Read Only | Bits            | Default Value  | Register Name                    | Description   |
|-------------|-------------------------|-----------------|--|----------------------------------|---|
| 0x40        | Read/Write              | [7]             | 0*****   | GC_pkt_en                        | 1 = enable general control packet. Default = 0.   |
|             |                         | [6]             | *0*****  | SPD_pkt_en                       | 1 = enable source product descriptor packet. Default = 0.   |
|             |                         | [5]             | **0*****   | MPEG_pkt_en                      | 1 = enable MPEG packet. Default = 0.  |
|             |                         | [4]             | ***0****   | ACP_pkt_en                       | 1 = enable ACP packet. Default = 0.   |
|             |                         | [3]             | ****0***   | ISRC_pkt_en                      | 1 = enable ISRC packet. Default = 0.  |
| 0x41        | Read/Write              | [6]             | *1*****  | system_PD                        | 0 = all circuits powered up.<br>1 = power down the whole chip, except I <sup>2</sup> C, HPD interrupt and MSEN interrupt. Default = 1.                |
|             |                         | [5]             | **0*****   | Test bit                         | Must be set to 0.   |
|             |                         | [4]             | ***1****   | INTR_pol                         | Interrupt polarity.<br>0 = low active interrupt.<br>1 = high active interrupt. Default = 1.   |
|             |                         | [3]             | ****0***   | initiate_scan                    | 1 = initiate scan. Default = 1.   |
| 0x42        | Read                    | [7]             | 1*****   | PD_pol                           | Polarity for power-down pin.<br>0 = low active.<br>1 = high active.   |
|             |                         | [6]             | *0*****  | HPD_state                        | State of the hot plug detection.<br>0 = hot plug detect inactive.<br>1 = hot plug active.   |
|             |                         | [5]             | **0*****   | MSEN_state                       | State of the monitor connection.<br>0 = HDMI clock termination not detected.<br>1 = HDMI clock termination detected.                                  |
| 0x43        | Read/Write              | [7:0]           | 01111110   | EDID_ID                          | The I <sup>2</sup> C address for EDID memory. Default = 0x7E.   |
| 0x44        | Read/Write              | [7]             | 0*****   | spdif_en                         | 1 = enable S/PDIF receiver. Default = 0.  |
|             |                         | [6]             | *1*****  | N_CTS_pkt_en                     | 1 = enable N_CTS packet. Default = 1.   |
|             |                         | [5]             | **1*****   | audio_sample_pkt_en              | 1 = enable audio sample packet. Default = 1.  |
|             |                         | [4]             | ***1****   | aviIF_pkt_en                     | 1 = enable avi info frame. Default = 1.   |
| 0x45        | Read/Write              | [3]             | ****1***   | audioIF_pkt_en                   | 1 = enable audio info frame. Default = 1.   |
|             |                         | [7]             | 0*****   | clear_avmute                     | 1 = clear av mute. Default = 0.   |
|             |                         | [6]             | *0*****  | set_avmute                       | 1 = set av mute. Default = 0.   |
|             |                         | [5:4]           | **00****   | Y1Y0                             | Output format, should be written when 0x16[7:6] is written.<br>00 = RGB.<br>01 = YCbCr 4:2:2.<br>10 = YCbCr 4:4:4.<br>11 = reserved.<br>Default = 00. |
|             |                         | [3]             | ****0***   | Active Format Information Status | Active format information present.<br>0 = no data.<br>1 = active format information valid. Default = 0.   |
| [2:1]       | ****00*                 | Bar Information | B[1:0].<br>00 = no bar information.<br>01 = horizontal bar information valid.<br>10 = vertical bar information valid.<br>11 = horizontal and vertical bar information valid. Default = 00. |                                  |   |

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name              | Description   |
|-------------|-------------------------|-------|---------------|----------------------------|---|
| 0x46        | Read/Write              | [7:6] | 00*****       | Scan Information           | S[1:0].<br>00 = no information.<br>01 = overscanned (television).<br>10 = underscanned (computer).<br>11 = undefined.<br>Default = 00.  |
|             |                         | [5:4] | **00****      | Colorimetry                | C[1:0].<br>00 = no data.<br>01 = SMPTE 170M, ITU601.<br>10 = ITU709.<br>11 = undefined.<br>Default = 00.  |
|             |                         | [3:2] | ****00**      | Picture Aspect Ratio       | M[1:0].<br>00 = no data.<br>01 = 4:3.<br>10 = 16:9.<br>11 = undefined.<br>Default = 00.   |
|             |                         | [1:0] | *****00       | Nonuniform Picture Scaling | SC[1:0].<br>00 = No known nonuniform scaling.<br>01 = picture has been scaled horizontally.<br>10 = picture has been scaled vertically.<br>11 = picture has been scaled horizontally and vertically.<br>Default = 00. |
| 0x47        | Read/Write              | [7:4] | 0000****      | Active Format Aspect Ratio | R[3:0].<br>1000 = same as picture aspect ratio.<br>1001 = 4:3 (center).<br>1010 = 16:9 (center).<br>1011 = 14:9 (center).<br>Default = 0x0.   |
| 0x48        | Read/Write              | [7:0] | 00000000      | Active Line Start LSB      | This represents the line number at the end of the top horizontal bar. If 0, there is no horizontal bar.   |
| 0x49        | Read/Write              | [7:0] | 00000000      | Active Line Start MSB      |   |
| 0x4A        | Read/Write              | [7:0] | 00000000      | Active Line End LSB        | This represents the line number at the beginning of a lower horizontal bar. If greater than the number of active video lines, there is no lower horizontal bar.   |
| 0x4B        | Read/Write              | [7:0] | 00000000      | Active Line End MSB        |   |
| 0x4C        | Read/Write              | [7:0] | 00000000      | Active Pixel Start LSB     | This represents the last pixel in a vertical pillar bar at the left side of the picture. If 0, there is no left bar.  |
| 0x4D        | Read/Write              | [7:0] | 00000000      | Active Pixel Start MSB     |   |
| 0x4E        | Read/Write              | [7:0] | 00000000      | Active Pixel End LSB       | This represents the first horizontal pixel in a vertical pillar bar at the right side of the picture. If greater than the maximum number of horizontal pixels, there is no vertical bar.                              |
| 0x4F        | Read/Write              | [7:0] | 00000000      | Active Pixel End MSB       |   |
| 0x50        | Read/Write              | [7:5] | 000*****      | audio_IF_CC                | Channel count.<br>000 = refer to stream header.<br>001 = 2 channels.<br>010 = 3 channels.<br>...<br>111 = 8 channels.<br>Default = 000.   |
|             |                         | [4]   | ***0****      | audio_IF_DM_INH            | Down-mix inhibit.<br>0 = Permitted or no information about this.<br>1 = Prohibited.<br>Default = 0.   |
|             |                         | [3:0] | ****0000      | Level Shift                | LSV[3:0]. Level Shift Values with attenuation information.<br>0000 = 0 dB attenuation.<br>0001 = 1 dB attenuation.<br>...<br>1111 = 15 dB attenuation.<br>Default = 0x0.  |

# AD9389

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name   | Description  |
|-------------|-------------------------|-------|---------------|---|--|
| 0x51        | Read/Write              | [7:0] | 00000000      | Speaker Mapping                                       | CA[7:0]. Speaker mapping or placement for up to 8 channels (see Table 24).<br>Default = 0x00.  |
| 0x52        | Read/Write              | [7:0] | 00000000      | Source Product Description Infoframe Byte 1. (SPD_B1) | Vendor name character 1 (VN1).   |
| 0x53        | Read/Write              | [7:0] | 00000000      | SPD_B2  | VN2.   |
| 0x54        | Read/Write              | [7:0] | 00000000      | SPD_B3  | VN3.   |
| 0x55        | Read/Write              | [7:0] | 00000000      | SPD_B4  | VN4.   |
| 0x56        | Read/Write              | [7:0] | 00000000      | SPD_B5  | VN5.   |
| 0x57        | Read/Write              | [7:0] | 00000000      | SPD_B6  | VN6.   |
| 0x58        | Read/Write              | [7:0] | 00000000      | SPD_B7  | VN7.   |
| 0x59        | Read/Write              | [7:0] | 00000000      | SPD_B8  | VN8.   |
| 0x5A        | Read/Write              | [7:0] | 00000000      | SPD_B9  | Product description character 1 (PD1).   |
| 0x5B        | Read/Write              | [7:0] | 00000000      | SPD_B10   | PD2.   |
| 0x5C        | Read/Write              | [7:0] | 00000000      | SPD_B11   | PD3.   |
| 0x5D        | Read/Write              | [7:0] | 00000000      | SPD_B12   | PD4.   |
| 0x5E        | Read/Write              | [7:0] | 00000000      | SPD_B13   | PD5.   |
| 0x5F        | Read/Write              | [7:0] | 00000000      | SPD_B14   | PD6.   |
| 0x60        | Read/Write              | [7:0] | 00000000      | SPD_B15   | PD7.   |
| 0x61        | Read/Write              | [7:0] | 00000000      | SPD_B16   | PD8.   |
| 0x62        | Read/Write              | [7:0] | 00000000      | SPD_B17   | PD9.   |
| 0x63        | Read/Write              | [7:0] | 00000000      | SPD_B18   | PD10.  |
| 0x64        | Read/Write              | [7:0] | 00000000      | SPD_B19   | PD11.  |
| 0x65        | Read/Write              | [7:0] | 00000000      | SPD_B20   | PD12.  |
| 0x66        | Read/Write              | [7:0] | 00000000      | SPD_B21   | PD13.  |
| 0x67        | Read/Write              | [7:0] | 00000000      | SPD_B22   | PD14.  |
| 0x68        | Read/Write              | [7:0] | 00000000      | SPD_B23   | PD15.  |
| 0x69        | Read/Write              | [7:0] | 00000000      | SPD_B24   | PD16.  |
| 0x6A        | Read/Write              | [7:0] | 00000000      | SPD_B25   | Source device information code.<br>Code defines source, such as DVD or STB.<br>Default = 0x00.   |
| 0x6B        | Read/Write              | [7:0] | 00000000      | MPEG_B0   | MB[0]. Lower byte of MPEG bit rate: Hz. This is the lower 8 bits of 32 bits (4 bytes) that specify the MPEG bit rate in Hz.<br>MB[1].<br>MB[2].<br>MB[3] (upper byte).         |
| 0x6C        | Read/Write              | [7:0] | 00000000      | MPEG_B1   |  |
| 0x6D        | Read/Write              | [7:0] | 00000000      | MPEG_B2   |  |
| 0x6E        | Read/Write              | [7:0] | 00000000      | MPEG_B3   |  |
| 0x6F        | Read/Write              | [7]   | 0*****        | MPEG_FR   | FR indicates new picture or repeat.<br>0 = new field or picture.<br>1 = repeated field.<br>Default = 0.  |
| 0x70        | Read/Write              | [6:5] | *00*****      | MPEG_MF   | MPEG frame indicator.<br>MF[1:0] identifies whether frame is an I, B, or P picture.<br>00 = unknown.<br>01 = I picture.<br>10 = B picture.<br>11 = P picture.<br>Default = 00. |

| Hex Address | Read/Write or Read Only | Bits                        | Default Value                         | Register Name  | Description   |
|-------------|-------------------------|-----------------------------|---------------------------------------|--|---|
| 0x71        | Read/Write              | [7:0]                       | 00000000                              | Audio Content Protection Packet (ACP) Type             | ACP type.<br>0 = generic audio.<br>1 = IEC 60958-identified audio.<br>2 = DVD audio.<br>3 = reserved for SACD.<br>Default = 0x00.   |
| 0x72        | Read/Write              | [7:0]                       | 00000000                              | ACP_byte1  | Audio content protection.<br>[7:6] audio_copy_permission.<br>[5:3] audio_copy_number.<br>[2:1] quality.<br>[0] transaction.   |
| 0x73        | Read/Write              | [7]<br><br>[6]<br><br>[5:3] | 0*****<br><br>*0*****<br><br>**000*** | ISRC1 Continued<br><br>ISRC1_valid<br><br>ISRC1 Status | International standard recording code continued (ISRC1). Indicates an ISRC2 packet is being transmitted.<br>1 = the 2nd ISRC packet is needed.<br>Default = 0.<br>0 = ISRC1 status bits and PBs not valid.<br>1 = ISRC1 status bits and PBs valid.<br>Default = 0.<br>These bits indicate beginning, middle, and end of a track.<br>001 = start.<br>010 = middle.<br>100 = end.<br>Default = 000. |
| 0x74        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB0  | ISRC1 Packet Byte 0.  |
| 0x75        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB1  | ISRC1 Packet Byte 1.  |
| 0x76        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB2  | ISRC1 Packet Byte 2.  |
| 0x77        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB3  | ISRC1 Packet Byte 3.  |
| 0x78        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB4  | ISRC1 Packet Byte 4.  |
| 0x79        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB5  | ISRC1 Packet Byte 5.  |
| 0x7A        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB6  | ISRC1 Packet Byte 6.  |
| 0x7B        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB7  | ISRC1 Packet Byte 7.  |
| 0x7C        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB8  | ISRC1 Packet Byte 8.  |
| 0x7D        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB9  | ISRC1 Packet Byte 9.  |
| 0x7E        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB10   | ISRC1 Packet Byte 10.   |
| 0x7F        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB11   | ISRC1 Packet Byte 11.   |
| 0x80        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB12   | ISRC1 Packet Byte 12.   |
| 0x81        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB13   | ISRC1 Packet Byte 13.   |
| 0x82        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB14   | ISRC1 Packet Byte 14.   |
| 0x83        | Read/Write              | [7:0]                       | 00000000                              | ISRC1_PB15   | ISRC1 Packet Byte 15.   |
| 0x84        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB0  | ISRC2 Packet Byte 0.  |
| 0x85        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB1  | ISRC2 Packet Byte 1.  |
| 0x86        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB2  | ISRC2 Packet Byte 2.  |
| 0x87        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB3  | ISRC2 Packet Byte 3.  |
| 0x88        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB4  | ISRC2 Packet Byte 4.  |
| 0x89        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB5  | ISRC2 Packet Byte 5.  |
| 0x8A        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB6  | ISRC2 Packet Byte 6.  |
| 0x8B        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB7  | ISRC2 Packet Byte 7.  |
| 0x8C        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB8  | ISRC2 Packet Byte 8.  |
| 0x8D        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB9  | ISRC2 Packet Byte 9.  |
| 0x8E        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB10   | ISRC2 Packet Byte 10.   |
| 0x8F        | Read/Write              | [7:0]                       | 00000000                              | ISRC2_PB11   | ISRC2 Packet Byte 11.   |

# AD9389

| Hex Address | Read/Write or Read Only | Bits                                   | Default Value  | Register Name  | Description  |
|-------------|-------------------------|--|--|--|--|
| 0x90        | Read/Write              | [7:0]                                  | 00000000   | ISRC2_PB12   | ISRC2 Packet Byte 12.  |
| 0x91        | Read/Write              | [7:0]                                  | 00000000   | ISRC2_PB13   | ISRC2 Packet Byte 13.  |
| 0x92        | Read/Write              | [7:0]                                  | 00000000   | ISRC2_PB14   | ISRC2 Packet Byte 14.  |
| 0x93        | Read/Write              | [7:0]                                  | 00000000   | ISRC2_PB15   | ISRC2 Packet Byte 15.  |
| 0x94        | Read/Write              | [7:0]                                  | 11000000   | mask1  | Mask for Interrupt Group1 (0x96).  |
| 0x95        | Read/Write              | [7:6]                                  | 00*****  | mask2  | Mask for Interrupt Group 2 (0x97[7:6].<br>[7] for HDCP error.<br>[6] for BKSV flag.  |
| 0x96        | Read/Write              | [7]<br>[6]<br>[5]<br>[4]<br>[3]<br>[2] | 0*****<br>*0*****<br>**0*****<br>***0*****<br>****0***<br>*****0** | HPD_INT<br>MSEN_INT<br>VS_INT<br>AUD_FIFO_FULL_INT<br>ITU656_ERR_INT<br>EDID_RDY_INT | Interrupt for hot plug detect (HPD).<br>Interrupt for monitor connection (MSEN).<br>Interrupt for active VS edge.<br>Interrupt for audio FIFO overflow.<br>Interrupt for ITU656 error.<br>Interrupt for EDID Ready.  |
| 0x97        | Read/Write              | [7]<br>[6]<br>[2]                      | 0*****<br>*0*****<br>*****0**                                      | HDCP_ERR_INT<br>BKSV_flag<br>Test bit  | Interrupt bit from HDCP master.<br>Set to 1 to instruct the MPU to read the BKSV or the EDID MEM for revocation list checking.<br>Must be written to 1 for proper operation.   |
| 0x98        | Read/Write              | [7]<br>[3:0]                           | 0*****<br>****0010   | Test bits  | Must be written to 0 for proper operation.<br>Must be written to 0x2 for proper operation.   |
| 0x9C        | Read/Write              | [7:0]                                  |  | Test bits  | Must be written to 0x3A for proper operation.  |
| 0x9D        | Read/Write              | [3:0]                                  | ****0***   | Test bit   | Must be written to 1 for proper operation.   |
| 0xA2        | Read/Write              | [7:0]                                  |  | Test bits  | Must be written to 0x87 for proper operation.  |
| 0xA3        | Read/Write              | [7:0]                                  |  | Test bits  | Must be written to 0x87 for proper operation.  |
| 0xAF        | Read/Write              | [7]<br>[5]<br>[4]<br>[3]<br>[1]<br>[0] | 0*****<br>**0*****<br>***1****<br>****0***<br>*****0*<br>*****0    | HDCP_desired<br><br>frame_enc<br><br>ext_HDMI_MODE                                   | HDCP encryption.<br>0 = input A/V content not to be encrypted.<br>1 = the input A/V content should be encrypted.<br>Default = 0.<br>Must be written to 0 for proper operation.<br>Frame encryption.<br>0 = the current frame should not be encrypted.<br>1 = the current frame should be encrypted.<br>Default = 1.<br>Must be written to 0 for proper operation.<br>HDMI mode.<br>0 = DVI.<br>1 = HDMI.<br>Default = 0.<br>Must be written to 0 for proper operation. |
| 0xB0        | Read                    | [7:0]                                  | 00000000   | An_0   | Byte 0 of An.  |
| 0xB1        | Read                    | [7:0]                                  | 00000000   | An_1   | Byte 1 of An.  |
| 0xB2        | Read                    | [7:0]                                  | 00000000   | An_2   | Byte 2 of An.  |
| 0xB3        | Read                    | [7:0]                                  | 00000000   | An_3   | Byte 3 of An.  |
| 0xB4        | Read                    | [7:0]                                  | 00000000   | An_4   | Byte 4 of An.  |
| 0xB5        | Read                    | [7:0]                                  | 00000000   | An_5   | Byte 5 of An.  |
| 0xB6        | Read                    | [7:0]                                  | 00000000   | An_6   | Byte 6 of An.  |

| Hex Address | Read/Write or Read Only | Bits      | Default Value | Register Name              | Description  |
|-------------|-------------------------|-----------|---------------|----------------------------|--|
| 0xB7        | Read                    | [7:0]     | 00000000      | An_7                       | Byte 7 of An.<br>1 = the A/V content is being encrypted.<br>0 = not encrypted.<br>Default = 0.<br>Digital mode.<br>1 = HDMI mode.<br>0 = DVI mode.<br>1 = HDCP key reading error.  |
|             |                         | [6]       | *0*****       | ENC_on                     |  |
|             |                         | [5]       | **0*****      | int_HDMI_MODE              |  |
|             |                         | [4]       | ***0****      | keys_read_error            |  |
| 0xBA        | Read/Write              | [7:5]     | 000*****      | clk_delay                  | Edge select for input video clock.<br>011 = positive edge capture.<br>111 = negative edge capture.<br>Default = 000.<br>Must be written to 1 for proper operation.<br>Must be written to 0 for proper operation.   |
|             |                         | [4]       | ***0****      |                            |  |
|             |                         | [3]       | ****0***      |                            |  |
| 0xBE        | Read                    | [7]       | 0*** ****     | BCAPS                      | HDMI reserved.<br>HDCP repeater.<br>0 = HDCP receiver is not repeater capable.<br>1 = HDCP receiver is repeater capable.<br>KSV FIFO ready.<br>1 = HDCP receiver has compiled list of attached KSVs.<br>Must be written to 0 for proper operation.<br>Reserved.<br>HDCP 1.1 features support.<br>0 = HDCP receiver does not support version 1.1 features.<br>1 = HDCP receiver supports 1.1 features such as enhanced encryption status signaling (EESS).<br>Fast authentication.<br>0 = HDCP Receiver not capable of fast authentication.<br>1 = HDCP Receiver capable of receiving unencrypted video during the session re-authentication. |
|             |                         | [6]       | *0** ****     | Repeater                   |  |
|             |                         | [5]       | **0* ****     | KSV ready                  |  |
|             |                         | [4]       | ***0 ****     | Test bit                   |  |
|             |                         | [3:2]     | **** 00**     | Test bit                   |  |
|             |                         | [1]       | **** *0*      | HDCP support               |  |
| [0]         | **** **0                | Fast HDCP |               |                            |  |
| 0xBF        | Read                    | [7:0]     | 00000000      | BKSV1                      | BKSV read from Rx by the HDCP controller 40 bits (5 bytes).  |
| 0xC0        | Read                    | [7:0]     | 00000000      | BKSV2                      |  |
| 0xC1        | Read                    | [7:0]     | 00000000      | BKSV3                      |  |
| 0xC2        | Read                    | [7:0]     | 00000000      | BKSV4                      |  |
| 0xC3        | Read                    | [7:0]     | 00000000      | BKSV5                      |  |
| 0xC4        | Read/Write              | [7:0]     | 00000000      | EDID Segment               | Sets the E-DDC segment used by the EDID fetch routine.   |
| 0xC5        | Read                    | [7]       | 0*****        | Error Flag                 | Error flag.<br>AN stop.<br>HDCP enabled.<br>EDID ready.<br>I <sup>2</sup> C.<br>RI.<br>BKSV update.<br>PJ.   |
|             |                         | [6]       | *0*****       | AN Stop                    |  |
|             |                         | [5]       | **0*****      | HDCP Enabled               |  |
|             |                         | [4]       | ***0****      | EDID Ready Flag            |  |
|             |                         | [3]       | ****0***      | I <sup>2</sup> C Interrupt |  |
|             |                         | [2]       | *****0**      | RI Flag                    |  |
|             |                         | [1]       | *****0*       | BKSV Update Flag           |  |
| [0]         | *****0                  | PJ Flag   |               |                            |  |
| 0xC6        | Read                    | [4]       | ***0****      | HDMI Mode                  | HDMI.<br>HDCP requested.<br>Rx sense.<br>EEPROM read.<br>TMDS output enabled.  |
|             |                         | [3]       | ****0***      | HDCP Requested             |  |
|             |                         | [2]       | *****0**      | Rx Sense                   |  |
|             |                         | [1]       | *****0*       | EEPROM Read OK             |  |
|             |                         | [0]       | *****0        | TMDS Output Enabled        |  |
| 0xC7        | Read/Write              | [7]       | 0*****        | BKSV Flag                  | BKSV flag.<br>BKSV count   |
|             |                         | [6:0]     | *0000000      | BKSV Count                 |  |

# AD9389

| Hex Address | Read/Write or Read Only | Bits  | Default Value | Register Name         | Description   |
|-------------|-------------------------|-------|---------------|-----------------------|---|
| 0xC8        | Read                    | [7:4] | 0000****      | HDCP Controller Error | HDCP controller error, see Table 28.                                  |
|             |                         | [3:0] | ****0000      | HDCP Controller State | HDCP controller state.  |
| 0xC9        | Read/Write              | [3:0] | ****0011      | EDID Tries            | Number of times that the EDID is read if unsuccessful. Default = 0x3. |



## 2-WIRE SERIAL CONTROL REGISTER DETAIL CHIP IDENTIFICATION

### 0x00—Bits[7:0] Chip Revision

An 8-bit register that represents the silicon revision.

### 0x01—Bits[3:0] N[19:16]

These are the most significant four bits of a 20-bit word used along with the 20-bit CTS term in the receiver to regenerate the audio clock.

### 0x02—Bits[7:0] N[15-8]

### 0x03—Bits[7:0] [(7-0)]

### 0x04—Bits[3:0] CTS\_Int[19:16]

These are the most significant four bits of a 20-bit word used along with the 20-bit N term in the receiver to regenerate the audio clock. This is the measured or internal CTS. The internal or external CTS can be selected via 0x0A Bit 7.

### 0x05—Bits[7:0] CTS\_Int[15:8]

### 0x06—Bits[7:0] CTS\_In[7:0]

### 0x07—Bits[3:0] CT\_Ext[19:16]

These are the most significant four bits of a 20-bit word used along with the 20-bit N term in the receiver to regenerate the audio clock. This is the external CTS. The internal or external CTS can be selected via 0x0A Bit 7.

### 0x08—Bits[7:0] CTS\_Ext[15:8]

### 0x09—Bits[7:0] CTS\_Ext[7:0]

### 0x0A—Bits[7] CTS\_Sel

When internal CTS is selected, the CTS is calculated by the AD9389.

- 0 = internal CTS
- 1 = external CTS

### 0x0A—Bits[6:5] Avg\_Mode

- 00 = no filter
- 01 = divide by 4
- 10 = divide by 8
- 11 = divide by 16
- Default = 10

### 0x0A—Bit[4] Audio\_Sel

- 0 = I<sup>2</sup>S
- 1 = S/PDIF
- Default = 0

### 0x0A—Bit[3] MCLK\_SP

If MCLK is available for S/PDIF, it is used for bit recovery; otherwise, internal circuitry is used.

- 1 = MCLK active
- 0 = MCLK inactive
- Default = 0

### 0x0A—Bit[2] MCLK\_I<sup>2</sup>S

- 1 = I<sup>2</sup>S MCLK active
- 0 = I<sup>2</sup>S MCLK inactive
- Default = 0

If MCLK is available for I<sup>2</sup>S, it is used for bit recovery; otherwise, internal circuitry is used.

### 0x0A—Bits[1:0] MCLK\_Ratio

- 00 = ×128 f<sub>s</sub>
- 01 = ×256 f<sub>s</sub>
- 10 = ×384 f<sub>s</sub>
- 11 = ×512 f<sub>s</sub>
- Default = 01

### 0x0B—Bit[6] MCLK\_Pol

- 0 = rising edge
- 1 = falling edge
- Default = 0

### 0x0B—Bit[5] Flat\_Line

- 1 = flat line audio (audio sample not valid)
- 0 = normal
- Default = 0

### 0x0C—Bits[5:2] I<sup>2</sup>S enable

- 0001 = I<sup>2</sup>S0
- 0010 = I<sup>2</sup>S1
- 0100 = I<sup>2</sup>S2
- 1000 = I<sup>2</sup>S3
- Default = 1111 for all

### 0x0C—Bits[1:0] I<sup>2</sup>S Format

- 00 = standard I<sup>2</sup>S mode
- 01 = right-justified I<sup>2</sup>S mode
- 10 = left-justified I<sup>2</sup>S mode
- 11 = raw IEC60958 mode
- Default = 00

### 0x0D—Bits[4:0] I<sup>2</sup>S bit width

For right-justified audio only. Default is 11000 (24). Not valid for widths greater than 24.

### 0x0E—Bits[5:3] SUBPKT0\_L\_src

Source of audio subpacket 0 (left channel) data. Default is 000.

**Table 23. Source of Subpacket Audio**

| Field Code | Channel (0 to 3) and Left/Right |
|------------|---------------------------------|
| 000        | Channel 0 Left                  |
| 001        | Channel 0 Right                 |
| 010        | Channel 1 Left                  |
| 011        | Channel 1 Right                 |
| 100        | Channel 2 Left                  |
| 101        | Channel 2 Right                 |
| 110        | Channel 3 Left                  |
| 111        | Channel 3 Right                 |

**0x0E—Bits[2:0] SUBPKT0\_R\_src**

Default is 001 (see Table 27).

**0x0F—Bits[5:3] SUBPKT1\_L\_src**

Default is 010 (see Table 27).

**0x0F—Bits[2:0] SUBPKT1\_R\_src**

Default is 011 (see Table 27).

**0x10—Bits[5:3] SUBPKT2\_L\_src**

Default is 100 (see Table 27).

**0x10—Bits[2:0] SUBPKT2\_R\_src**

Default is 101 (see Table 27).

**0x11—Bits[5:3] SUBPKT3\_L\_src**

Default is 110 (see Table 27).

**0x11—Bits[2:0] SUBPKT3\_R\_src**

Default is 111 (see Table 27).

**0x18—Bits[4:0] CSC\_A1\_MSB**

These five bits form the 5 MSBs of the Color Space Conversion coefficient a1. Combined with the 8 LSBs of the following register, they form a 13-bit, twos complement coefficient that is user programmable. The equation takes the form of

$$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$$

$$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$$

$$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$$

The default value for the 13-bit, a1 coefficient is 0x0662.

**0x19—Bits[7:0] CSC\_A1\_LSB**

See Register 0x18.

**0x1A—Bits[4:0] CSC\_A2\_MSB**

These five bits form the 5 MSBs of the Color Space Conversion coefficient a2. This combined with the 8 LSBs of the following register form a 13-bit, twos complement coefficient that is user programmable. The equation takes the form of

$$R_{OUT} = (a1 \times R_{IN}) + (a2 \times G_{IN}) + (a3 \times B_{IN}) + a4$$

$$G_{OUT} = (b1 \times R_{IN}) + (b2 \times G_{IN}) + (b3 \times B_{IN}) + b4$$

$$B_{OUT} = (c1 \times R_{IN}) + (c2 \times G_{IN}) + (c3 \times B_{IN}) + c4$$

The default value for the 13-bit a2 coefficient is 0x04A8.

**0x1B—Bits[7:0] CSC\_A2\_LSB**

See Register 0x1A.

**0x1C—Bits[4:0] CSC\_A3\_MSB**

The default value for the 13-bit a3 is 0x0000.

**0x1D—Bits[7:0] CSC\_A3\_LSB**

**0x1E—Bits[4:0] CSC\_A4\_MSB**

The default value for the 13-bit a4 is 0x1C84.

**0x1F—Bits[7:0] CSC\_A4\_LSB**

**0x20—Bits[4:0] CSC\_B1\_MSB**

The default value for the 13-bit b1 is 0x1CBF.

**0x21—Bits[7:0] CSC\_B1\_LSB**

**0x22—Bits[4:0] CSC\_B2\_MSB**

The default value for the 13-bit b2 is 0x04A8.

**0x23—Bits[7:0] CSC\_B2\_LSB**

**0x24—Bits[4:0] CSC\_B3\_MSB**

The default value for the 13-bit b3 is 0x1E70.

**0x25—Bits[7:0] CSC\_B3\_LSB**

**0x26—Bits[4:0] CSC\_B4\_MSB**

The default value for the 13-bit b4 is 0x021E.

**0x27—Bits[7:0] CSC\_B4\_LSB**

**0x28—Bits[4:0] CSC\_C1\_MSB**

The default value for the 13-bit c1 is 0x0000.

**0x29—Bits[7:0] CSC\_C1\_LSB**

**0x2A—Bits[4:0] CSC\_C2\_MSB**

The default value for the 13-bit c2 is 0x04A8.

**0x2B—Bits[7:0] CSC\_C2\_LSB**

**0x2C—Bits[4:0] CSC\_C3\_MSB**

The default value for the 13-bit c3 is 0x0812.

**0x2D—Bits[7:0] CSC\_C3\_LSB**

**0x2E—Bits[4:0] CSC\_C4\_MSB**

The default value for the 13-bit c4 is 0x1BAC.

**0x2F—Bits[7:0] CSC\_C4\_LSB**

**0x3C—Bits[5:0] ext VID to Rx**

Table 24.

| VID | Format | Vertical Refresh    |
|-----|--------|---------------------|
| 1   | 480p   | ~60 Hz <sup>1</sup> |
| 2   | 480p   | ~60 Hz              |
| 3   | 480p   | ~60 Hz              |
| 4   | 720p   | ~60 Hz              |
| 5   | 1080i  | ~60 Hz              |
| 6   | 480i   | ~60 Hz              |
| 7   | 480i   | ~60 Hz              |
| 8   | 240p   | ~60 Hz              |
| 9   | 240p   | ~60 Hz              |
| 10  | 480i   | ~60 Hz              |
| 11  | 480i   | ~60 Hz              |
| 12  | 240p   | ~60 Hz              |
| 13  | 240p   | ~60 Hz              |
| 14  | 480p   | ~60 Hz              |
| 15  | 480p   | ~60 Hz              |
| 16  | 1080p  | ~60 Hz              |
| 17  | 576p   | ~50 Hz <sup>2</sup> |
| 18  | 576p   | ~50 Hz              |
| 19  | 720p   | ~50 Hz              |
| 20  | 1080i  | ~50 Hz              |
| 21  | 576i   | ~50 Hz              |
| 22  | 576i   | ~50 Hz              |
| 23  | 288p   | ~50 Hz              |
| 24  | 288p   | ~50 Hz              |
| 25  | 576i   | ~50 Hz              |
| 26  | 576i   | ~50 Hz              |
| 27  | 288p   | ~50 Hz              |
| 28  | 288p   | ~50 Hz              |
| 29  | 576p   | ~50 Hz              |
| 30  | 576p   | ~50 Hz              |
| 31  | 1080p  | ~50 Hz              |
| 32  | 1080p  | 24 Hz to 30 Hz      |
| 33  | 1080p  | 24 Hz to 30 Hz      |
| 34  | 1080p  | 24 Hz to 30 Hz      |

<sup>1</sup> V<sub>REF</sub> can range from 59.826 Hz to 60.115 Hz.<sup>2</sup> V<sub>REF</sub> can range from 49.761 Hz to 50.080 Hz.**0x3D—Bits[7:6] pr to Rx****0x43—Bits[7:0] EDID Read Address**

This is a programmable I<sup>2</sup>C address from which the EDID information (1 to 256 segment) can be read. Default is 0x7E.

**0x48—Bits[7:0] Active Line Start LSB**

Combined with the MSB in Register 0x49, these bits indicate the beginning line of active video. All lines before this comprise a top horizontal bar. This is used in letter-box modes. If the 2-byte value is 0x00, there is no horizontal bar.

**0x49—Bits[7:0] Active Line Start MSB**

See Register 0x48.

**0x4A—Bits[7:0] Active Line End LSB**

Combined with the MSB in Register 0x4B, the bits indicate the last line of active video. All lines past this comprise a lower horizontal bar. This is used in letter-box modes. If the 2-byte value is greater than the number of lines in the display, there is no lower horizontal bar.

**0x4B—Bits[7:0] Active Line End MSB**

See Register 0x4A.

**0x4C—Bits[7:0] Active Pixel Start LSB**

Combined with the MSB in Register 0x4D, these bits indicate the first pixel in the display that is active video. All pixels before this comprise a left vertical bar. If the 2-byte value is 0x00, there is no left bar.

**0x4D—Bits[7:0] Active Pixel Start MSB**

See Register 0x4C.

**0x4E—Bits[7:0] Active Pixel End LSB**

Combined with the MSB in Register 0x4F, these bits indicate the last active video pixel in the display. All pixels past this comprise a right vertical bar. If the 2-byte value is greater than the number of pixels in the display, there is no vertical bar.

**0x4F—Bits[7:0] Active Pixel End MSB**

See Register 0x4E.

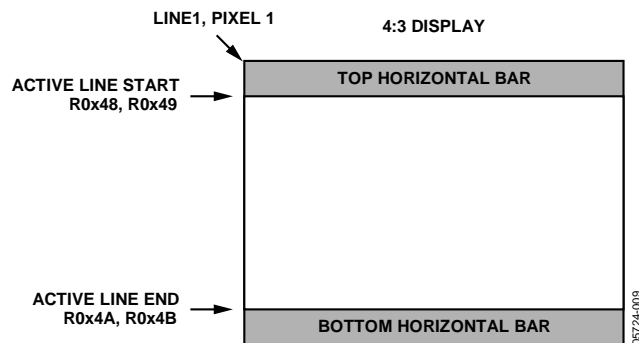


Figure 9. Horizontal Bars

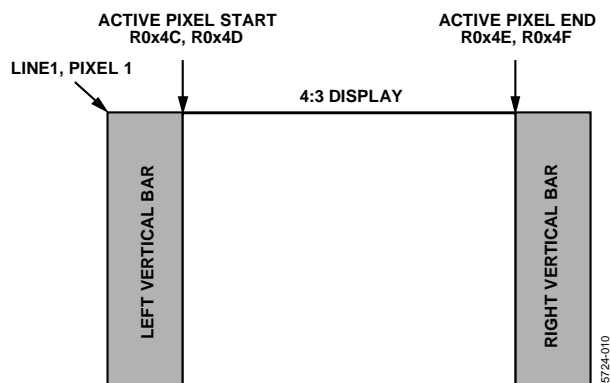


Figure 10. Vertical Bars

# AD9389

## 0x50—Bits[7:5] audio\_IF\_cc

000 = refer to stream header  
 001 = 2 channels  
 010 = 3 channels  
 ...  
 111 = 8 channels

## 0x50—Bits[4] audi\_IF\_DM\_INH

### 0x50—Bits[3:0] Level Shift

LSV[3:0] – Level Shift Values with attenuation information.  
 0000 = 0 dB attenuation  
 0001 = 1 dB attenuation  
 ...  
 1111 = 15 dB attenuation  
 Default = 0x0

## 0x51—Bits[7:0] Speaker Mapping

These bits define the suggested placement of speakers.

Table 25.

| CA    |       |       |       |       | Channel Number |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|----------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Bit 8          | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 |
| 0     | 0     | 0     | 0     | 0     |                |       |       |       | -     | -     | FR    | FL    |
| 0     | 0     | 0     | 0     | 1     |                |       |       |       | -     | LFE   | FR    | FL    |
| 0     | 0     | 0     | 1     | 0     |                |       |       |       | FC    | -     | FR    | FL    |
| 0     | 0     | 0     | 1     | 1     |                |       |       |       | FC    | LFE   | FR    | FL    |
| 0     | 0     | 1     | 0     | 0     |                |       |       | RC    | -     | -     | FR    | FL    |
| 0     | 0     | 1     | 0     | 1     |                |       |       | RC    | -     | LFE   | FR    | FL    |
| 0     | 0     | 1     | 1     | 0     |                |       |       | RC    | FC    | -     | FR    | FL    |
| 0     | 0     | 1     | 1     | 1     |                |       |       | RC    | FC    | LFE   | FR    | FL    |
| 0     | 1     | 0     | 0     | 0     |                |       | RR    | RL    | -     | -     | FR    | FL    |
| 0     | 1     | 0     | 0     | 1     |                |       | RR    | RL    | -     | LFE   | FR    | FL    |
| 0     | 1     | 0     | 1     | 0     |                |       | RR    | RL    | FC    | -     | FR    | FL    |
| 0     | 1     | 0     | 1     | 1     | -              | -     | RR    | RL    | FC    | LFE   | FR    | FL    |
| 0     | 1     | 1     | 0     | 0     | -              | RC    | RR    | RL    | -     | -     | FR    | FL    |
| 0     | 1     | 1     | 0     | 1     | -              | RC    | RR    | RL    | -     | LFE   | FR    | FL    |
| 0     | 1     | 1     | 1     | 0     | -              | RC    | RR    | RL    | FC    | -     | FR    | FL    |
| 0     | 1     | 1     | 1     | 1     | -              | RC    | RR    | RL    | FC    | LFE   | FR    | FL    |
| 1     | 0     | 0     | 0     | 0     | RRC            | RLC   | RR    | RL    | -     | -     | FR    | FL    |
| 1     | 0     | 0     | 0     | 1     | RRC            | RLC   | RR    | RL    | -     | LFE   | FR    | FL    |
| 1     | 0     | 0     | 1     | 0     | RRC            | RLC   | RR    | RL    | FC    | -     | FR    | FL    |
| 1     | 0     | 0     | 1     | 1     | RRC            | RLC   | RR    | RL    | FC    | LFE   | FR    | FL    |
| 1     | 0     | 1     | 0     | 0     | FRC            | FLC   | -     | -     | -     | -     | FR    | FL    |
| 1     | 0     | 1     | 0     | 1     | FRC            | FLC   | -     | -     | -     | LFE   | FR    | FL    |
| 1     | 0     | 1     | 1     | 0     | FRC            | FLC   | -     | -     | FC    | -     | FR    | FL    |
| 1     | 0     | 1     | 1     | 1     | FRC            | FLC   | -     | -     | FC    | LFE   | FR    | FL    |
| 1     | 1     | 0     | 0     | 0     | FRC            | FLC   | -     | RC    | -     | -     | FR    | FL    |
| 1     | 1     | 0     | 0     | 1     | FRC            | FLC   | -     | RC    | -     | LFE   | FR    | FL    |
| 1     | 1     | 0     | 1     | 0     | FRC            | FLC   | -     | RC    | FC    | -     | FR    | FL    |
| 1     | 1     | 0     | 1     | 1     | FRC            | FLC   | -     | RC    | FC    | LFE   | FR    | FL    |
| 1     | 1     | 1     | 0     | 0     | FRC            | FLC   | RR    | RL    | -     | -     | FR    | FL    |
| 1     | 1     | 1     | 0     | 1     | FRC            | FLC   | RR    | RL    | -     | LFE   | FR    | FL    |
| 1     | 1     | 1     | 1     | 0     | FRC            | FLC   | RR    | RL    | FC    | -     | FR    | FL    |
| 1     | 1     | 1     | 1     | 1     | FRC            | FLC   | RR    | RL    | FC    | LFE   | FR    | FL    |

## SOURCE PRODUCT DESCRIPTION (SPD) INFOFRAME

### 0x52—Bits[7:0] SPD\_B1

This is the first character in eight that is the name of the company that appears on the product. The data characters are 7-bit ASCII code.

### 0x53—Bits[7:0] SPD\_B 2 (VN2)

### 0x54—Bits[7:0] SPD\_B 3(VN3)

### 0x55—Bits[7:0] SPD\_B 4(VN4)

### 0x56—Bits[7:0] SPD\_B 5(VN5)

### 0x57—Bits[7:0] SPD\_B 6(VN6)

### 0x58—Bits[7:0] SPD\_B 7(VN7)

### 0x59—Bits[7:0] SPD\_B 8(VN8)

### 0x5A—Bits[7:0] SBD\_B9

### Product Description Character 1 (PD1)

This is the first character of 16 that contains the model number and a short description of the product. The data characters are 7-bit ASCII code.

### 0x5B—Bits[7:0] SBD\_B10(PD2)

### 0x5C—Bits[7:0] SBD\_B11(PD3)

### 0x5D—Bits[7:0] SBD\_B12(PD4)

### 0x5E—Bits[7:0] SBD\_B13(PD5)

### 0x5F—Bits[7:0] SBD\_B14(PD6)

### 0x60—Bits[7:0] SBD\_B15(PD7)

### 0x61—Bits[7:0] SBD\_B16(PD8)

### 0x62—Bits[7:0] SBD\_B17(PD9)

### 0x63—Bits[7:0] SBD\_B18(PD10)

### 0x64—Bits[7:0] SBD\_B19(PD11)

### 0x65—Bits[7:0] SBD\_B20(PD12)

### 0x66—Bits[7:0] SBD\_B21(PD13)

### 0x67—Bits[7:0] SBD\_B22(PD14)

### 0x68—Bits[7:0] SBD\_B23(PD15)

### 0x69—Bits[7:0] SBD\_B24(PD16)

### 0x6A—Bits[7:0] Source Device Information Code

These bytes classify the source device.

Table 26.

| SDI Code     | Source      |
|--------------|-------------|
| 0x00         | Unknown     |
| 0x01         | Digital STB |
| 0x02         | DVD         |
| 0x03         | D-VHS       |
| 0x04         | HDD Video   |
| 0x05         | DVC         |
| 0x06         | DSC         |
| 0x07         | Video CD    |
| 0x08         | Game        |
| 0x09         | PC general  |
| 0x0A to 0xFF | Reserved    |

### 0x6B—Bits[7:0] MPEG\_B0

This is the lower 8 bits of 32 bits that specify the MPEG bit rate in Hz.

### 0x6C—Bits[7:0] MPEG\_B1

### 0x6D—Bits[7:0] MPEG\_B2

### 0x6E—Bits[7:0] MPEG\_B3

### 0x73—Bits[7] ISRC1 Continued

This bit indicates that a continuation of the 16 ISRC1 packet bytes (an ISRC2 packet) is being transmitted.

### 0x73—Bit[6] ISRC1 Valid

This bit indicates whether ISRC1 packet bytes are valid.

Table 27.

| ISRC1 | Valid                               |
|-------|-------------------------------------|
| 0     | ISRC1 Status bits and PBs not valid |
| 1     | ISRC1 Status bits and PBs valid     |

### 0x73—Bits[5:3] ISRC1 Status

These bits define where the samples are in the ISRC track: at least two transmissions of 001 occur at the beginning of the track; continuous transmission of 010 occurs in the middle of the track, followed by at least two transmissions of 100 near the end of the track.

### 0x74—Bits[7:0] ISRC1\_PB0

### 0x75—Bits[7:0] ISRC1\_PB1

### 0x76—Bits[7:0] ISRC1\_PB2

### 0x77—Bits[7:0] ISRC1\_PB3

### 0x78—Bits[7:0] ISRC1\_PB4

### 0x79—Bits[7:0] ISRC1\_PB5

### 0x7A—Bits[7:0] ISRC1\_PB6

### 0x7B—Bits[7:0] ISRC1\_PB7

### 0x7C—Bits[7:0] ISRC1\_PB8

### 0x7D—Bits[7:0] ISRC1\_PB9

### 0x7E—Bits[7:0] ISRC1\_PB10

### 0x7F—Bits[7:0] ISRC1\_PB11

### 0x80—Bits[7:0] ISRC1\_PB12

### 0x81—Bits[7:0] ISRC1\_PB13

### 0x82—Bits[7:0] ISRC1\_PB14

### 0x83—Bits[7:0] ISRC1\_PB15

# AD9389

## **0x84—Bits[7:0] ISRC2\_PB0**

This is transmitted only when the ISRC continue bit (Register 0x73 Bit 7) is set to 1.

## **0x85—Bits[7:0] ISRC2\_PB1**

## **0x86—Bits[7:0] ISRC2\_PB2**

## **0x87—Bits[7:0] ISRC2\_PB3**

## **0x88—Bits[7:0] ISRC2\_PB4**

## **0x89—Bits[7:0] ISRC2\_PB5**

## **0x8A—Bits[7:0] ISRC2\_PB6**

## **0x8B—Bits[7:0] ISRC2\_PB7**

## **0x8C—Bits[7:0] ISRC2\_PB8**

## **0x8D—Bits[7:0] ISRC2\_PB9**

## **0x8E—Bits[7:0] ISRC2\_PB10**

## **0x8F—Bits[7:0] ISRC2\_PB11**

## **0x90—Bits[7:0] ISRC2\_PB12**

## **0x91—Bits[7:0] ISRC2\_PB13**

## **0x92—Bits[7:0] ISRC2\_PB14**

## **0x93—Bits[7:0] ISRC2\_PB15**

## **0x94—Bits[7:0] mask1**

## **0x95—Bits[7:6] mask2**

## **0x96—Bit[7] HPD\_INT**

## **0x96—Bit[6] MSEN\_INT**

## **0x96—Bit[5] VS\_INT**

## **0x96—Bit[4] AUD\_FIFO\_FULL\_INT**

## **0x96—Bit[3] ITU656\_ERR\_INT**

## **0x96—Bit[2] EDID\_RDY\_INT**

## **0x97—Bit[7] HDCP\_ERR\_INT**

## **0x97—Bit[6] BKSV\_flag**

## **0x97—Bit[2]**

## **0x98—Bit[7]**

## **0x98—Bits[3:0]**

## **0x9C—Bits[7:0]**

## **0x9D—Bits[3:0]**

## **0xA2—Bits[7:0]**

## **0xA3—Bits[7:0]**

## **0xAF—Bit[7] HDCP\_desired**

## **0xAF—Bit[4] frame\_enc**

## **0xAF—Bit[1] ext\_HDMI\_MODE**

## **0xB0—Bits[7:0] An\_0**

## **0xB1—Bits[7:0] An\_1**

## **0xB2—Bits[7:0] An\_2**

## **0xB3—Bits[7:0] An\_3**

## **0xB4—Bits[7:0] An\_4**

## **0xB5—Bits[7:0] An\_5**

## **0xB6—Bits[7:0] An\_6**

## **0xB7—Bits[7:0] An\_7**

## **0xB7—Bit[6] ENC\_on**

## **0xB7—Bit[5] int\_HDMI\_MODE**

## **0xB7—Bit[4] keys\_read\_error**

## **0xBA—Bits[7:5] clk\_delay**

## **0xBA—Bit[4] clk\_delay**

## **0xBE—Bit[7] BCAPS**

## **0xBE—Bit[6]**

## **0xBE—Bit[5]**

## **0xBE—Bit[4]**

## **0xBE—Bits[3:2]**

## **0xBE—Bit[1]**

## **0xBE—Bit[0]**

## **0xBF—Bits[7:0] Bksv1**

## **0xC0—Bits[7:0] Bksv Byte2**

## **0xC1—Bits[7:0] Bksv3**

## **0xC2—Bits[7:0] Bksv4**

## **0xC3—Bits[7:0] Bksv5**

## **0xC4—Bits[7:0] EDID Segment**

These bits support up to 256 EDID segments that can be addressed. The requested segment address is written here before initiation of the read.

## **0xC5—Bit[7] ErrorFlag**

## **0xC5—Bit[6] AN Stop**

## **0xC5—Bit[5] HDCP Enabled**

## **0xC5—Bit[4] EDID Ready**

## **0xC5—Bit[3] I<sup>2</sup>C**

## **0xC5—Bit[2] RI**

## **0xC5—Bit[1] BKSV Update**

## **0xC5—Bit[0] PJ**

## **0xC6—Bit[4] HDMI Mode**

## **0xC6—Bit[3] HDCP Requested**

## **0xC6—Bit[2] Rx Sense**

## **0xC6—Bit[1] EEPROM Read**

## **0xC7—Bit[7] BKSV Flag**

## **0xC7—Bits[6:0] BKSV Count**

**0xC8—Bits[7:4] HDCP Controller Error**

When an error occurs in the HDCP flow, it is reported here after setting the error flag (0xC5[7]).

Table 28.

| Error Code | Error Condition                                   |
|------------|---|
| 0000       | No error  |
| 0001       | Bad receiver BKSv                                 |
| 0010       | Ri mismatch                                       |
| 0011       | Pj mismatch                                       |
| 0100       | I <sup>2</sup> C error (usually a no acknowledge) |
| 0101       | Timed out waiting for downstream repeater         |
| 0110       | Maximum cascade of repeaters exceeded             |
| 0111       | SHA-1 hash check of BKSv list failed              |
| 1000       | Too many devices connected to repeater tree       |

**0xC8—Bits[3:0] HDCP Controller State**

This information is used in troubleshooting the HDCP controller.

**0xC9—Bits[3:0] EDID Read Tries**

These bits define the number of times the EDID attempts to be read if unsuccessful.

## 2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface is provided. Up to two AD9389 devices can be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

There are five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slave devices that a data transfer sequence is coming.

The first 8 bits of data transferred after a start signal comprise a 7-bit slave address (the first 7 bits) and a single R/W bit (the eighth bit). The R/W bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device, the AD9389 acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9389 does not acknowledge.

**Table 29. Serial Port Addresses**

| Bit 7                | Bit 6          | Bit 5          | Bit 4          | Bit 3          | Bit 2          | Bit 1          |
|----------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| A <sub>6</sub> (MSB) | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> |
| 0                    | 1              | 1              | 1              | 0              | 0              | 0              |
| 0                    | 1              | 1              | 1              | 0              | 0              | 1              |

## DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read from or written to, the MSB is the first bit of the sequence.

If the AD9389 does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9389 during a read sequence, the AD9389 interprets this as the end of data. The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9389 requires that the 8-bit address of the control register of interest be written to after the slave address has been established. This control register address is the base address for subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address.

Data is read from the control registers of the AD9389 in a similar manner. Reading requires two data transfer operations:

- The base address must be written with the R/W bit of the slave address byte low to set up a sequential read operation.
- Reading (the R/W bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the AD9389, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read/write) between the slave and master without releasing the serial interface lines.

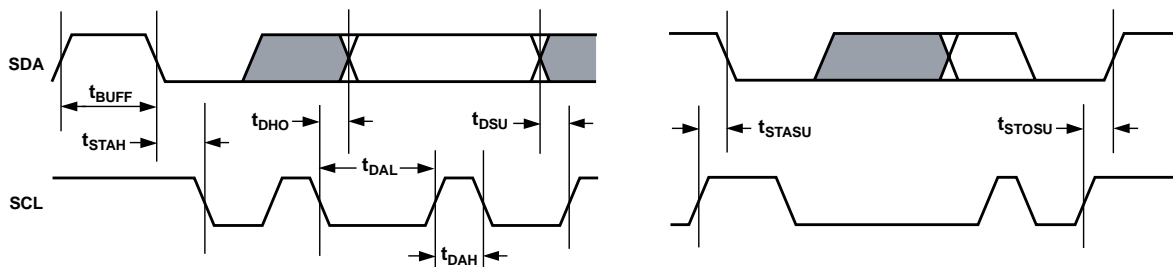


Figure 11. Serial Port Read/Write Timing

06724011



## SERIAL INTERFACE READ/WRITE EXAMPLES

Write to one control register:

- Start signal
- Slave address byte ( $\overline{R/\overline{W}}$  bit = low)
- Base address byte
- Data byte to base address
- Stop signal
- Write to four consecutive control registers
- Start signal
- Slave address byte ( $\overline{R/\overline{W}}$  bit = low)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Read from one control register:

- Start signal
- Slave address byte ( $\overline{R/\overline{W}}$  bit = low)
- Base address byte
- Start signal
- Slave address byte ( $\overline{R/\overline{W}}$  bit = high)
- Data byte from base address
- Stop signal

Read from four consecutive control registers:

- Start signal
- Slave address byte ( $\overline{R/\overline{W}}$  bit = low)
- Base address byte
- Start signal
- Slave address byte ( $\overline{R/\overline{W}}$  bit = high)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

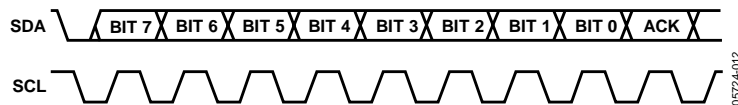


Figure 12. Serial Interface—Typical Byte Transfer

05724-012

## PCB LAYOUT RECOMMENDATIONS

The AD9389 is a high precision, high speed analog device. As such, to get the maximum performance out of the part, it is important to have a well laid out board. The following is a guide for designing a board using the AD9389.

### POWER SUPPLY BYPASSING

It is recommended to bypass each power supply pin with a 0.1  $\mu$ F capacitor. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have only one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9389, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of  $PV_{DD}$  (the clock generator supply). Abrupt changes in  $PV_{DD}$  can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups ( $V_{DD}$  and  $PV_{DD}$ ).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least  $PV_{DD}$ , from a different, cleaner power source (for example, from a 12 V supply).

It is also recommended to use a single ground plane for the entire board. Experience has shown repeatedly that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable, therefore, it is recommended to place a single ground plane under the AD9389. The location of the split should be at the receiver of the digital outputs. For this case, it is even more important to place components wisely because the current loops are much longer (current takes the path of least resistance).

### DIGITAL INPUTS

The digital inputs on the AD9389 are designed to work with 1.8 V signals, but are tolerant of 3.3 V signals. Therefore, no extra components need to be added if using 3.3 V logic.

Any noise that gets onto the HSYNC, VSYNC, or clock input traces can add jitter to the system. Therefore, minimize the trace lengths and do not run any digital or other high frequency traces near them. All TMDS lines must maintain a 50  $\Omega$  impedance trace and it is recommended that the trace lengths be as short as possible. To request a sample layout, send email to [flatpanel\\_apps@analog.com](mailto:flatpanel_apps@analog.com).

## COLOR SPACE CONVERTER (CSC) COMMON SETTINGS

Table 30. HDTV YCbCr (0 to 255) to RGB (0 to 255) (Default Setting for AD9389)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x0C            | 0x52 | 0x08            | 0x00 | 0x00            | 0x00 | 0x19           | 0xD7 |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x1C            | 0x54 | 0x08            | 0x00 | 0x3E            | 0x89 | 0x02           | 0x91 |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x00            | 0x00 | 0x08            | 0x00 | 0x0E            | 0x87 | 0x18           | 0xBD |

Table 31. HDTV YCbCr (16 to 235) to RGB (0 to 255)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x47            | 0x2C | 0x04            | 0xA8 | 0x00            | 0x00 | 0x1C           | 0x1F |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x1D            | 0xDD | 0x04            | 0xA8 | 0x1F            | 0x26 | 0x01           | 0x34 |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x00            | 0x00 | 0x04            | 0xA8 | 0x08            | 0x75 | 0x1B           | 0x7B |

Table 32. SDTV YCbCr (0 to 255) to RGB (0 to 255)

| Register | Red/Cr Coeff 1   |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|------------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18             | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x2A             | 0xF8 | 0x08            | 0x00 | 0x00            | 0x00 | 0x1A           | 0x84 |
| Register | Green/Y Coeff 1  |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20             | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x1A             | 0x6A | 0x08            | 0x00 | 0x1D            | 0x50 | 0x04           | 0x23 |
| Register | Blue/Cb Coeff. 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28             | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x00             | 0x00 | 0x08            | 0x00 | 0x0D            | 0xDB | 0x19           | 0x12 |

Table 33. SDTV YCbCr (16 to 235) to RGB (0 to 255)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x46            | 0x63 | 0x04            | 0xA8 | 0x00            | 0x00 | 0x1C           | 0x84 |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x1C            | 0xC0 | 0x04            | 0xA8 | 0x1E            | 0x6F | 0x02           | 0x1E |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x00            | 0x00 | 0x04            | 0xA8 | 0x08            | 0x11 | 0x1B           | 0xAD |

# AD9389

Table 34. RGB (0 to 255) to HDTV YCbCr (0 to 255)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x08            | 0x2D | 0x18            | 0x93 | 0x1F            | 0x3F | 0x08           | 0x00 |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x03            | 0x68 | 0x0B            | 0x71 | 0x01            | 0x27 | 0x00           | 0x00 |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x1E            | 0x21 | 0x19            | 0xB2 | 0x08            | 0x2D | 0x08           | 0x00 |

Table 35. RGB (0 to 255) to HDTV YCbCr (16 to 235)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x07            | 0x06 | 0x19            | 0xA0 | 0x1F            | 0x5B | 0x08           | 0x00 |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x02            | 0xED | 0x09            | 0xD3 | 0x00            | 0xFD | 0x01           | 0x00 |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x1E            | 0x64 | 0x1A            | 0x96 | 0x07            | 0x06 | 0x08           | 0x00 |

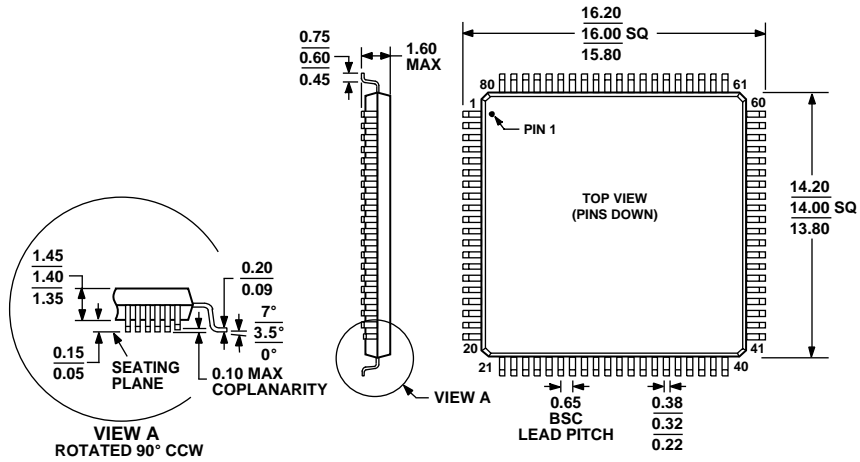
Table 36. RGB (0 to 255) to SDTV YCbCr (0 to 255)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x08            | 0x2D | 0x19            | 0x27 | 0x1E            | 0xAC | 0x08           | 0x00 |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x04            | 0xC9 | 0x09            | 0x64 | 0x01            | 0xD3 | 0x00           | 0x00 |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x1D            | 0x3F | 0x1A            | 0x93 | 0x08            | 0x2D | 0x08           | 0x00 |

Table 37. RGB (0 to 255) to SDTV YCbCr (16 to 235)

| Register | Red/Cr Coeff 1  |      | Red/Cr Coeff 2  |      | Red/Cr Coeff 3  |      | Red/Cr Offset  |      |
|----------|-----------------|------|-----------------|------|-----------------|------|----------------|------|
| Address  | 0x18            | 0x19 | 0x1A            | 0x1B | 0x1C            | 0x1D | 0x1E           | 0x1F |
| Value    | 0x07            | 0x06 | 0x1A            | 0x1E | 0x1E            | 0xDC | 0x08           | 0x00 |
| Register | Green/Y Coeff 1 |      | Green/Y Coeff 2 |      | Green/Y Coeff 3 |      | Green/Y Offset |      |
| Address  | 0x20            | 0x21 | 0x22            | 0x23 | 0x24            | 0x25 | 0x26           | 0x27 |
| Value    | 0x04            | 0x1C | 0x08            | 0x11 | 0x01            | 0x91 | 0x01           | 0x00 |
| Register | Blue/Cb Coeff 1 |      | Blue/Cb Coeff 2 |      | Blue/Cb Coeff 3 |      | Blue/Cb Offset |      |
| Address  | 0x28            | 0x29 | 0x2A            | 0x2B | 0x2C            | 0x2D | 0x2E           | 0x2F |
| Value    | 0x1D            | 0xA3 | 0x1B            | 0x57 | 0x07            | 0x06 | 0x08           | 0x00 |

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 13. 80-Lead Low Profile Quad Flat Package [LQFP] (ST-80-2)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model                      | Temperature Range | Package Description                          | Package Option |
|----------------------------|-------------------|--|----------------|
| AD9389KSTZ-80 <sup>1</sup> | 0°C to 70°C       | 80-Lead Low Profile Quad Flat Package (LQFP) | ST-80-2        |
| AD9389/PCB                 |                   | Evaluation Board                             |                |

<sup>1</sup> Z = Pb-free part.

**AD9389**

**Notes**

**NOTES**

**AD9389**

## NOTES

Purchase of licensed I<sup>2</sup>C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

©2006 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.  
D05724-0-1/06(0)



[www.analog.com](http://www.analog.com)