## Description

The AC23V8000 high performance read only memory is organized 1,048,576 x 8 bit (byte mode) and has an access time of 70/100/120ns. The low power feature allows the battery operation. The large size of 8M bit memory density is ideal for charactergenerator, data or program memory in micro-processor application. The AC23V8000 is provided as die form in waffle pack tray.

## Key features

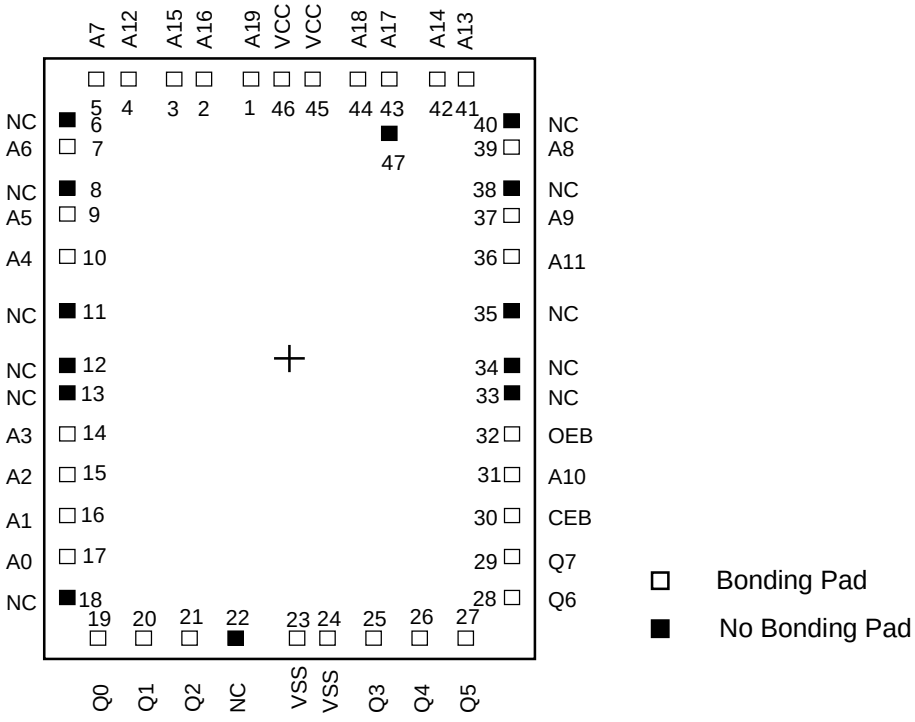
- 1,048,576 X 8bit organiszation
- Single 3.3V power supply operation
- Access Time : 70/100/120ns (Max)
- Standby Current : 50㎂(Max)
- Operating Current : 35㎃(Max)
- TTL compatible inputs and outputs
- 3-State outputs for wired-OR expansion
- Programmable CE or OE pin
- Fully static operation
- Package
  AC23V8000 : Die in waffle pack tray

## Pin Description

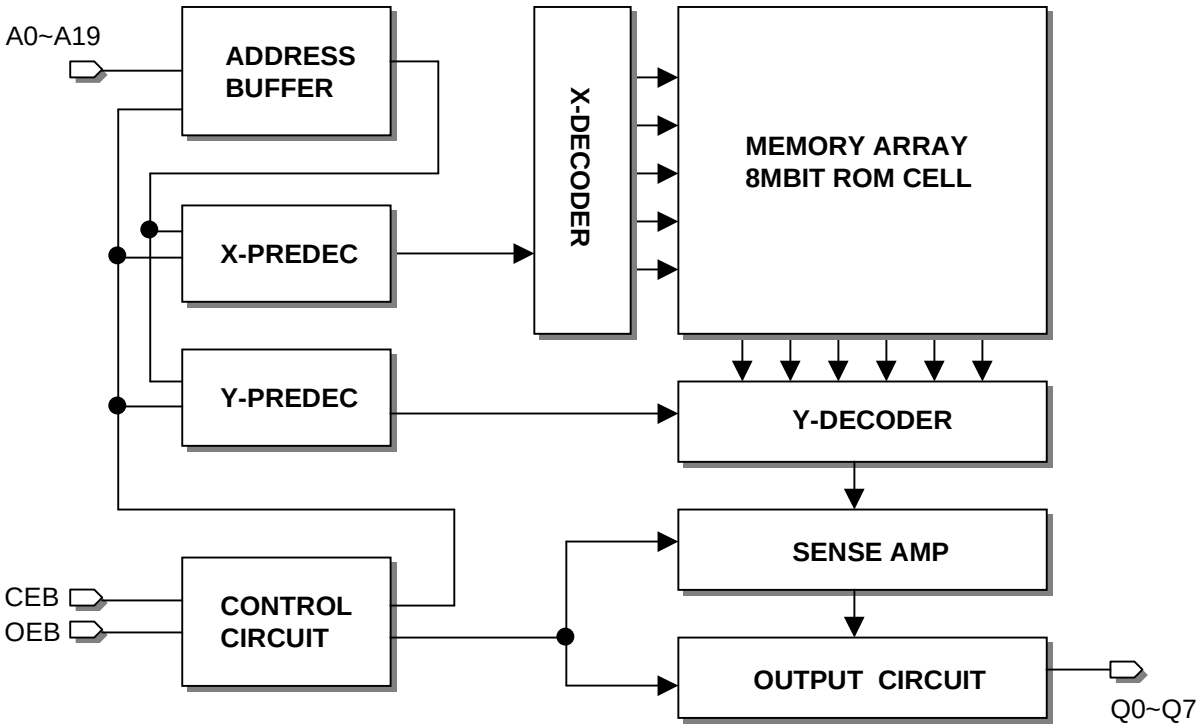
| Pin | Function |
|---|---|
| A0~A19 | Address inputs |
| Q0~Q7 | Data Outputs |
| CEB* | Chip Enable input |
| OEB* | Output Enable input |
| VCC | Power supply |
| VSS | Ground |

* User selectable polarity
- CEB : CE/CEB
- OEB : OE/OEB

## Pin Configuration



## ❑ Block Diagram



## ❑ Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | -10 ~ 80 | °C |
| $T_{STG}$ | Storage Temperature | -55 ~ 150 | °C |
| $V_{CC}$ | Supply Voltage to Ground Potential | -0.3 ~ 4.5 | V |
| $V_{OUT}$ | Output Voltage | -0.3~Vcc+0.3 | V |
| $V_{IN}$ | Input Voltage | -0.3~Vcc+0.3 | V |

Stress above those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ❑ Recommended DC Operating Conditions(VCC=3.3±0.3V, $T_A$=0~70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Vss | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | | Vcc+0.3 | V |
| $V_{IL}$ | Input Low Voltage | -0.3 | | 0.8 | V |

## ❑ DC Electrical Characteristics(VCC=3.3±0.3V, $T_A$=0~70 °C)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$=-0.4mA | 2.4 | | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$=2.1mA | | | 0.4 | V |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$=0V to $V_{CC}$ | | | ±10 | uA |
| $I_{OL}$ | Output Leakage Current | $V_{OUT}$=0V to $V_{CC}$ | | | ±10 | uA |
| $I_{CC}$ | Operating Supply Current (tRC=100ns) | CEB=OEB=$V_{IL}$ All Output Open | | | 35 | mA |
| $I_{SB1}$ | Standby Current(TTL) | CEB=$V_{IH}$, all Output Open | | | 500 | uA |
| $I_{SB2}$ | Standby Current(CMOS) | CEB=$V_{CC}$, all Output Open | | | 50 | uA |

## ❑ Capacitance($T_A$=25°C , f=1.0MHz)

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_I$ | Input Capacitance | VIN = 0V | | 10 | pF |
| $C_O$ | Output Capacitance | VOUT = 0V | | 10 | pF |

Capacitance is periodically sampled and not 100% tested

## ❑ Function Table

| CE/$\overline{CE}$ | OE/$\overline{OE}$ | Mode | Data | Power |
|---|---|---|---|---|
| L/H | X | Standby | High Z | Standby |
| H/L | H/L | Operating | $D_{OUT}$ | Active |
| | L/H | Output Disable | High Z | |

## ❑ AC Characteristics(VCC=3.3±0.3V, $T_A$=0~70°C )

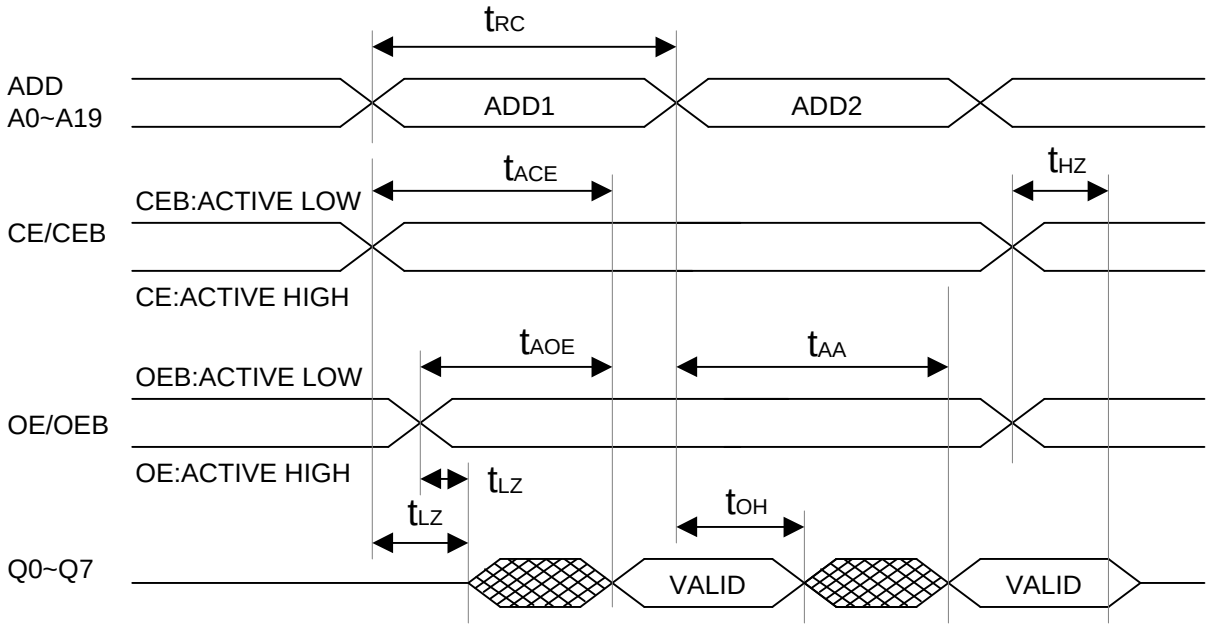
| Symbol | Parameter | 70ns | | 100ns | | 120ns | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| tRC | Read cycle time | 70 | | 100 | | 120 | | ns |
| tACE | Chip enable access time | | 70 | | 100 | | 120 | ns |
| tAA | Address access time | | 70 | | 100 | | 120 | ns |
| tAOE | Output enable access time | | 35 | | 50 | | 60 | ns |
| tOH | Output hold time from address change | 0 | | 0 | | 0 | | ns |
| tHZ | Output or chip disable to output High-Z | | 20 | | 20 | | 20 | ns |
| tLZ | Output or chip Enable to output Low-Z | 10 | | 10 | | 10 | | ns |

## ❑ AC Test Condition

- Input pulse level 0.4V to 2.4V
- Input rise and fall time 10ns
- Input and output timing level 1.5V
- Output load 1 TTL gate and CL=100pF(70ns product CL=30pF)

## Timing Waveforms

### READ MODE



## Revision History

| Rev No. | Date | Contents |
|---|---|---|
| rev0 | 10-Mar-2001 | |
| rev1 | 09-Jan-2002 | Package dimension modified |
| rev2 | 16-June-2003 | Package exempted and pad diagram added |