High Performance Step-Down DC-DC Converter With Adjustable Output Voltage

DESCRIPTION

The SiP12101 is a high efficiency 600 mA step down converter with internal low on resistance power MOSFET switch and synchronous rectifier transistors. It is designed to convert one cell Lilon battery or three cell alkaline battery voltages to an adjustable dc output. The integrated high frequency error amplifier with internal compensation minimizes external components.

2 MHz switching permits use of small external inductor and capacitor sizes allowing one of the smallest solutions.

The SiP12101 is available in the 10 pin MSOP and is specified to operate over the industrial temperature range of - 40 °C to 85 °C.

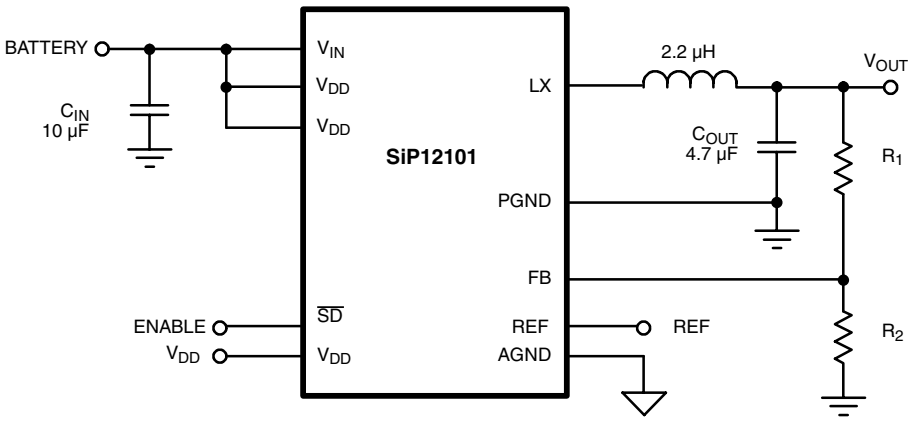
FEATURES

- 2 MHz PWM operation
- Integrated MOSFET switches
- 2.6 V to 6.0 V input voltage range
- Minimal number of external components
- Up to 96 % conversion efficiency
- 600 mA load capability
- 100 % cuty cycle allows low dropout
- Integrated compensation circuit
- Over-current protection
- Shutdown current < 2 mA
- Thermal shutdown
- Integrated UVLO
- 10 pin MSOP

APPLICATIONS

- PDAs/palmtop PCs
- LCD podules
- Portable image scanners
- GPS receivers
- Smart phones
- MP3 players
- 3G cell phone
- Digital cameras

TYPICAL APPLICATIONS CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Voltages Referenced to AGND = 0 V			
V_{IN}, V_{DD}		6.2	V
Lx, $\overline{SD}$, FB, C_{REF}		- 0.3 to 6.2 (or to V_{DD} + 0.3 whichever is less)	
GND		- 0.3 to + 0.3	
ESD Rating		2	kV
Storage Temperature		- 65 to 125	°C
Operating Junction Temperature		150	
Power Dissipation (Package)[a]	10-pin MSOP[b]	481	mW
	10-pin MLP33	915	
Thermal Impedance (Θ_{JA})	10-Pin MSOP	135	°C/W
Peak Inductor Current		1.8	A

Notes:
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.4 mW/°C above 85 °C.
c. Derate 14 mW/°C above 85 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
V_{IN} Range	2.6 to 5.5	V
C_{IN}	10 µF ceramic	
C_{OUT}	4.7 µF ceramic	
Inductor	2.2	µH
Load Current	0 to 600	mA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified - 40 °C to 85 °C, $V_{IN} = V_{DD}$, C_{IN} = 10 µF, C_{OUT} = 4.7 µF L = 2.2 µH, 2.6 V ≤ V_{IN} ≤ 5.5 V, R_1 = 11.3 kΩ, R_2 = 20 kΩ		Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Under Voltage Lockout (UVLO)							
Under Voltage Lockout (turn-on)		V_{IN} rising		2.3		2.5	V
Hysteresis					0.1		
Shutdown ($\overline{SD}$)							
Logic High	V_{SDH}			1.6			V
Logic Low	V_{SDL}					0.4	
Delay to Output[c]	t_{en}	Settle within ± 2 % accuracy $\overline{SD}$ rising t_r < 1 µs	R_L = 3.3 Ω			100	µs
			R_L = 51 Ω		100		
Pull Down	I_{SD}	Input at V_{IN}					µA
Oscillator							
Frequency	f_{OSC}			1.6	2	2.4	MHz
Error Amplifier (FB Pin)							
FB Voltage Accuracy	V_{FB}		T_A = 25 °C	1.185	1.215	1.245	V
			T_A = - 40 °C to 85 °C	1.170		1.260	
Power Supply Rejection	PSRR	V_{IN} = 2.6 V to 5.5 V_{DC}			60		db
Input Bias Current	I_{FB}	V_{FB} = 1.25 V		- 1	0.01	1	µA

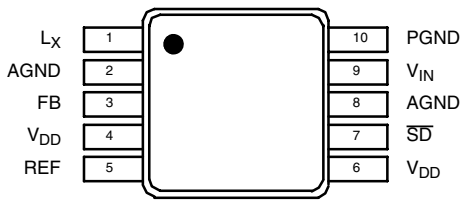
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified - 40 °C to 85 °C, $V_{IN} = V_{DD}$, C_{IN} = 10 µF, C_{OUT} = 4.7 µF L = 2.2 µH, 2.6 V ≤ V_{IN} ≤ 5.5 V, R_1 = 11.3 kΩ, R_2 = 20 kΩ		Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Converter Operation							
Maximum Output Current	I_{LOAD}	V_{IN} = 3.6 V		600			mA
Dropout Voltage[e]	V_{DD}	V_{IN} = 2.6 V, I_{OUT} = 600 mA			190	300	mV
Closed Loop Bandwidth	BW				300		kHz
Load Regulation[c]		V_{IN} = 3.6 V, V_{OUT} = 1.9 V at 25 °C I_{OUT} = 30 mA to 600 mA			0.5		%
Line Regulation		V_{OUT} = 3.0 V, V_{IN} = 3.5 V to 5.5 V			± 0.1		%/V
Maximum Inductor Peak Current Limit	I_{Lpk}				1500		mA
On Resistance - P-Channel and N-Channel	$R_{DS(on)}$	V_{IN} = 3.6 V			250		mΩ
					250		
Output Ripple Voltage		0.05 Ω $C_{OUT(ESR)}$	I_{OUT} = 600 mA		60		mV_{p-p}
Efficiency		V_{IN} = 3.6 V, V_{OUT} = 3.3 V	I_{OUT} = 600 mA		90		%
Frequency		I_{OUT} ≥ 30 mA		20			kHz
Supply Current							
Input Supply Current	I_{SUPPLY} (V_{DD} & V_{IN})	I_{OUT} = 0 mA, V_{IN} = 3.6 V, (not switching, FB = GND)			450	750	µA
Shutdown Supply Current	I_{SD}	$\overline{SD}$ = Low				2	
Thermal Shutdown							
Thermal Shutdown Temperature[c]	$T_{J(S/D)}$				165		°C
Thermal Hysteresis[c]					20		

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
c. Guaranteed by design.
d. Settling times, t_s, apply after t_{en}.
e. Bypass is a device mode of operation, in which, the device is in 100 % duty cycle.

PIN CONFIGURATION

MSOP-10



Top View

PIN DESCRIPTION

Pin Number	Name	Function
1	L_X	Inductor connection
2	AGND	Low power analog ground
3	FB	Output voltage feedback
4	V_{DD}	Input supply voltage for the analog circuit.
5	REF	Internal reference, no connection should be made to this pin.
6	V_{DD}	Input supply voltage for the analog circuit.
7	$\overline{SD}$	Logic low disables IC and reduces quiescent current to below 2 µA
8	AGND	Must be connected to AGND.
9	V_{IN}	Input supply voltage
10	PGND	Low impedance power ground

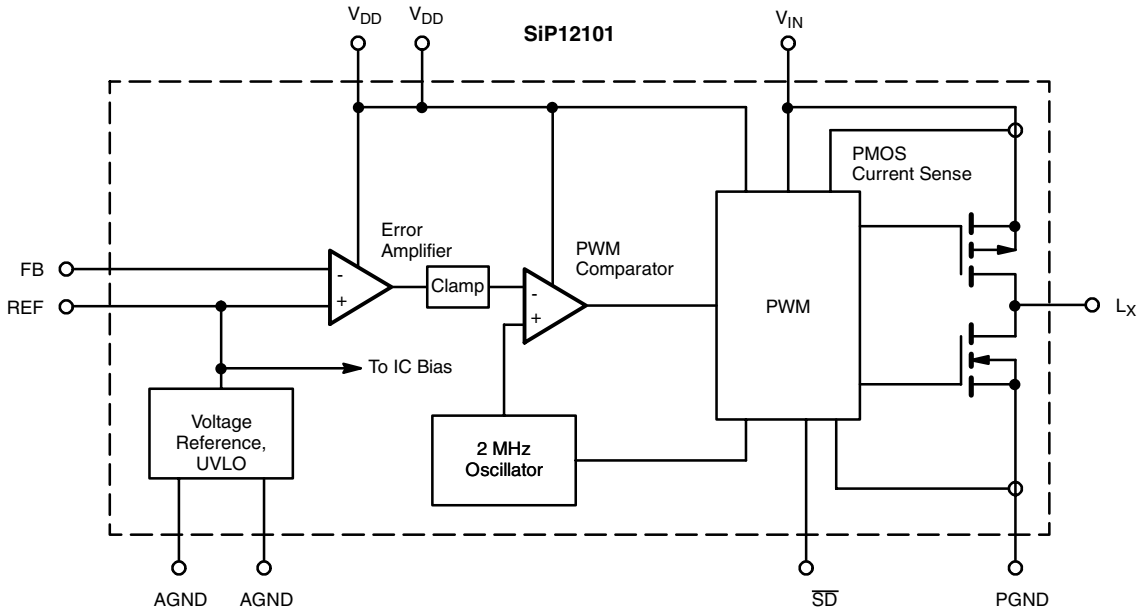
ORDERING INFORMATION

Part Number	Marking	Temperature	Package
SiP12101DH-T1	2101	- 40 °C to 85 °C	MSOP-10

Additional voltage options are available.

Eval Kit	Temperature Range	Board
SiP12101DB	- 40 °C to 85 °C	Surface Mount

FUNCTIONAL BLOCK DIAGRAM



DETAIL OPERATION

General

The SiP12101 is a high efficiency synchronous dc-dc converter that is ideally suited for lithium ion battery or three cell alkaline applications, as well as step-down of 3.3 V or 5.0 V supplies. The major blocks of the SiP12101 are shown in the Functional Block Diagram. The 0.25 Ω internal MOSFETs switching at a frequency of 2 MHz minimize PC board space while providing high conversion efficiency and performance. The high frequency error-amplifier with built-in loop compensation minimizes external components and provides rapid output settling times of < 30 µs. Sensing of the inductor current for control is accomplished internally without power wasting resistors.

Start-Up

When voltage is applied to V_{IN} and V_{DD}, the under-voltage lockout (UVLO) circuit prevents the oscillator and control circuitry from turning on until the voltage on the exceeds 2.4 V. With a typical UVLO hysteresis of 0.1 V, the converter operates continuously until the voltage on V_{IN} drops below 2.3 V, whereupon the converter shuts down. This hysteresis prevents false start-stop cycling as the input voltage approaches the UVLO switching threshold. The start-up sequence occurs after $\overline{SD}$ switches from LOW to HIGH with V_{IN} applied, or after VIN rises above the UVLO threshold and $\overline{SD}$ is a logic HIGH.

PWM

SiP12101 operates as a 2 MHz fixed frequency voltage mode converter. An NMOS synchronous rectification MOSFET transistor provides very high conversion efficiency for large load currents by minimizing the conduction losses. Output load currents can range from 0 to 600 mA.

The error amplifier and comparator control the duty cycle of the PMOS MOSFET to continuously force the REF pin and FB pin voltages to be equal. As the input-to-output voltage difference drops, the duty cycle of the PMOS MOSFET can reach 100 % to allow system designers to extract the maximum stored energy from the battery. The dropout voltage is 190 mV at 600 mA.

During each cycle, the PMOS switch current is limited to a maximum of 1.5 A (typical) thereby protecting the IC while continuing to force maximum current into the load.

Oscillator

The internal oscillator provides for a fixed 2 MHz switching frequency.

Dynamic Output Voltage Control (REF)

The SiP12101 is designed with an adjustable output voltage which has a change of V_{FB} to V_{IN} - V_{DROP}. V_{OUT} is defined according to the following relationship:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$$

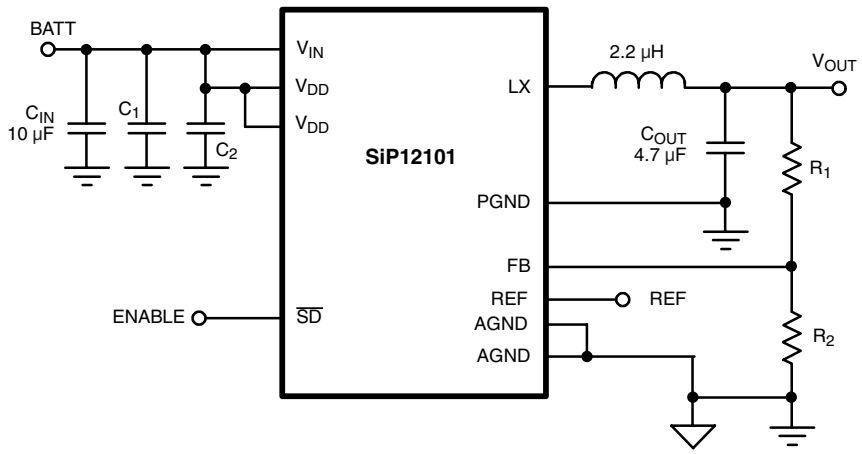
Converter Shutdown ($\overline{SD}$ pin)

With logic LOW level on the $\overline{SD}$ pin, the SiP12101 is shutdown. Shutdown reduces current consumption to less than 2 µA by shutting off all of the internal circuits. Both the PMOS and NMOS transistors are turned off. A logic HIGH enables the IC to start up as described in "Start-up" section.

Thermal Shutdown

The SiP12101 includes thermal shutdown circuitry, which turns off the regulator when the junction temperature exceeds 165 °C. Once the junction temperature drops below 145 °C, the regulator is enabled. If the condition causing the over temperature, the SiP12101 begins thermal cycling, turning the regulator on and off in response to junction temperature. Restart from a thermal shutdown condition is the same as described in the "Start-up" section.

APPLICATIONS CIRCUIT



C_{IN} = 10 µF, Ceramic, Murata GRM42-2X5R106K16
C_1, C_2 = 0.01 µF, Vishay VJ0603Y 104KXXAT
C_{OUT} = 4.7 µF, Ceramic, Murata GRM42-6X5R475K16
R_1 = 8.2 kΩ, Vishay CRCW06031132F
R_2 = 20 kΩ, Vishay CRCW06032002F
L_1 = 2.2 µH, Toko A914BYW-2R2M

TYPICAL CHARACTERISTICS

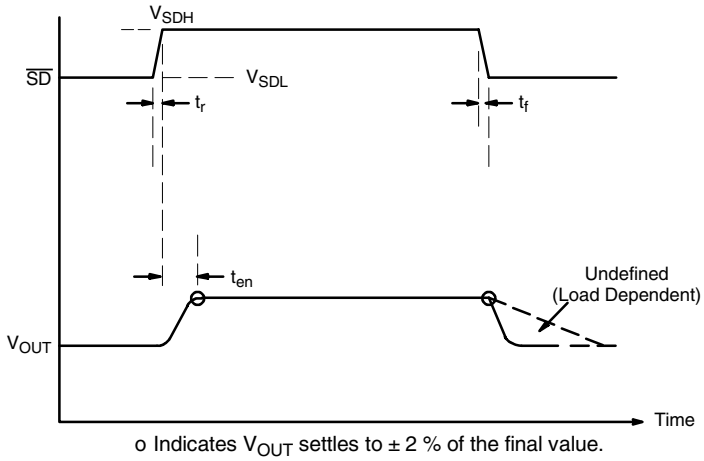
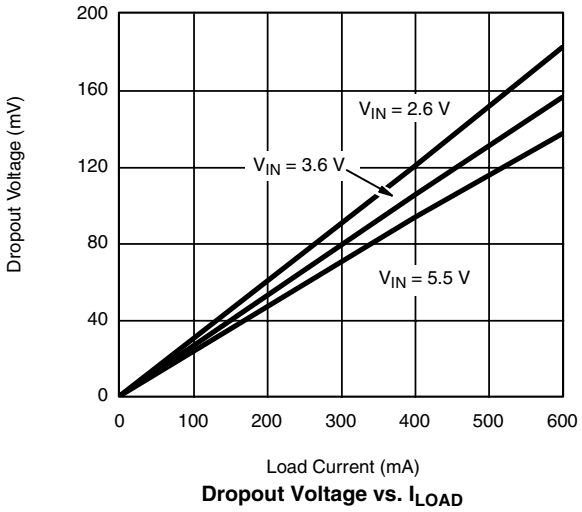
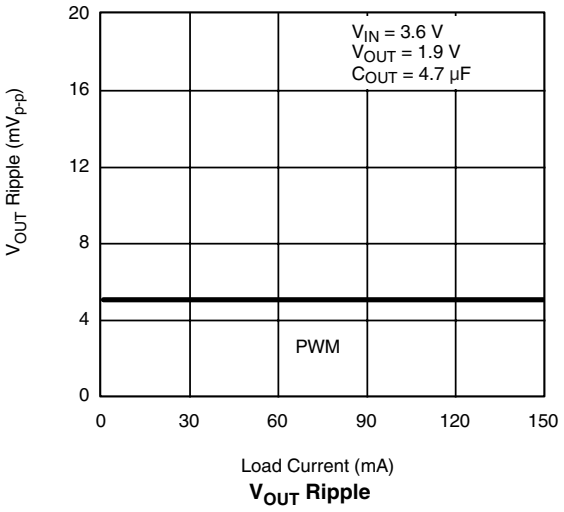


Figure 1. PWM Mode V_{OUT} Settling

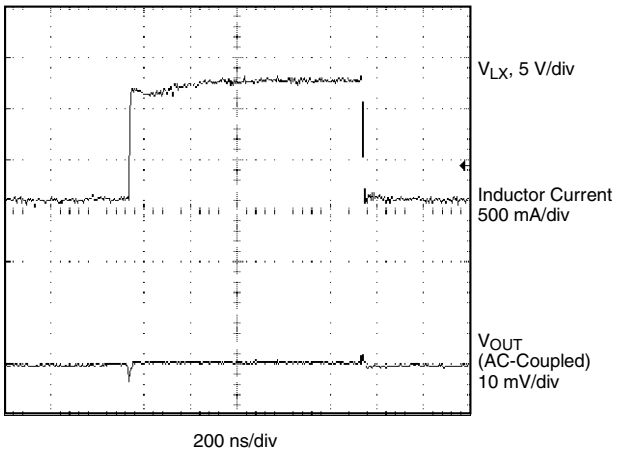


Dropout Voltage vs. I_{LOAD}

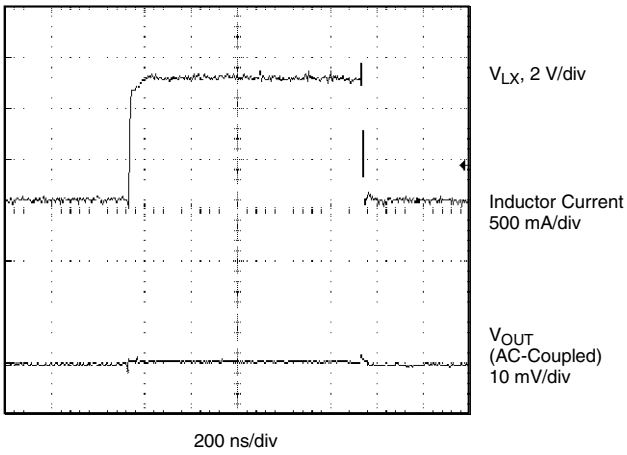


V_{OUT} Ripple

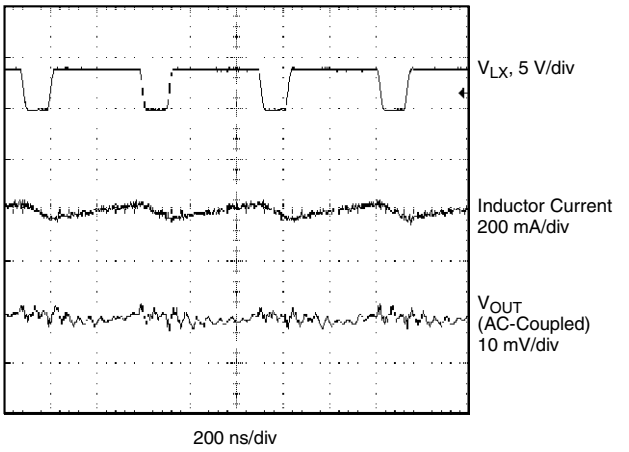
TYPICAL SWITCHING WAVEFORMS (V_{IN} = 3.6 V, V_{OUT} = 3.0 V)



Heavy-Load Switching Waveforms
I_{OUT} = 600 mA

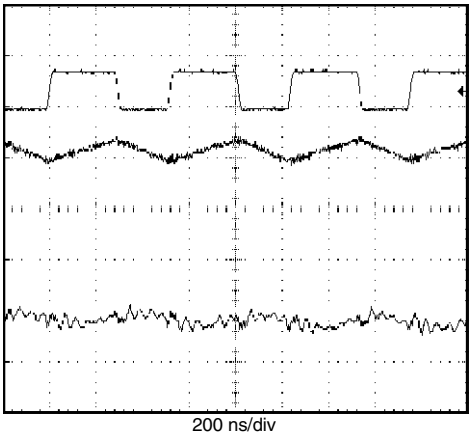


Medium-Load Switching Waveforms
I_{OUT} = 300 mA

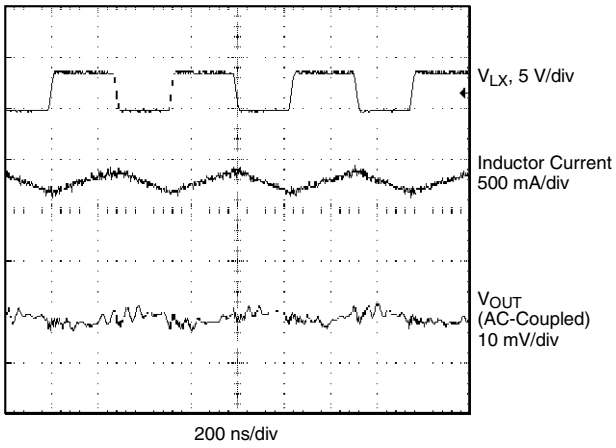


Light-Load Switching Waveforms
I_{OUT} = 0 mA

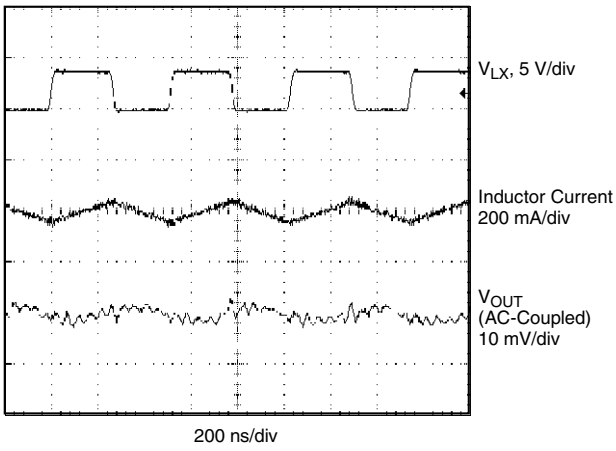
TYPICAL SWITCHING WAVEFORMS (V_{IN} = 3.6 V, V_{OUT} = 1.9 V)



Heavy-Load Switching Waveforms
I_{OUT} = 600 mA

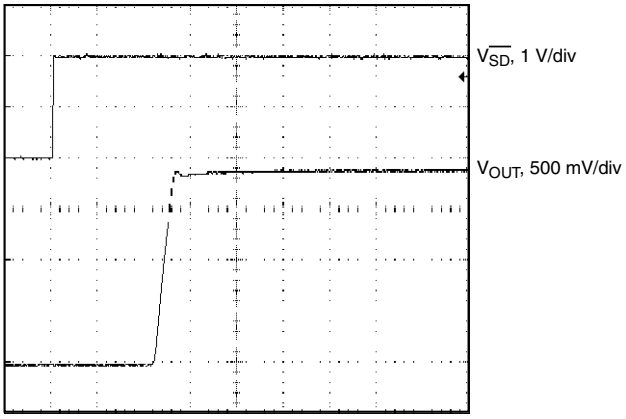


Medium-Load Switching Waveforms
I_{OUT} = 300 mA

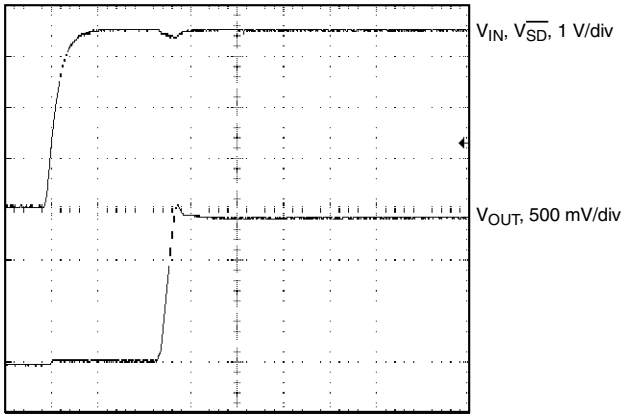


Light-Load Switching Waveforms
I_{OUT} = 0 mA

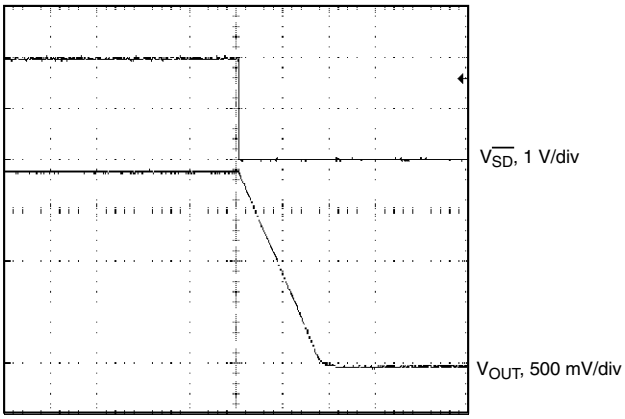
TYPICAL START-UP AND SHUTDOWN TRANSIENT WAVEFORMS (V_{IN} = 3.6 V, V_{OUT} = 1.9 V)



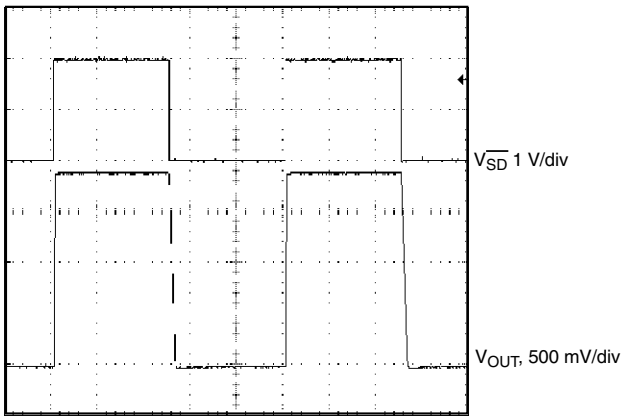
Start-Up, R_{LOAD} = 4 Ω



Start-Up, V_{IN} = $V_{\overline{SD}}$ = 3.6 V, R_{LOAD} = 4 Ω

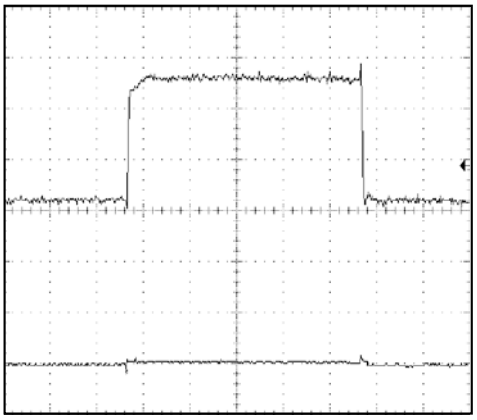


Shutdown, R_{LOAD} = 4 Ω



Enable Switching, R_{LOAD} = 4 Ω

TYPICAL LOAD TRANSIENT WAVEFORMS (V_{IN} = 3.6 V, V_{OUT} = 1.9 V)



Load Transient
I_{LOAD} = 30 to 500 mA, L = 2.2 µH

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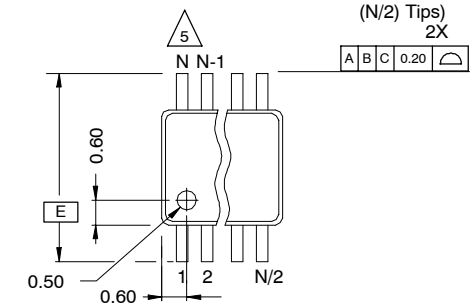
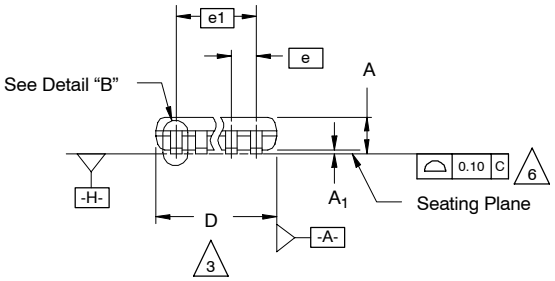
MSOP: 10-LEADS (POWER IC ONLY)

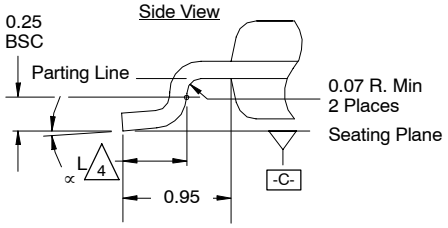
JEDEC Part Number: MO-187, (Variation AA and BA)



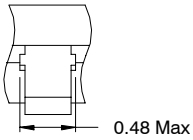
Top View



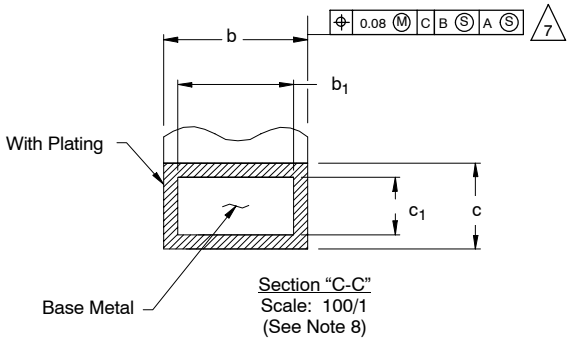
Side View



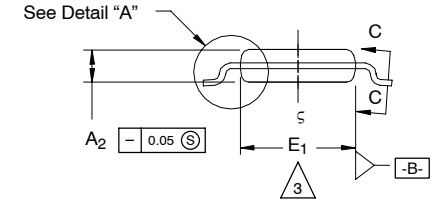
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	–	–	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	–	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	–	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

ECN: S-40082—Rev. A, 02-Feb-04
DWG: 5922

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