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FUJITSU

DATA SHEET

MB85326-60/-70/-80

CMOS 4M x 36 Fast Page Mode DRAM Module

CMOS 4,194,304 x 36 Bit Fast Page Mode DRAM Module

The Fujitsu MB85326 is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of nine MB8117400 devices. The MB85326 is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85326 are the same as the MB8117400 which features fast page mode operation. For ease of memory expansion, the MB85326 is offered in a 72–pad Single In–line Memory Module package (SIMM).

PRELIMINARY

See page 7

MSS–72P–P30

PRODUCT LINE & FEATURES

Parameter	MB85326-60	MB85326-70	MB85326-80
$\overline{RAS}$ Access Time	60ns max.	70ns max.	80ns max.
Random Cycle Time	110ns min.	130ns min.	150ns min.
Address Access Time	30ns max.	35ns max.	40ns max.
$\overline{CAS}$ Access Time	15ns max.	18ns max.	20ns max.
Fast Page Mode Cycle Time	40ns min.	45ns min.	50ns min.
Power Dissipation • Operating mode	5940mW max.	4950mW max.	4208mW max.
• Standby mode	99mW max. (TTL level) / 50mW max. (CMOS level)		

- Organization :
  4,194,304 words x 36 bits
- Memory :
  MB8117400, 9 pcs
- Refresh :
  2048 refresh cycles every 32ms
- Decoupling Capacitor :
  0.22 µF, 9 pcs
- Package and Ordering Information:
  72–pad SIMM, order as
  MB85326–xxPJPBK
  (PJPBK = Gold Pad)

DQ0	2	1	VSS
DQ2	4	3	DQ1
DQ4	6	5	DQ3
DQ6	8	7	DQ5
VCC	10	9	DQ7
A1	12	11	A0
A3	14	13	A2
A5	16	15	A4
DQ8	18	17	VSS
DQ10	20	19	DQ9
DQ12	22	21	DQ11
DQ14	24	23	DQ13
VCC	26	25	DQ15
A7	28	27	A6
A9	30	29	A8
A10	32	31	VSS
DQ17	34	33	DQ16
DQ19	36	35	DQ18
DQ21	38	37	DQ20
DQ23	40	39	DQ22
VSS	42	41	NC
NC	44	43	$\overline{OE0}$
NC	46	45	$\overline{WE0}$
DQ24	48	47	VCC
DQ26	50	49	DQ25
DQ28	52	51	DQ27
DQ30	54	53	DQ29
VSS	56	55	DQ31
NC	58	57	$\overline{RAS0}$
NC	60	59	$\overline{CAS0}$
DQ32	62	61	VCC
DQ34	64	63	DQ33
NC	66	65	DQ35
NC	68	67	NC
NC	70	69	NC
VSS	72	71	NC

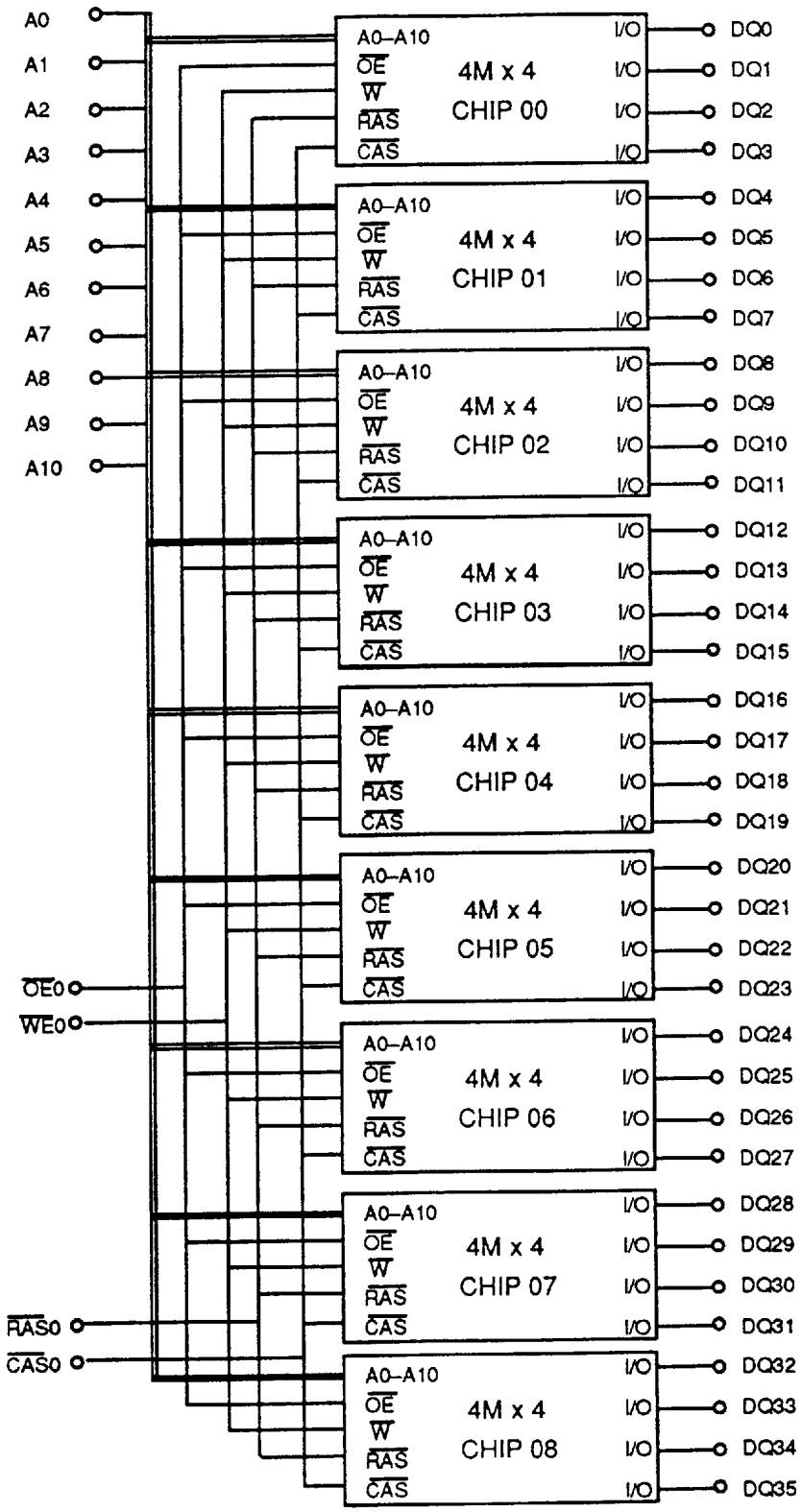
ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	–1.0 to +7.0	V
Input Voltage	VIN	–1.0 to +7.0	V
Output Voltage	VOUT	–1.0 to +7.0	V
Short Circuit Output Current	IOUT	50	mA
Power Dissipation	PD	9.0	W
Storage Temperature	TSTG	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Value			Unit	Ambient Operating Temp.
			Min	Typ	Max		
Supply Voltage	1	VCC	4.5	—	5.5	V	*2 0 °C to 70 °C
		VSS	0	—	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs *1	1	VIL	−0.5	—	0.8	V	

*1 : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.
*2 : Ambient temp. depend on cycle time and cooling conditions.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Notes	Symbol	Conditions	Values			Unit
					Min	Typ	Max	
Output High Voltage		1	VOH	IOH = −5mA	2.4	—	—	V
Output Low Voltage		1	VOL	IOL = 4.2mA	—	—	0.4	V
Input Leakage Current	$\overline{RAS}$, $\overline{WE}$		II(L)	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V; all other pins not under test = 0V	−50	—	50	µA
	$\overline{CAS}$, $\overline{OE}$							
	ADD				−60	—	60	
Output Leakage Current			IO(L)	0V ≤ VOUT ≤ 5.5V; Data out disabled	−10	—	10	µA
Operating Current (Average power supply current)	MB85326-60	2	ICC1	$\overline{RAS}$ & $\overline{CAS}$ cycling; tRC = min.	—	—	1080	mA
	MB85326-70						900	
	MB85326-80						765	
Standby Current (Power supply current)	TTL Level		ICC2	$\overline{RAS}$ = $\overline{CAS}$ = VIH	—	—	18	mA
	CMOS Level			$\overline{RAS}$ = $\overline{CAS}$ ≥ VCC-0.2V			9	
Refresh Current #1 (Average power supply current)	MB85326-60	2	ICC3	$\overline{CAS}$ = VIH; $\overline{RAS}$ = cycling; tRC = min.	—	—	1080	mA
	MB85326-70						900	
	MB85326-80						765	
Fast Page Mode Current	MB85326-60	2	ICC4	$\overline{RAS}$ = VIL; $\overline{CAS}$ = cycling; tPC = min.	—	—	720	mA
	MB85326-70						630	
	MB85326-80						585	
Refresh Current #2 (Average power supply current)	MB85326-60	2	ICC5	$\overline{RAS}$ = cycling; $\overline{CAS}$-before-$\overline{RAS}$ tRC = min.	—	—	1080	mA
	MB85326-70						900	
	MB85326-80						765	

CAPACITANCE (T_A = 25°C, f = 1MHz, VCC=5.0V)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10	CIN1	—	80	pF
Input Capacitance, $\overline{RAS}$0	CIN2	—	72	pF
Input Capacitance, $\overline{CAS}$0	CIN3	—	74	pF
Input Capacitance, $\overline{WE}$0	CIN4	—	72	pF
Input Capacitance, $\overline{OE}$0	CIN5	—	72	pF
I/O Capacitance, (DQ0-35)	CDQ	—	14	pF

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB85326-60		MB85326-70		MB85326-80		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	32	—	32	—	32	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	130	—	150	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	174	—	200	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	60	—	70	—	80	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	15	—	17	—	20	ns
6	Column Address Access Time	8,9	t_{AA}	—	30	—	35	—	40	ns
7	Output Hold Time		t_{OH}	3	—	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	15	—	17	—	20	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	50	—	60	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	80	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	17	—	20	—	ns
14	$\overline{CAS}$ to RAS Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to CAS Delay Time	11,12	t_{RCD}	20	45	20	53	20	60	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	15	—	17	—	20	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	80	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	t_{CPN}	10	—	10	—	10	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	10	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	ns
23	Column Address Hold Time from $\overline{RAS}$		t_{AR}	35	—	35	—	35	—	ns
24	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	30	15	35	15	40	ns
25	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	40	—	ns
26	Column Address to $\overline{CAS}$ Lead time		t_{CAL}	30	—	35	—	40	—	ns
27	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
30	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
31	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	ns
32	Write Hold Time from $\overline{RAS}$		t_{WCR}	35	—	35	—	35	—	ns
33	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	ns
34	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	17	—	20	—	ns
35	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	17	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

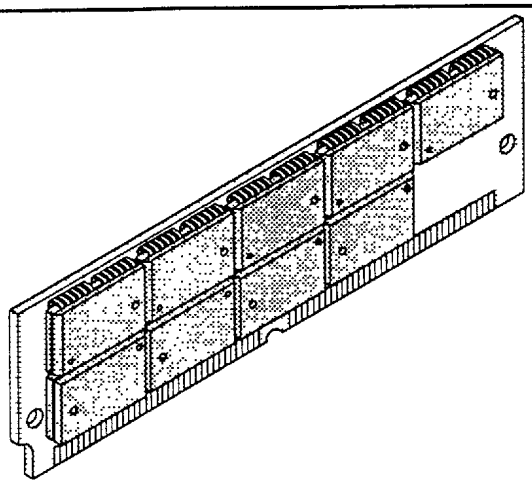
No.	Parameter	Notes	Symbol	MB85326-60		MB85326-70		MB85326-80		Unit
				Min	Max	Min	Max	Min	Max	
36	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
37	DIN Hold Time		t_{DH}	15	—	15	—	15	—	ns
38	Data Hold Time from $\overline{RAS}$		t_{DHR}	35	—	35	—	35	—	ns
39	$\overline{RAS}$ to $\overline{WE}$ Delay Time	20	t_{RWD}	80	—	92	—	105	—	ns
40	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	t_{CWD}	35	—	39	—	45	—	ns
41	Column Address to $\overline{WE}$ Delay Time	20	t_{AWD}	50	—	57	—	65	—	ns
42	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	5	—	5	—	5	—	ns
43	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
44	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	12	—	15	—	ns
45	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
46	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	10	—	10	—	10	—	ns
47	Access Time from $\overline{OE}$	9	t_{OEA}	—	15	—	17	—	20	ns
48	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	15	—	17	—	20	ns
49	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	5	—	7	—	10	—	ns
50	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	5	—	5	—	5	—	ns
51	$\overline{OE}$ to Data In Delay Time		t_{OED}	15	—	17	—	20	—	ns
52	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	ns
53	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	ns
54	Fast Page Mode $\overline{RAS}$ Pulse width		t_{RASP}	—	100000	—	100000	—	100000	ns
61	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	50	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	80	—	89	—	100	—	ns
63	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	35	—	40	—	45	ns
64	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	10	—	ns
65	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	45	—	ns
66	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	55	—	62	—	70	—	ns

Notes:

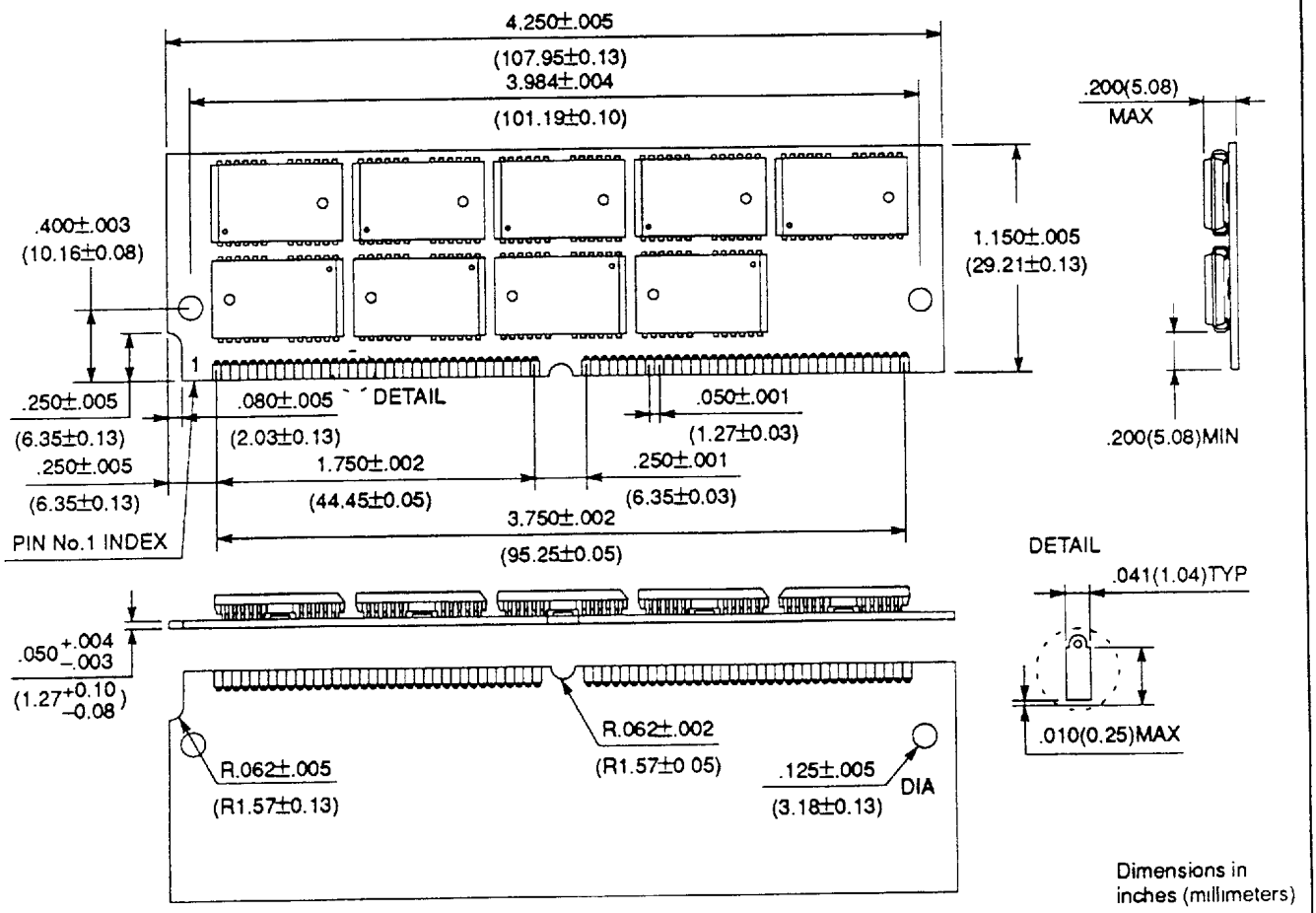
1. Referenced to VSS.
2. ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open. ICC depends on the number of address change as $\overline{RAS}$ = VIL , $\overline{CAS}$ = VIH and VIL > −0.3V.
   ICC1, ICC3, ICC4 and ICC5 are specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH. ICC2 is specified during $\overline{RAS}$=VIH and VIL>−0.3V.
3. An Initial pause ($\overline{RAS}$ =$\overline{CAS}$ =VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than tCPA (max).
19. Assuemes that $\overline{CAS}$ –before–$\overline{RAS}$ refresh.
20. Assuemes that test mode function.

PACKAGE DIMENSIONS

(Suffix: PJPBK)



72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P30)



Dimensions in
inches (millimeters)