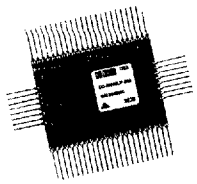
DDC
ILC DATA DEVICE CORPORATION®

DD-42900



ARINC 429 Microprocessor Interface Device

This Preliminary data sheet provides detailed functional capabilities for product currently in prototype production. These specifications are being provided to allow for electrical design, layout and operation.

DESCRIPTION

DDC's DD-42900 provides a complete and flexible interface between a microprocessor and ARINC 429 data bus. The 42900 interfaces to a processor through a 128 x 32 bit static RAM as well as four 32 x 32 receive FIFO's and two 32 x 32 transmit FIFO's. The 42900 can be easily interfaced to 8- or 16-bit processors via a buffered shared RAM configuration.

The 42900 supports four ARINC 429 Receive channels (Rx0, Rx1, Rx2 and Rx3) and each receive data independently. The recieve data rates (high or low speed) for channel Rx0 and Rx1 can be programmed independently from Rx2 and Rx3. The 42900 can decode and sort data based on the ARINC 429 Label and SDI bits via the Data Match Processor and store it in RAM and/or FIFO's via the Data Store Processor.

The 42900 supports two ARINC 429 Transmit channels (Tx0 and Tx1) and can transmit data independently. The transmit data rate can be programmed independently as well. There are two 32 x 32 bit FIFO's for each of the transmitters for sending out data.

The device has the capability of programming three general purpose interrupts as well as generating an interrupt based on an error condition. The general purpose interrupts can be programmed to trigger other external hardware. They can either be LEVEL triggered or PULSE triggered.

The features built into the DD-42900 enable the user to off-load the host processor and use that processing time to do other more important duties than polling the ARINC 429 Bus. The decoding and sorting of data allows the user to gather data much quicker that past designs. If the user requires a microprocessor in the avionics box, this device will enable a clean and quick design.

FEATURES

- ***Four ARINC 429 Receive Channels***
- ***128 x 32 Shared RAM Interface***
- ***Label and Destination Decoding and Sorting***
- ***Two ARINC 429 Transmit Channels***
- ***Two 32 x 32 Transmit FIFO's***
- ***Interfaces Easily to 8- or 16-Bit Microprocessors***
- ***Built-in Fault Detection Circuitry***

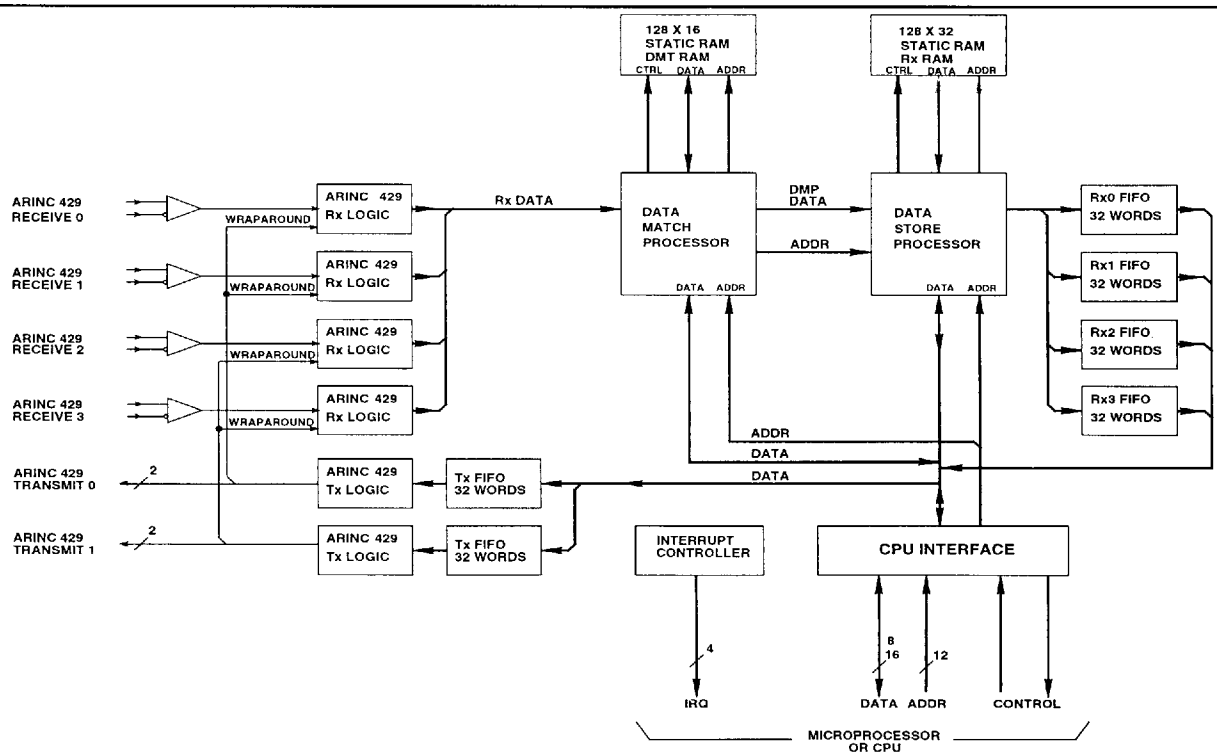


FIGURE 1. DD-42900 BLOCK DIAGRAM

ARINC 429 RECEIVERS

The DD-42900 supports four ARINC 429 inputs, designated Receive channels 0 through 3 (Rx0, Rx1, Rx2 and Rx3). The architecture of each of the four receiver circuits is identical and each receive data independently. ARINC 429 data is directly received into the DD-42900 with no additional circuitry required. Input protection, IAW the ARINC 429 specification, is provided as well as the voltage level translation from +5 V Bipolar nonreturn to zero Data to conventional +5 V logic levels used internal to the DD-42900 device.

Receive Data Rates can be programmed for channels 0 and 1 independently of channels 2 and 3 via bits 2 and 3 of Arinc Control Register 2. The receiver circuitry will successfully decode an incoming ARINC 429 data stream as long as the data rate is within ±5% of the nominal rate as determined by the Hi Speed/Lo Speed Bit and the associated ARINC Clock input (ARINC CLK 0 or ARINC CLK 1). The two 1 MHz ARINC clock inputs may be tied to the 1 MHz receive clock output or may be connected to another clock source. The ARINC CLK input should nominally be 10 times (for High Speed Mode) or 80 times (for low speed mode) the desired ARINC Data Rate. ARINC CLK 0 is used by channels Rx0 and Rx1 while ARINC CLK 1 is used by channels Rx2 and Rx3.

Filtering and Sorting Rx Data: The receiver circuitry converts the serial data stream to a 32 bit wide parallel data word. The 32 bit word is processed internally by a Data Match Processor (DMP). It compares the incoming data to a table of data initialized by the processor which determines what incoming data is to be saved, where it is going to be saved, and if any interrupts are to be generated. The table of data is stored in a 128 word x 16 bit Data Match Table (DMT) RAM. When a match between the received ARINC 429 data and the criteria stored in a DMT entry is found, the received data, the storage address and modes, and interrupt parameters are passed to the Data Store Processor (DSP). The storage address in the Receive RAM is the address of the first matching DMT entry minus 200 hex.

There are three requirements to matching incoming ARINC-429 data to each DMT entry.

1) System Address Label: Bits 0-7 of the DMT are compared to the System Address Label (SAL) of the incoming ARINC 429 data word. If the DMT SAL entry is zero then the SAL of the incoming data word is ignored (or considered a match).

2) Source/Destination Bits: Bits 8 and 9 of each DMT entry are compared to the Source/Destination bits of the incoming ARINC-429 data word. If these bits match or if Bit 10 of the DMT entry is set to a one then the S/D bit comparison is considered a match. It is also possible through the DMP Control Register 1 to enable "All Call Mode" as defined in ARINC 429 specification. When enabled for a particular receive channel, the S/D bits will be considered a match when the incoming ARINC 429 data contains a 00 in its S/D bit pair.

3) Receive Channel Number: Bits 12 and 13 of each DMT entry are compared to the number of the channel which received the ARINC 429 data.

If and when all of the above conditions are satisfied then a Data Match has occurred and the data will be stored in a RAM location whose address equals the matching DMT entry minus 200 hex.

Bit 11 of each DMT entry, when set, will cause the incoming ARINC 429 data to stored in the corresponding receive channel FIFO (as well as the Rx RAM) when the data match conditions are met.

Bits 14 and 15 of each DMT entry provide the ability to cause one of three general purpose interrupts upon a data match condition. If set to "00" then no interrupt will occur upon a data match condition. (more information on interrupts is described later)

ARINC-429 TRANSMITTER(S)

The DD-42900 supports two ARINC 429 transmitters. Each transmitter channel transmits data independently and are designated Tx0 and Tx1. The transmit output of the DD-42900 is a TTL encoded digital data stream which can be connected directly to DDC's DD-03182 ARINC 429 line driver.

Transmit data rates can be programmed for channels 0 and 1 independently. The transmit data rate is determined by the Hi Speed/Lo Speed Bit for each of the Tx channels in Arinc Control Register 2 and the associated ARINC Clock input (ARINC CLK 0 or ARINC CLK 1). The two 1 MHz ARINC clock inputs may be tied to the 1 MHz clock output or may be connected to another clock source to achieve transmit data rates other than 100 kHz or 12.5 kHz. The transmit clock input should be 10 times (for High Speed Mode) or 80 times (for low speed mode) the desired ARINC transmit data rate.

Transmit FIFOs: Each transmitter channel is provided with an output FIFO which is 32 words deep by 32 bits wide. When writing data to the Tx FIFO the associated Disable Txn bit in Arinc Control Register 1 can be set to a logic zero until the FIFO is loaded with the desired data. Upon setting the Disable Txn low the transmit channel will send the 32 bit message words with appropriate interword gaps on the ARINC 429 output. A status bit indicating that the FIFO is empty is supplied for each transmitter in the Arinc Status Register.

Wraparound testing can be performed from Tx0 to Rx0 and Rx1 and from Tx1 to Rx2 and Rx3. Wraparound testing is enabled by setting the appropriate bits in Arinc Control Register 2. The parity of the transmitted word can be altered to even parity (instead of the normally odd parity) by setting the associated Txn Parity bit in the Arinc Control Register 2 which is useful to verify proper operation of the parity check circuitry each of the receive circuits during wraparound test mode.

PROCESSOR INTERFACE

The processor interface allows for the use of either a 8- or 16-bit data bus. Also Intel or Motorola control signal formats can be used.

INTERRUPT OPERATIONAL MODES

The DD-42900 provides 4 interrupt outputs. Three of these interrupt outputs (IRQ1, IRQ2, and IRQ3) are general purpose programmable interrupts. The fourth interrupt is an Error interrupt output which is specifically used to provide indications of various error conditions and is nonmaskable.

ERROR INTERRUPT OPERATION

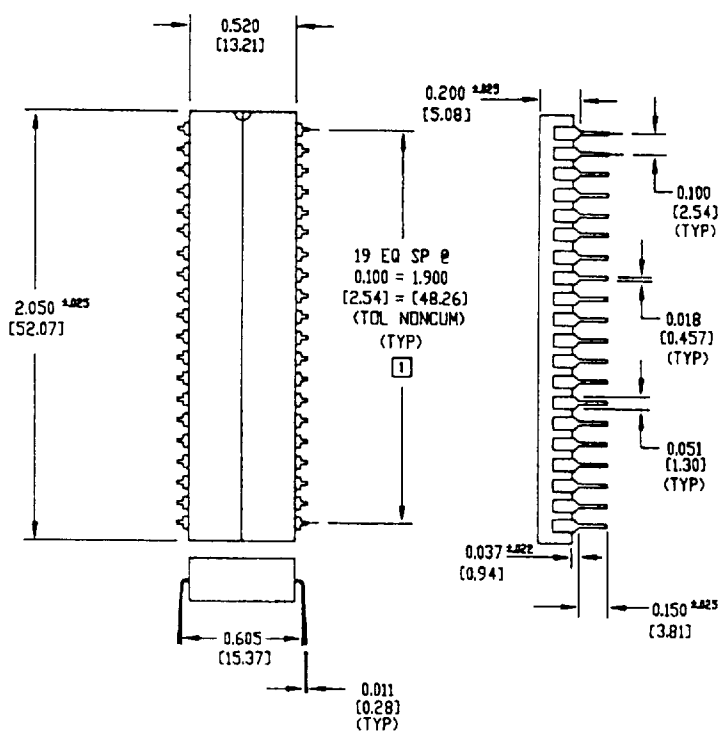
When an error condition occurs the ERROR* output pin goes low to indicate the presence of an error. The error pin will go high again when the Error Status Register is clear. Each of these bits is cleared by either reading the Error Status Register or removing the error condition.

GENERAL PURPOSE INTERRUPTS

The three general purpose interrupt outputs can be used for multilevel interrupts or to trigger other external hardware on various conditions. Each condition can be mapped to any one of the three general purpose interrupts or disabled (by mapping to IRQ0 which does not exist). Each interrupt output can be programmed to be either a LEVEL interrupt or PULSE interrupt via IRQ Control Register 2. When programmed for pulse interrupt mode the associated interupt pin will go low for 1 µS and return high again. When programmed for LEVEL interrupt mode the interrupt will remain until the associated IRQ Status Register is read thus clearing the associated bits in each interrupt register.

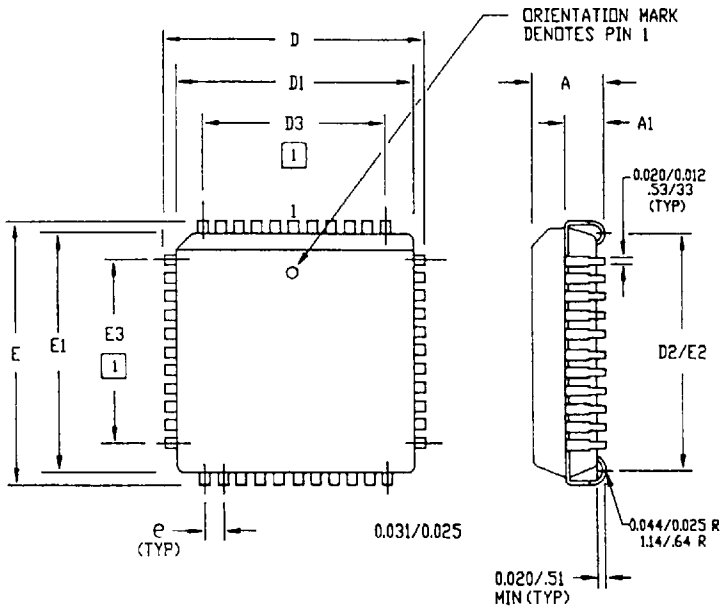
Each of the individual interrupt registers can be masked by setting their corresponding bit in IRQ Control Register 1. It should be noted that the masking function only prevents the associated IRQ pin from becoming active. When the mask bit is cleared an interrupt can occurr in LEVEL IRQ mode if one or more interrupt conditions occurred during the time when the mask was set. If the user needs to ensure the interrupt will not occur upon clearing the mask bit the CPU should be programmed to read the associated interrupt status register immediately prior to clearing the IRQ mask bit.

Zero Wait Mode Operation: When Zero Wait Mode is enabled by grounding the ZERO WAIT pin the host microprocessor may read data from the DD-42900 shared memory resources (DMT and Rx RAM) without using the READY or DTACK signals to insert wait states into the microprocessor cycle. This is accomplished by an additional "dummy read" of the desired address. This dummy read causes the DD-42900 to fetch the data from the source and place it in a latch. The data can then be read from the latch (word by word or byte by byte) by reading the same addresses. Thus for a 32 bit read in 8 bit mode the microprocessor would perform a total of 5 read operations. The first read would be the dummy read, subsequent reads would transfer the data.



1 LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±.010

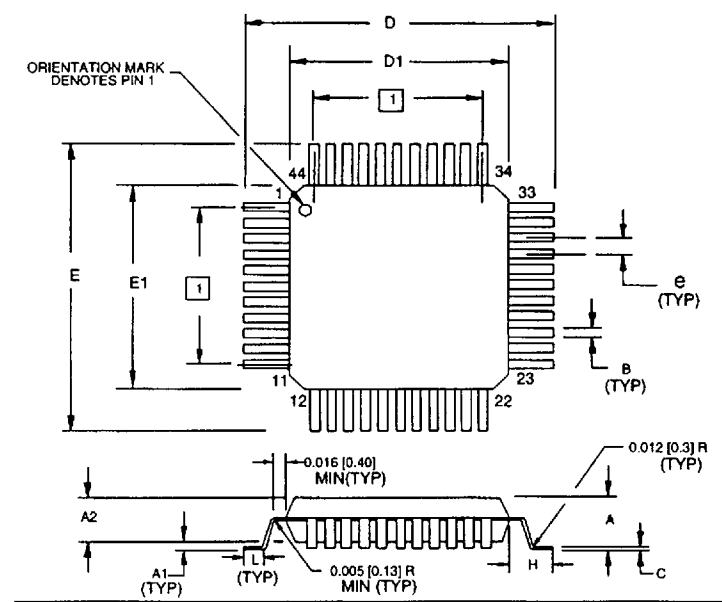
FIGURE 2A. DD-03282 DIP MECHANICAL OUTLINE



		A	A1	D1	D2	D3	E1	E1	E3	e	D	E
MIN	INCHES	0.165	0.090	0.649	0.590	0.500	0.650	.0.590	0.500	0.050	0.685	0.685
MAX		0.180	0.119	0.655	0.630	0.500	0.655	0.630	0.500	0.050	0.694	0.694
MIN	MM	4.20	2.29	16.51	14.99	12.70	16.51	14.99	12.70	1.27	17.40	17.40
MAX		4.57	3.04	16.66	16.00	BSC	16.66	16.00	BSC	BSC	17.65	17.65

[1] LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±.010

FIGURE 2B. DD-03282 PLCC MECHANICAL OUTLINE

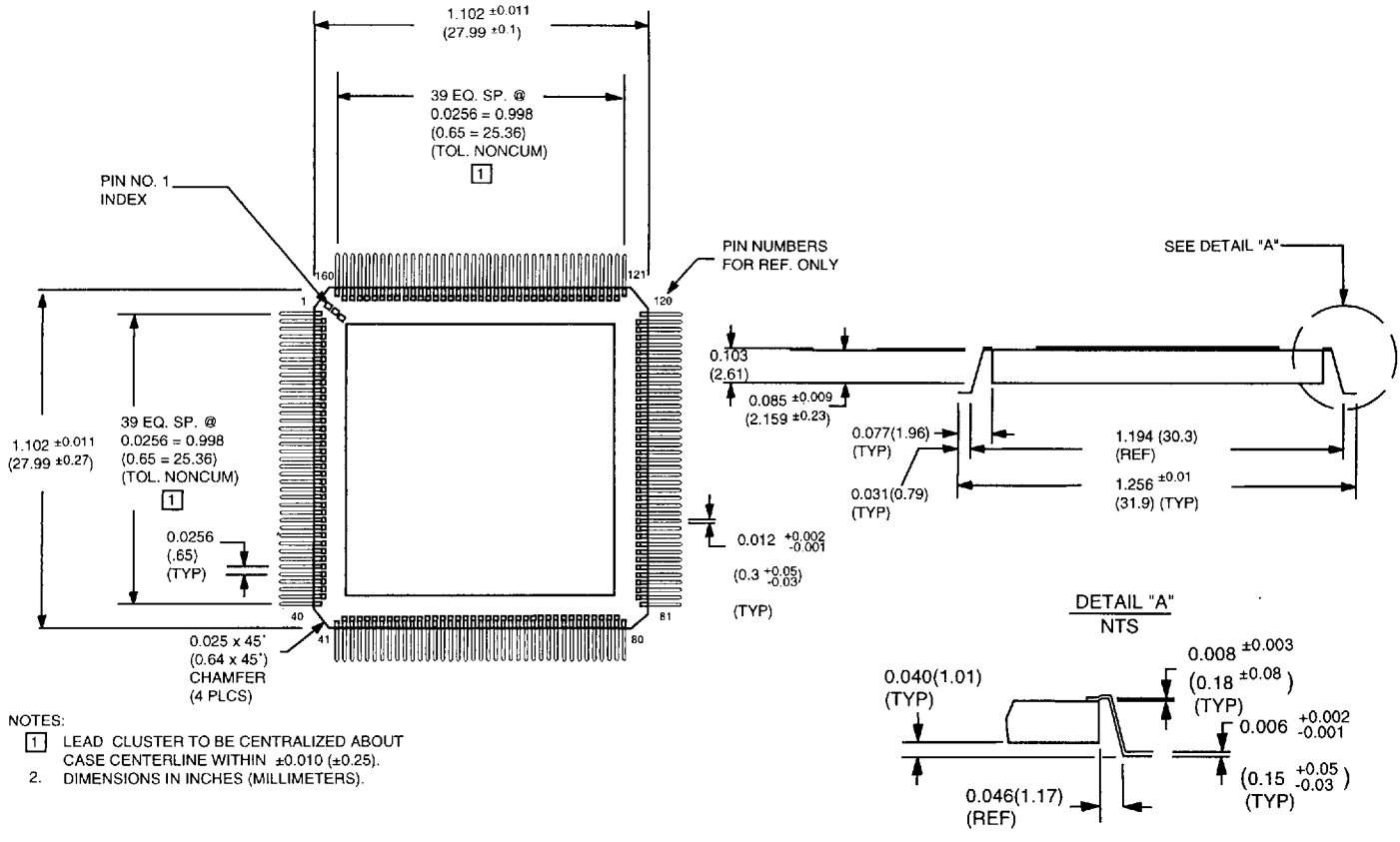


		A	A1	A2	D	D1	E	E1	L	e	B	H	C
MIN	INCHES	-	0.004	0.077	0.537	0.390	0.537	0.390	0.026	0.031	0.012	0.077	0.005
MAX		0.093	0.010	0.083	0.557	0.398	0.557	0.398	0.037	BSC	0.018	REF	0.009
MIN	MM	-	0.10	1.95	13.65	9.90	13.65	9.90	0.65	0.80	0.30	1.95	0.13
MAX		2.35	0.25	2.10	14.15	10.10	14.15	10.10	0.95	BSC	0.45	REF	0.23

[1] LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN [0.00039]

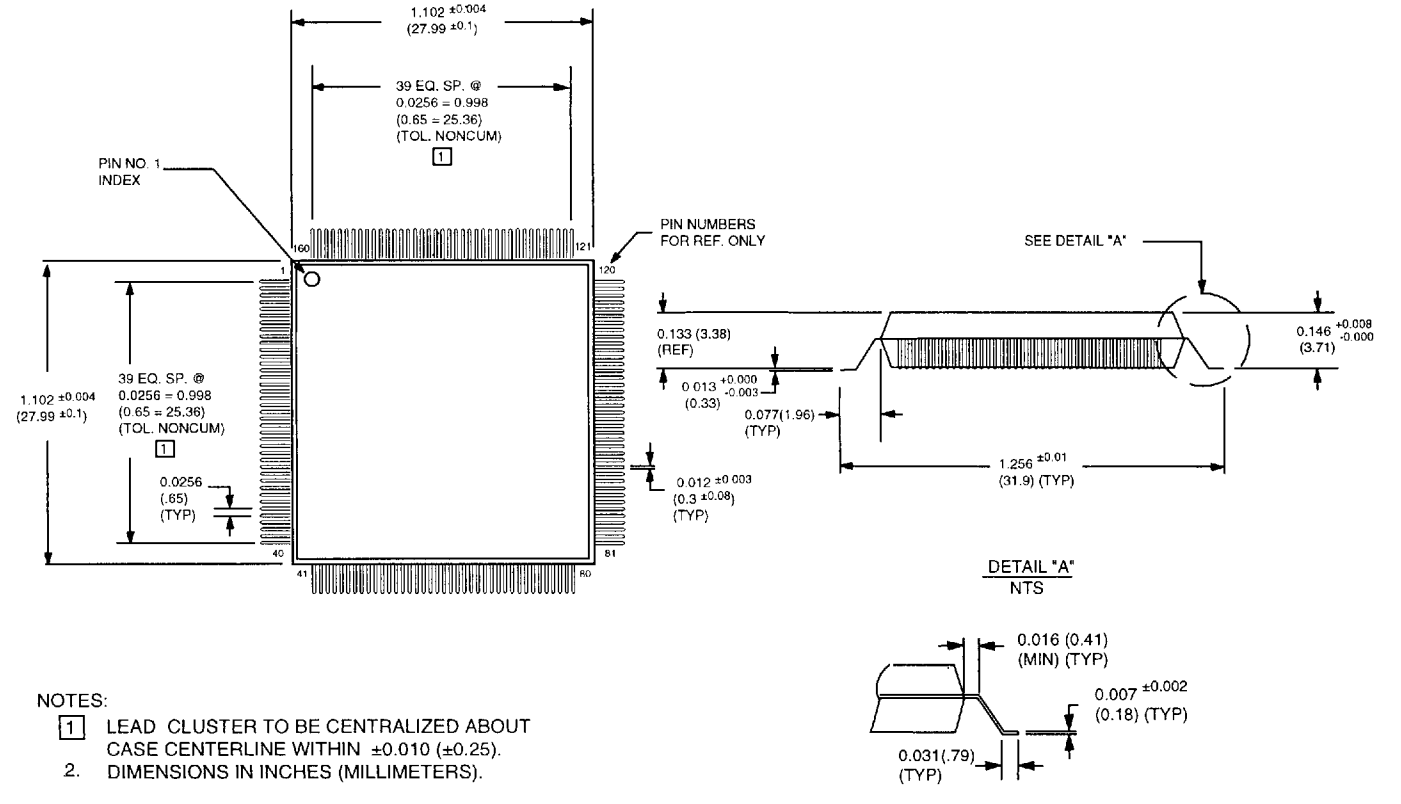
2 DIMENSIONS SHOWN ARE IN INCHES [MILLIMETERS]

FIGURE 2C. DD-03282GP MECHANICAL OUTLINE



NOTES:
1. LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±0.010 (±0.25).
2. DIMENSIONS IN INCHES (MILLIMETERS).

FIGURE 3A. DD-42900 ASIC MECHANICAL OUTLINE (CERAMIC)



NOTES:
1. LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±0.010 (±0.25).
2. DIMENSIONS IN INCHES (MILLIMETERS).

FIGURE 3B. DD-42900 ASIC MECHANICAL OUTLINE (PLASTIC)

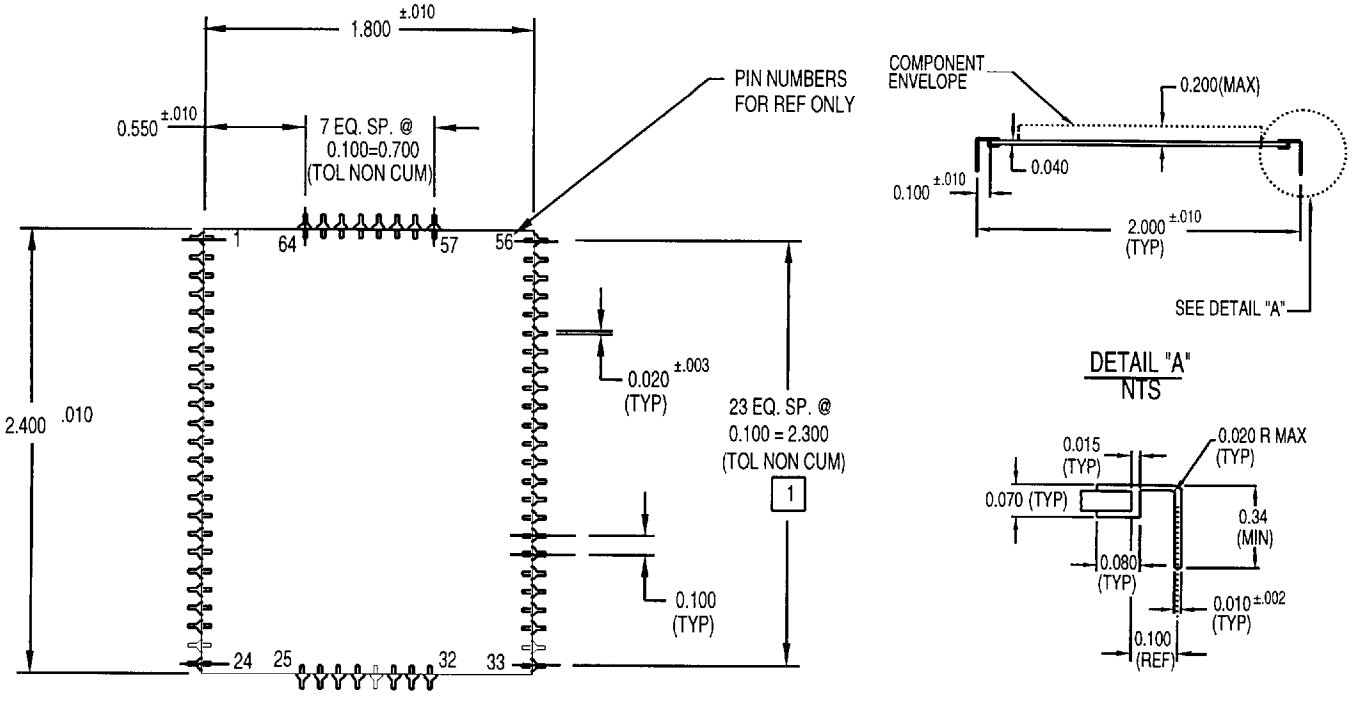
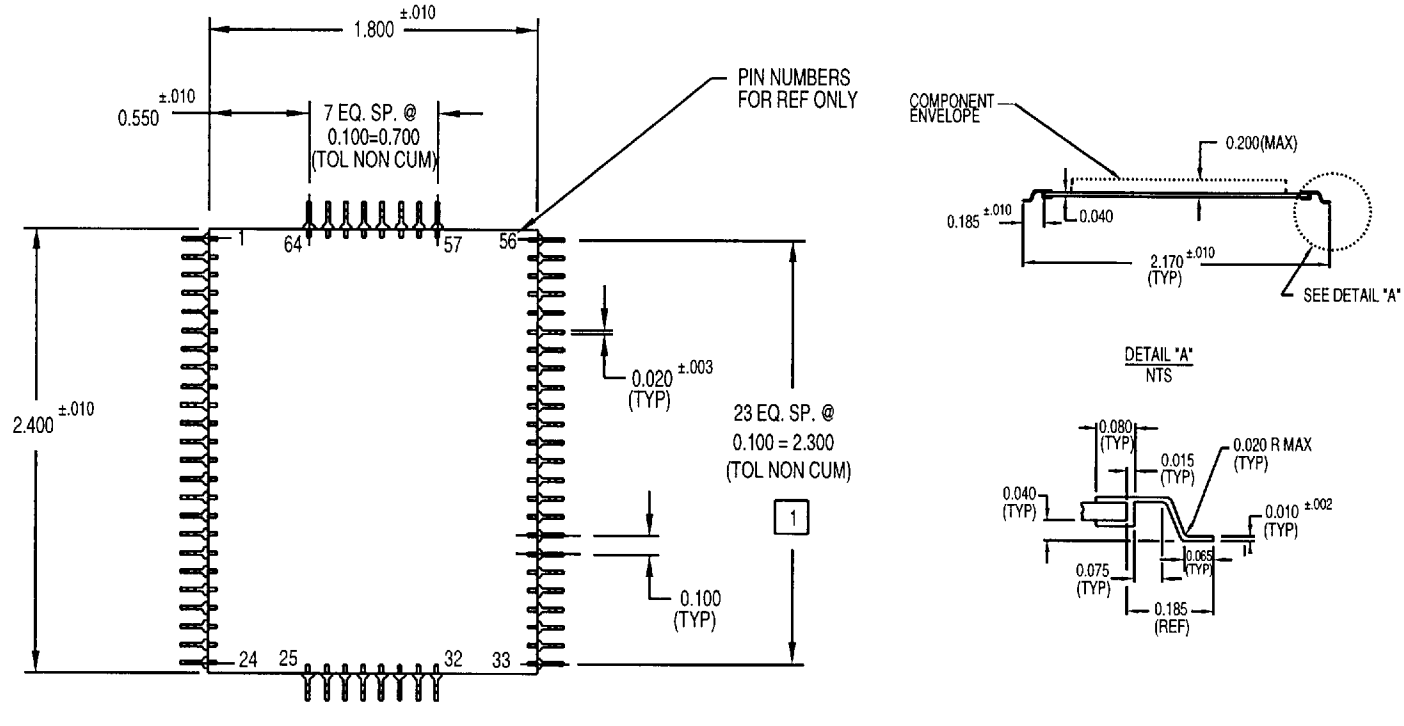


FIGURE 4A. DD-42900 DIP MECHANICAL ASSEMBLY



NOTES:

1 LEAD CLUSTER TO BE CENTRALIZED ABOUT PWB CENTERLINE WITHIN ±.010

FIGURE 4B. DD-42900 FLAT PACK MECHANICAL ASSEMBLY

DD-42900 PINOUTS (DIP AND FLAT PACK)			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	POL SEL A1	33	D0
2	POL SEL A0	34	D1
3	INTEL / MOTO*	35	D2
4	8/16* BIT	36	D3
5	Tx0 A	37	D4
6	Tx0 B	38	D5
7	Tx1 A	39	D6
8	Tx1 B	40	D7
9	A0	41	D8
10	A1	42	D9
11	A2	43	D10
12	A3	44	D11
13	A4	45	D12
14	A5	46	D13
15	A6	47	D14
16	A7	48	D15
17	A8	49	IRQ3*
18	A9	50	IRQ2*
19	A10	51	IRQ1*
20	CS0*	52	1 MHz OUT
21	CS1*	53	ARINC CLK 1
22	CS2	54	ARINC CLK 0
23	GND	55	+5 V
24	GND	56	+5 V
25	ZERO WAIT MODE	57	Rx3 B
26	READY	58	Rx3 A
27	RD* (DS*)	59	Rx2 B
28	WR* (RD/WR*)	60	Rx2 A
29	DTACK*	61	Rx1 B
30	ERROR*	62	Rx1 A
31	MASTER RESET*	63	Rx0 B
32	16 MHz CLOCK	64	Rx0 A

ORDERING INFORMATION

Full Assembly:

DD-42900XY-300

- Burn-in
  - 0 = No Burn-in
  - 2 = Burn-in (Ceramic Only)
- Temperature Range
  - 3 = 0 - 70°C
  - 2 = -40 - +85°C
  - 1 = -55 - +125°C (Ceramic Only)
- ASIC Package Type
  - P = Plastic
  - C = Ceramic
- Lead Type
  - D = Dip
  - F = Flat Pack

Chip Set:

DD-429X0XY-300

- Burn-in
  - 0 = No Burn-in
  - 2 = Burn-in (Ceramic Only)
- Temperature Range
  - 3 = 0 - 70°C
  - 2 = -40 - +85°C
  - 1 = -55 - +125°C (Ceramic Only)
- Transceiver Package Type
  - P = Plastic
  - C = Ceramic
- Lead Type
  - D = Dip (Ceramic Only)
  - P = PLCC (Plastic Only)
  - G = PQFP (Plastic Only)
- Chip Set
  - 42910 = ASIC + one transceiver
  - 42920 = ASIC + two transceivers

Note: "ASIC" is a QFP package.