2.5V Drive Pch+SBD MOSFET

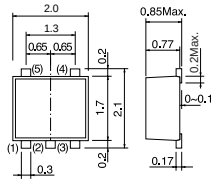
US5U38

●Structure
Silicon P-channel MOSFET
Schottky Barrier DIODE

●Features
1) The US5U38 combines Pch MOSFET with a Schottky barrier diode in a TUMT5 package.
2) Low on-resistance with fast switching.
3) Low voltage drive (2.5V).
4) Built-in schottky barrier diode has low forward voltage.

●Dimensions (Unit : mm)

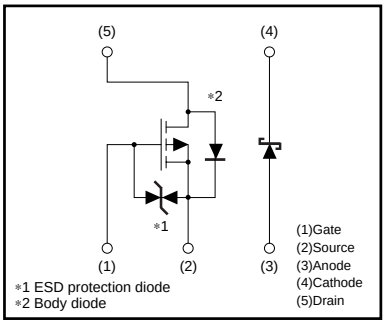
TUMT5



Abbreviated symbol : U38

●Applications
Switching

●Equivalent circuit



*1 ESD protection diode
*2 Body diode

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US5U38		○

●Absolute maximum ratings (Ta=25°C)

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−20	V
Gate-source voltage		V_{GSS}	±12	V
Drain current	Continuous	I_D	±1.0	A
	Pulsed	I_{DP} *1	±4.0	A
Source current (Body diode)	Continuous	I_S	−0.4	A
	Pulsed	I_{SP} *1	−4.0	A
Channel temperature		Tch	150	°C
Power dissipation		P_D *3	0.7	W / ELEMENT
<Di>				
Repetitive peak reverse voltage		V_{RM}	25	V
Reverse voltage		V_R	20	V
Forward current		I_F	0.7	A
Forward current surge peak		I_{FSM} *2	3.0	A
Junction temperature		Tj	150	°C
Power dissipation		P_D *3	0.5	W / ELEMENT
<MOSFET AND Di>				
Power dissipation		P_D *3	1.0	W / TOTAL
Range of storage temperature		Tstg	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1% *2 60Hz・1cyc. *3 Mounted on a ceramic board

●**Electrical characteristics** (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±12V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–20	–	–	V	I_D=–1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}=–20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.7	–	–2.0	V	V_{DS}=–10V, I_D=–1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$ *	–	280	390	mΩ	I_D=–1A, V_{GS}=–4.5V
		–	310	430	mΩ	I_D=–1A, V_{GS}=–4.0V
		–	570	800	mΩ	I_D=–0.5A, V_{GS}=–2.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	0.7	–	–	S	V_{DS}=–10V, I_D=–0.5A
Input capacitance	C_{iss}	–	150	–	pF	V_{DS}=–10V
Output capacitance	C_{oss}	–	20	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	20	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	9	–	ns	I_D=–0.5A V_{DD}≒–15V V_{GS}=–4.5V R_L≒30Ω R_G=10Ω
Rise time	t_r *	–	8	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	25	–	ns	
Fall time	t_f *	–	10	–	ns	
Total gate charge	Q_g *	–	2.1	–	nC	I_D=–1A, V_{DD}≒–15V
Gate-source charge	Q_{gs} *	–	0.5	–	nC	V_{GS}=–4.5V
Gate-drain charge	Q_{gd} *	–	0.5	–	nC	R_L≒15Ω, R_G=10Ω

* Pulsed

<Body diode (source–drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	–	–	–1.2	V	I_S=–0.4A, V_{GS}=0V

<Di>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_F	–	–	0.49	V	I_F=0.7A
Reverse current	I_R	–	–	200	μA	V_R=20V

●**Electrical characteristic curves**

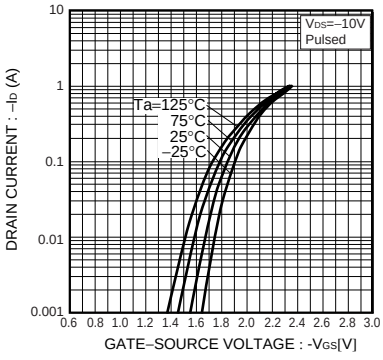


Fig.1 Typical Transfer Characteristics

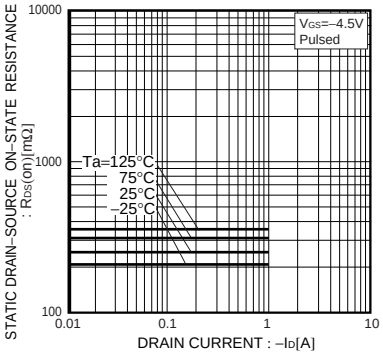


Fig.2 Static Drain–Source On–State Resistance vs.Drain Current (I)

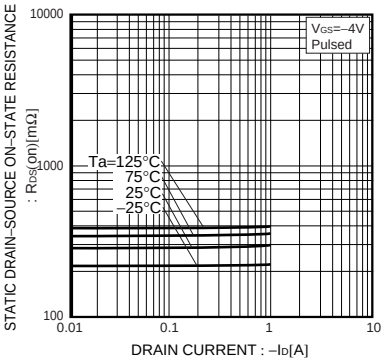


Fig.3 Static Drain–Source On–State Resistance vs.Drain Current (II)

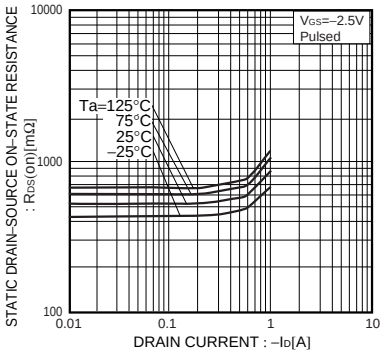


Fig.4 Static Drain–Source On–State Resistance vs.Drain–Current (III)

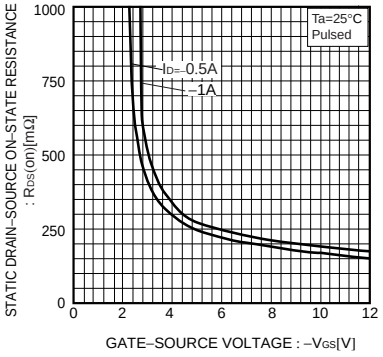


Fig.5 Static Drain–Source On–State Resistance vs.Gate–Source Voltage

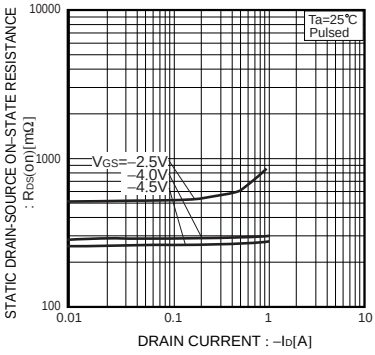


Fig.6 Static Drain–Source On–State Resistance vs.Drain Current

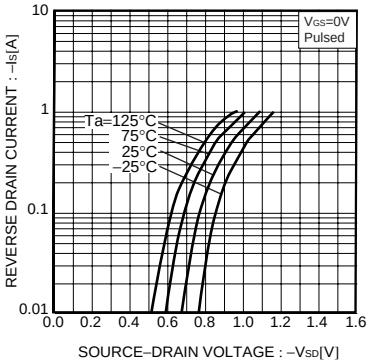


Fig.7 Reverse Drain Current vs. Source-Drain Current

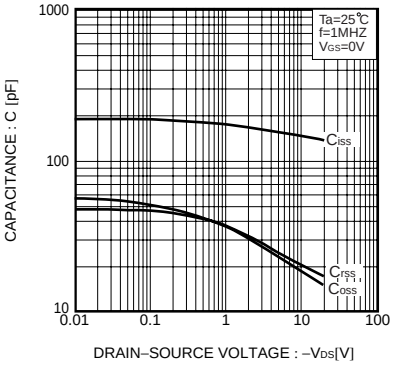


Fig.8 Typical Capactitance vs.Drain–Source Voltage

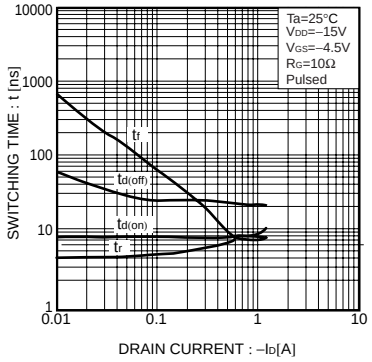


Fig.9 Switching Characteristics

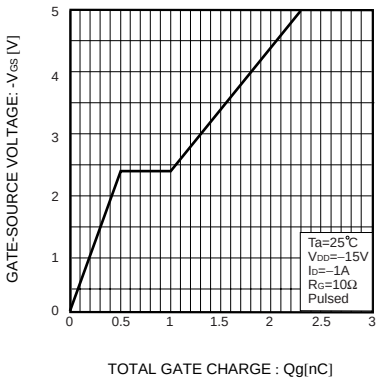


Fig.10 Dynamic Input Characteristics

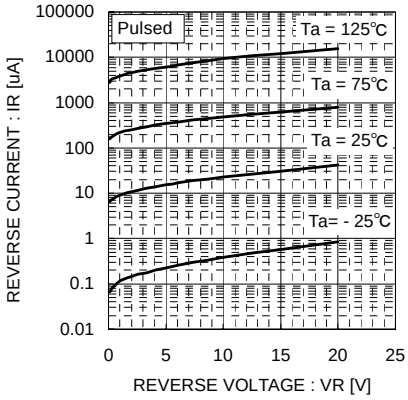


Fig.11 Reverse Current vs. Reverse Voltage

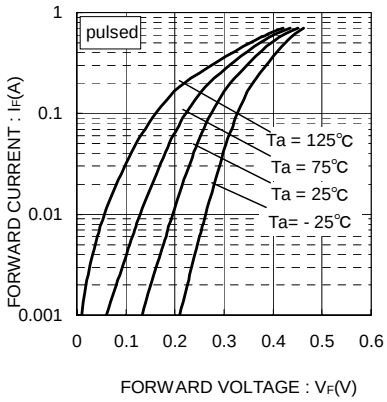


Fig.12 Forward Current vs. Forward Voltage

●Notice

1. SBD has a large reverse leak current compared to other type of diode. Therefore; it would raise a junction temperature, and increase a reverse power loss. Further rise of inside temperature would cause a thermal runaway.
   This built-in SBD has low V_F characteristics and therefore, higher leak current. Please consider enough the surrounding temperature, generating heat of MOSFET and the reverse current.

2. This product might cause chip aging and breakdown under the large electrified environment.
   Please consider to design ESD protection circuit.

●**Measurement circuits**

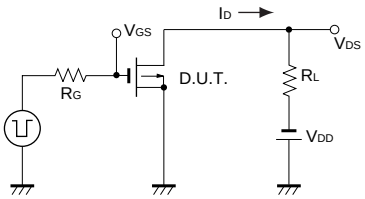


Fig.13 Switching Time Measurement Circuit

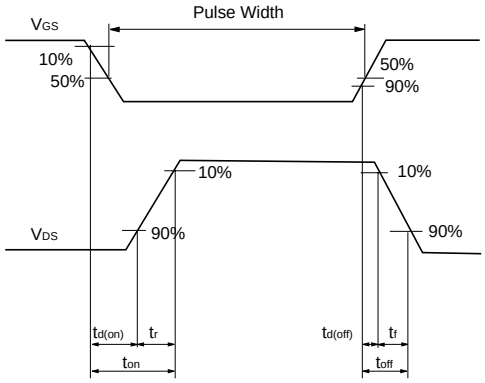


Fig.14 Switching Waveforms

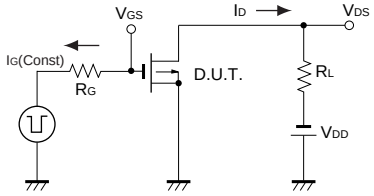


Fig.15 Gate Charge Measurement Circuit

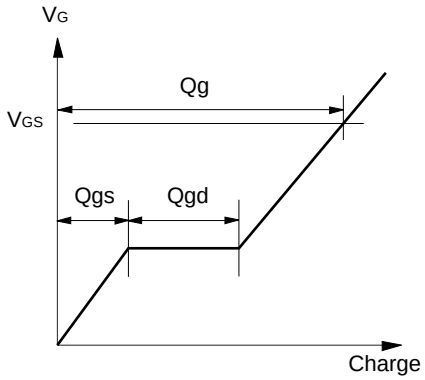


Fig.16 Gate Charge Waveforms

Appendix

Notes

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