CMOS 8-BIT MICROCONTROLLER

TMP90CS38F / TMP90CS38T
TMP90CS39F / TMP90CS39T

1. OUTLINE AND CHARACTERISTICS

TMP90CS38 is a high speed, high performance 8-bit microcontroller developed for application in the control of various devices.

TMP90CS38, CMOS 8-bit microcontroller, integrates an 8-bit CPU, ROM, RAM, A/D converter, multifunction timer/event counter, general-purpose serial interface and pattern generation/stepping motor controller in a single chip, and with which external program memory and data memory can be extended up to 2KB. The TMP90CS39 is the same as the TMP90CS38 but without the ROM.

The TMP90CS38F/S39F uses a 80-pin flat package.

The TMP90CS38T/S39T uses a 84-pin QFJ (PLCC) package.

The following are the features of the TMP90CS38.

(1) Highly efficient instruction set
167 basic instructions
Division and multiplication instructions, 16-bit operation instructions and bit operation instructions

(2) Minimum instruction execution time : 250 ns (at 16 MHz)

(3) Built-in ROM: 60K bytes (The TMP90CS39 does not have a buit-in ROM.)

(4) Built-in RAM: 2K bytes

(5) Memory extension capability
External program memory : 2K bytes
External data memory : 2K bytes

(6) Interrupt functions : 13 internal, 5 external

(7) 8-bit A/D converter (8 channels)

(8) Pattern generation/Stepping motor control ports (2 channels)

(9) General-purpose serial interface mode (2 channels)
- With asynchronous mode and I/O interface mode (1 channel)
- I/O interface mode (1 channel)

(10) Timer function
  (1) 16-bit timer/event counter (1 channel)
  ------ Built-in 2 capture register and 2 comparator
  (2) 8-bit timer (4 channels)
  ------ Built-in 1 comparator in each channels
  (3) Watchdog timer function ($\overline{\text{WDTOUT}}$ pin having)

(11) I/O ports : MAX66 pins

(12) HDMA function (2 channels) ------ 1 byte transmission : 1.75 μs (at 16.0 MHz)

(13) Software standby function ------ RUN、 STOP、 IDLE modes
Hardware standby function------ STOP mode

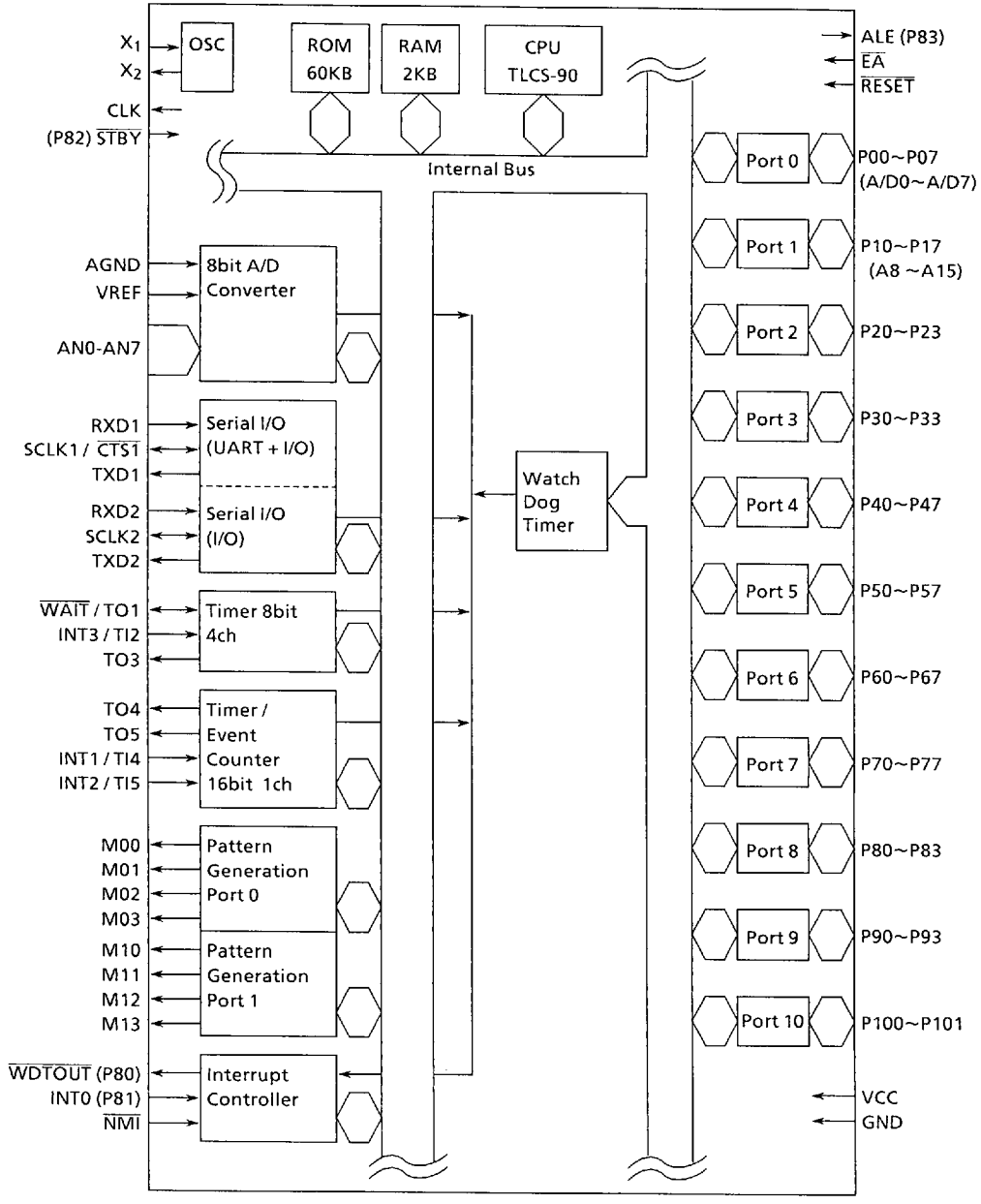

Figure 1 TMP90CS38 block diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for TMP90CS38/S39, their name and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.(1) shows pin assignment of TMP90CS38F/S39F.

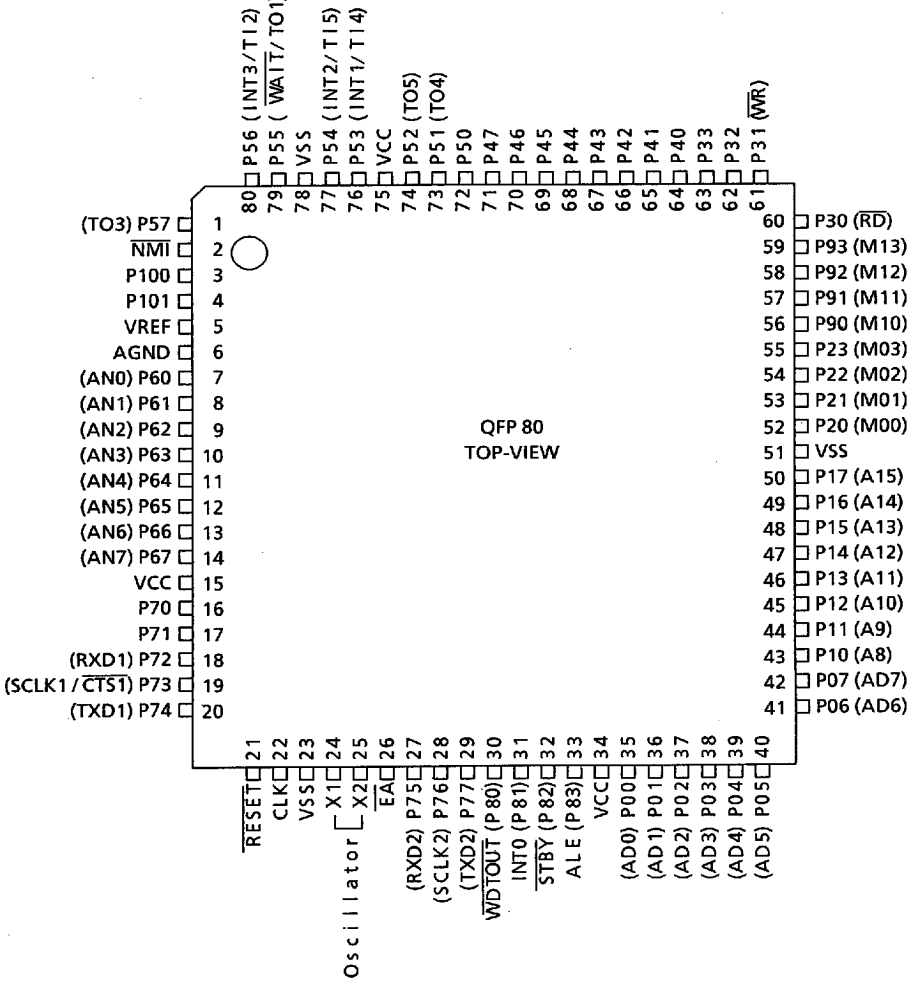

Figure 2.1 (1) Pin assignments (flat package)

Figure 2.1 (2) shows pin assignment of TMP90CS38T/S39T.

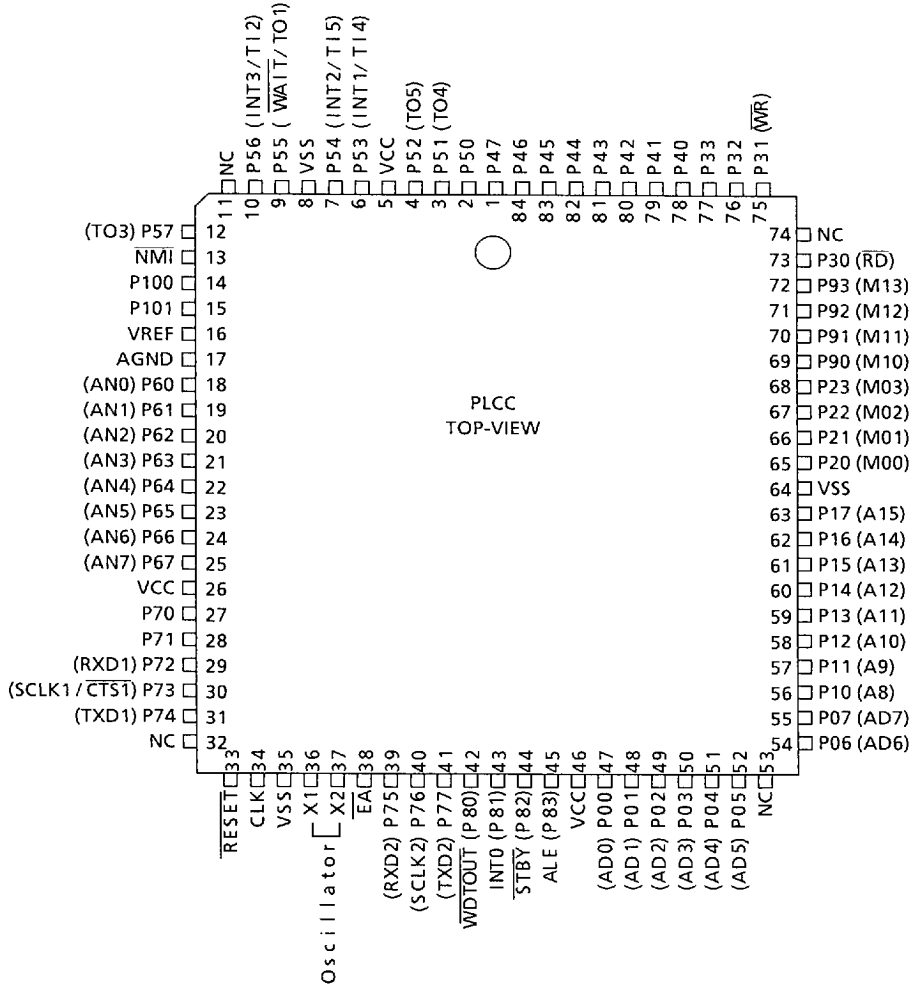

Figure 2.1 (2) Pin assignments (QFJ (PLCC) package)

2.2 Pin Names and Functions

The names of input / output pins and their functions are described below. Table 2.2 Pin Names and Functions.

Table 2.2 (1/3)

Pin name	No. of pins	I/O or tristate	Function
P00~P07	8	I/O	Port 0 : An 8-bit I/O port. Each bit can be set for input or output.
/AD0~AD7		Tristate	Address/data bas : Operates as an 8-bit bi-directional address bus or data bus when using external memory.
P10~P17	8	I/O	Port1: An 8-bit I/O port. Each bit can be set for input or output.
/A8~A15		Output	Address bus: Operates as the 8 upper bits of the address bus when using external memory.
P20~P23	4	I/O	Port2: An 8-bit I/O port. Each bit can be set for input or output.
/M00~M03		Output	Stepping motor control port 0 or pattern generation port 0.
P30	1	Output	Port30: A 1-bit output port.
/$\overline{RD}$			Read: Strobe signal output for reading external memory.
P31	1	Output	Port31: A 1-bit output port.
/$\overline{WR}$			Write: Strobe signal output for writing into external memory.
P32, P33	2	I/O	Port32, Port33: A 2-bit I/O port. Each bit can be set for input or output.
P40~P47	8	I/O	Port40~47: A 8-bit I/O port. Each bit can be set for input or output.
P50	1	I/O	Port50: A 1-bit I/O port.
P51	1	I/O	Port51: A 1-bit I/O port.
/TO4		Output	Timer Output4: Timer 4 output pin.
P52	1	I/O	Port52: A 1-bit I/O port.
/TO5		Output	Timer Output5: Timer 5 output pin.
P53	1	I/O	Port53: A 1-bit I/O port.
/INT1		Input	Interrupt request pin1: A rising/falling edge programmable interrupt request pin.
/TI4		Input	Timer input4: Timer 4 counter input pin.

(2/3)

Pin name	No. of pins	I/O or tristate	Function
P54	1	I/O	Port54: A 1-bit I/O port.
/INT2		Input	Interrupt request pin2: A rising edge interrupt request input pin.
/TI5		Input	Timer input5: Timer 5 counter input pin.
P55	1	I/O	Port55: A 1-bit I/O port.
/TO1		Output	Timer output1: Timer 0 or timer 1 output.
/$\overline{WAIT}$		Input	/ Wait: Input pin for connecting a memory or peripheral LSI with delayed access time.
P56	1	I/O	Port56: A 1-bit I/O port.
/TI2		Input	Timer input2: Timer 2 or Timer 3 counter input pin.
/INT3		Input	Interrupt request pin3: A rirising edge interrupt request input pin.
P57	1	I/O	Port57: A 1-bit I/O port.
/TO3		Output	Timer Output3: Timer 2 or Timer 3 output.
$\overline{NMI}$	1	Input	Non-maskable Interrupt request pin: A falling edge interrupt request pin (Sctimitt input).
VREF	1	Input	Reference Voltage to A/D converter.
AGND	1	Input	GND pin for A/D converter (0V).
P60~P67	8	Input	Port60~67: An 8-bit input ports.
/AN0~AN7			Analog input: 8 analog inputs to A/D converter.
VCC	3	Input	Power supply pin (+ 5V).
VSS (GND)	3	Input	GND pin (0V).
P70	1	I/O	Port70: A 1-bit I/O port.
P71	1	I/O	Port71: A 1-bit I/O port.
P72	1	I/O	Port72: A 1-bit I/O port.
/RXD1		Input	Serial channel 1 receive data input pin.
P73	1	I/O	Port73: A 1-bit I/O port.
/SCLK1		I/O	Serial clock 1: External clock for SCLK1 do input or send clock for internal boudrate generator do output when I/O interface mode is condition.
/CTS1		Input	$\overline{CTS1}$ input pin: Serial data send possible signal (Clear To Send).

(3/3)

Pin name	No. of pins	I/O or tristate	Function
P74	1	I/O	Port74: A 1-bit I/O port (with pull-up resister).
/TXD1		Output	Serial channel 1 send data output pin.
P75	1	I/O	Port75: A 1-bit I/O port.
/RXD2		Input	Serial channel 2 receive data input pin.
P76	1	I/O	Port76: A 1-bit I/O port.
/SCLK2		I/O	Serial clock I/O: External clock for SCLK2 do input or send clock for internal boudrate generator do output when I/O interface mode is condition.
P77	1	I/O	Port77: A 1-bit I/O port (with pull-up resister).
/TXD2		Output	Serial channel 2 send data output pin.
$\overline{\text{RESET}}$	1	Input	Reset: Reset input pin to initialize the TMP90CS38.
CLK	1	Output	Clock output: Output 1/4 frequency of the clock oscillation. Pulled up during reset.
X1, X2	2	I/O	The crystal oscillator connectopn pin.
$\overline{\text{EA}}$	1	Input	External access: Connects with Vcc pin in the TMP90CS38 using internal ROM, and with GND pin in the TMP90CS39 with no internal ROM.
P80	1	Output	Port80: A 1-bit output port.
/$\overline{\text{WDTOUT}}$		Output	Wachdog timer out: Outputs $\overline{\text{WDTOUT}}$ after reset.
P81	1	Input	Port81: A 1-bit input port.
/INT0		Input	Interrupt request pin0: A level/rising edge programmable interrupt request pin.
P82	1	Input	Port82: A 1-bit input port.
/$\overline{\text{STBY}}$		Input	Hardware standby input pin (schmitt input).
P83	1	Output	Port83: A 1-bit output port.
/ALE		Output	Address latch enable : The falling edge of this signal is used for latching addresses on AD0-AD7 when accessing external memory.
P90~P93	4	I/O	Port9: 4-bit I/O port. Each bit can be used for input or output.
/M10~M13		Output	Stepping motor control port 1 or pattern generation port 1.
P100~P101	2	I/O	Port10: 2-bit I/O port. Each bit can be used for input or output.

3. OPERATION

The following explains the TMP90CS38/S39 functions and basic operations. The CPU functions and internal I/O functions of the TMP90CM38/M39 are the same as the TMP90CM38/M39.

Refer to the "TMP90CM38/M39" section concering functions which are not explained the following.

3.1 CPU

The TMP90CS38/S39 has a internal high-performance 8-bit CPU.
Refer to the "TLCS-90 CPU" section concering CPU operation.

3.2 Memory Map

The TMP90CS38 can provide a maximum 64Kbyte program and data memory.
The program and data memories may be allocated to the addresses 0000H to FFFFH.

(1) Built-in ROM

TMP90CS38 has an internal 60Kbyte ROM. This ROM is located at addresses 0000H to EFFFH. Program execution starts from address 0000H after a reset operation.

Addresses 0010H to 00C0H in the internal ROM area are used as the interrupt processing entry area.

The TMP90CS39 does not have a built-in ROM; therefore, the address space 0000H to EFFFH is used as external memory spase.

(2) Built-in RAM

TMP90CS38 contains a 2Kbyte built-in RAM which is allocated to the addresses F7A0H to FF9FH. The CPU can also access some portions of the RAM (160 byte area FF00H to FF9FH) using short instruction codes in the direct addressing mode.

(3) Built-in I/O

TMP90CS38 uses 96 bytes of the address space as a built-in I/O area. The area is allocated to the addresses FFA0H to FFFFH. The CPU can access the built-in I/O using short instruction codes in the direct addressing mode.

Figure 3.1 shows the memory map and the access ranges of the CPU for each addressing mode.

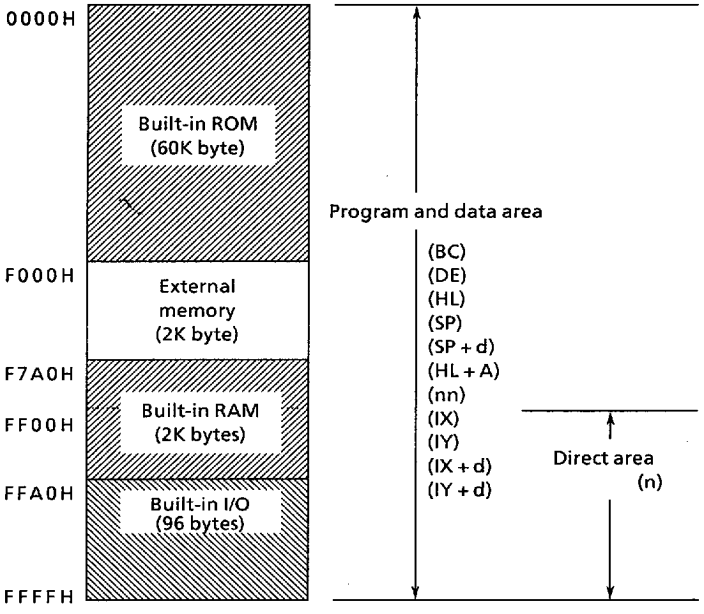

Figure 3.1 Memory Map

4. ELECTRICAL CHARACTERISTICS

TMP90CS38F/TMP90CS38T
TMP90CS39F/TMP90CS39T

4.1 Maximum Ratings

Symbol	Item	Rating	Unit
V_{CC}	Power supply voltage	− 0.5 to + 6.5	V
V_{IN}	Input voltage	− 0.5 to Vcc + 0.5	V
ΣI_{OL}	Output current (Total)	100	mA
ΣI_{OH}	Output current (Total)	− 70	mA
P_D	Power dissipation (Ta = 85 °C)	F 500 T 600	mW
T_{SOLDER}	Soldering temperature (10 s)	260	°C
T_{STG}	Storage temperature	− 65 to 150	°C
T_{OPR}	Operating temperature	− 20 to 70	°C

4.2 DC Characteristics

Vcc = 5V ± 10 % TA = − 20 to 70 °C (1 to 16 MHz)
Typical values are for TA = 25 °C and V_{CC} = 5V.

Symbol	Item	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage (P0)	− 0.3	0.8	V	
V_{IL1}	P1, P2, P3, P4, P5, P6, P7, P9, P10	− 0.3	0.3 Vcc	V	
V_{IL2}	$\overline{RESET}$, P81 (INT0), P82 ($\overline{STBY}$), $\overline{NMI}$	− 0.3	0.25 Vcc	V	
V_{IL3}	$\overline{EA}$	− 0.3	0.3	V	
V_{IL4}	X1	− 0.3	0.2 Vcc	V	
V_{IH}	Input High Voltage (P0)	2.2	Vcc + 0.3	V	
V_{IH1}	P1, P2, P3, P4, P5, P6, P7, P9, P10	0.7 Vcc	Vcc + 0.3	V	
V_{IH2}	$\overline{RESET}$, P81 (INT0), P82 ($\overline{STBY}$), $\overline{NMI}$	0.75 Vcc	Vcc + 0.3	V	
V_{IH3}	$\overline{EA}$	Vcc − 0.3	Vcc + 0.3	V	
V_{IH4}	X1	0.8 Vcc	Vcc + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 0.75 Vcc 0.9 Vcc		V V V	I_{OH} = − 400 μA I_{OH} = − 100 μA I_{OH} = − 20 μA
I_{DAR}	Darlington Drive Current (8 I/O Pins max)	− 1.0	− 3.5	mA	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ
I_{LI}	Input Leakage Current	0.02 (Typ)	± 5	μA	0.0 ≦ Vin ≦ Vcc
I_{LO}	Output Leakage Current	0.05 (Typ)	± 10	μA	0.2 ≦ Vin ≦ Vcc − 0.2
I_{CC}	Operating Current (RUN) Idle1	35 (Typ) 1.5 (Typ)	50 5	mA mA	tosc = 16 MHz
	STOP (TA = − 20 to 70 °C) STOP (TA = 0 to 50 °C)	0.2 (Typ)	40 10	μA μA	0.2 ≦ Vin ≦ Vcc − 0.2
V_{STOP}	Power Down Voltage (at STOP) (RAM back Up)	2.0	6.0	V	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc
R_{RST}	$\overline{RESET}$ Pull Up Register	50	150	kΩ	
C_{IO}	Pin Capacitance		10	pF	testfreq = 1 MHz
V_{TH}	Schmitt width ($\overline{RESET}$, P81, P82)	0.4	1.0 (Typ)	V	

4.3 AC Characteristics

Vcc = 5V ± 10 % TA = – 20 to 70 °C (1 to 16 MHz)

Symbol	Parameter	Variable		12.5 MHz Clock		16 MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{OSC}	Oscillation cycle (= X)	62.5	1000	80		62.5		ns
t_{CYC}	CLK Period	4X	4X	320		250		ns
t_{WH}	CLK High width	2X – 40		120		85		ns
t_{WL}	CLK Low width	2X – 40		120		85		ns
t_{AL}	A0 to 7 effective address → ALE fall	0.5X – 15		25		16		ns
t_{LA}	ALE fall → A0 to 7 hold	0.5X – 20		15		11		ns
t_{LL}	ALE Pulse width	X – 40		40		23		ns
t_{LC}	ALE fall → $\overline{RD}/\overline{WR}$ fall	0.5X – 30		10		1		ns
t_{CL}	$\overline{RD}/\overline{WR}$ rise → ALE rise	0.5X – 25		15		6		ns
t_{ACL}	A0 to 7 effective address → $\overline{RD}/\overline{WR}$ fall	X – 25		55		38		ns
t_{ACH}	Upper effective address → $\overline{RD}/\overline{WR}$ fall	1.5X – 50		70		44		ns
t_{CA}	$\overline{RD}/\overline{WR}$ fall → Upper address hold	0.5X – 25		15		6		ns
t_{ADL}	A0 to 7 effective address → Effective data input		3.0X – 55		185		132	ns
t_{ADH}	Upper effective address → Effective data input		3.5X – 70		210		148	ns
t_{RD}	$\overline{RD}$ fall → Effective data input		2.0X – 65		95		60	ns
t_{RR}	$\overline{RD}$ Pulse width	2.0X – 40		120		85		ns
t_{HR}	$\overline{RD}$ rise → Data hold	0		0		0		ns
t_{RAE}	$\overline{RD}$ rise → Address enable	X – 15		65		48		ns
t_{WW}	$\overline{WR}$ pulse width	2.0X – 40		120		85		ns
t_{DW}	Effective data → $\overline{WR}$ rise	2.0X – 50		110		75		ns
t_{WD}	$\overline{WR}$ rise → Effective data hold	0.5X – 15		25		16		ns
t_{ACKH}	Upper address → CLK fall	2.5X – 50		150		106		ns
t_{ACKL}	Lower address → CLK fall	2.0X – 50		110		75		ns
t_{CKHA}	CLK fall → Upper address hold	1.5X – 80		40		13		ns
t_{CCK}	$\overline{RD}/\overline{WR}$ fall → CLK fall	X – 25		55		37		ns
t_{CKHC}	CLK fall → $\overline{RD}/\overline{WR}$ rise	X – 60		20		2		ns
t_{DCK}	Valid data → CLK fall	X – 50		30		12		ns
t_{CWA}	$\overline{RD}/\overline{WR}$ fall → Valid $\overline{WAIT}$		X – 40		40		22	ns

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Vcc = 5V ± 10 % TA = – 20 to 70 ℃ (1 to 16 MHz)

Symbol	Parameter	Variable		12.5 MHz Clock		16 MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
t_{AWAL}	Lower address → Valid $\overline{WAIT}$		2.0X – 70		90		55	ns
t_{WAH}	CLK fall → Valid $\overline{WAIT}$ hold	0		0		0		ns
t_{AWAH}	Upper address → Valid $\overline{WAIT}$		2.5X – 70		130		86	ns
t_{CPW}	CLK fall → Port Data Output		X + 200		280		262	ns
t_{PRC}	Port Data Input → CLK fall	200		200		200		ns
t_{CPR}	CLK fall → Port Data hold	100		100		100		ns

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AC Measuring Conditions

- Output level : High 2.2V / Low 0.8V, C_L = 50 pF
  (However, CL = 100pF for AD0 to 7, A8 to 15, ALE, $\overline{RD}$, $\overline{WR}$)
- Input level : High 2.4V/Low 0.45V (AD0 to AD7)
  High 0.8 Vcc/Low 0.2 Vcc (except for AD0 to AD7)

4.4 A/D Conversion Characteristics

Vcc = 5V ± 10 % TA = −20 to 70 °C
(f = 1 to 16 MHz)

Symbol	Item	Min	Typ	Max	Unit
VREF	Analog veference voltage	4.0		Vcc	V
A_{GND}	Analog veference voltage	V_{SS}		Vss	
V_{AIN}	Analog input voltage range	V_{SS}		Vcc	
I_{REF}	Analog reference voltage power supply current		0.5	1.0	mA
Error (Quantize error of ± 0.5LSB not included)	Total error (TA = 25 °C, Vcc = VREF = 5.0V)		1.0		LSB
	Total error			2.5	

4.5 Timer/Counter Input Clock (TI2, TI4)

Vcc = 5V ± 10 % TA = −20 to 70 °C
(f = 1 to 16 MHz)

Symbol	Item	Variable		12.5 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock cycle	8X + 100		740		600		ns
t_{VCKL}	Low level clock pulse width	4X + 40		360		290		ns
t_{VCKH}	High level clock pulse width	4X + 40		360		290		ns

4.6 Interrupt Operation

Vcc = 5V ± 10 % TA = −20 to 70 °C
(f = 1 to 16 MHz)

Symbol	Item	Variable		12.5 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{NMI}$, INT0 low level pulse width (⎍)	4X		320		250		ns
t_{INTAH}	$\overline{NMI}$, INT0 high level pulse width (⎍)	4X		320		250		ns
t_{INTBL}	INT1, INT2, INT3 low level pulse width (⎍)	8X + 100		740		600		ns
t_{INTBH}	INT1, INT2, INT3 high level pulse width (⎍)	8X + 100		740		600		ns

4.7 Serial Channel SIO1 Timing – I/O interface Mode

(1) SCLK1 Input Mode

Vcc = 5V ± 10 % TA = – 20 to 70 ℃
f = 1 to 16 MHz

Symbol	Item	Variable		12.5 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK1 cycle	16X		1.28		1		μs
t_{OSS}	Output Data→SCLK1 rise	$t_{SCY}/2 - 5X - 50$		190		137		ns
t_{OHS}	SCLK1 rise→Output Data hold	5X – 100		300		212		ns
t_{HSR}	SCLK1 rise→Input Data hold	0		0		0		ns
t_{SRD}	SCLK1 rise→Effective Data input		$t_{SCY} - 5X - 100$		780		587	ns

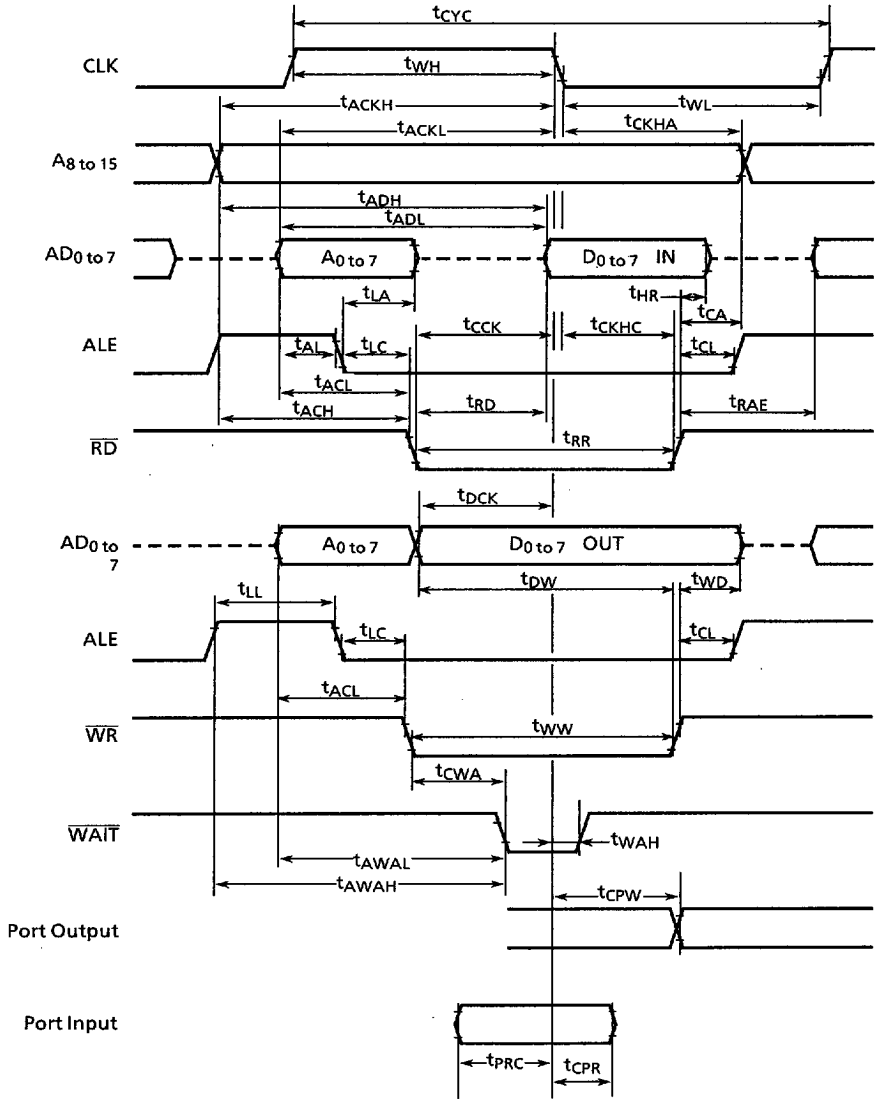
(2) SCLK1 Output Mode

Symbol	Item	Variable		12.5 MHz		16 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK1 cycle (programmable)	16X	8192X	1.28	655.4	1	512	μs
t_{OSS}	Output Data→SCLK1 rise	$t_{SCY} - 2X - 150$		970		725		ns
t_{OHS}	SCLK1 rise→Output Data hold	2X – 80		80		45		ns
t_{HSR}	SCLK1 rise→Input Data hold	0		0		0		ns
t_{SRD}	SCLK1 rise→Effective Data input		$t_{SCY} - 2X - 150$		970		725	ns

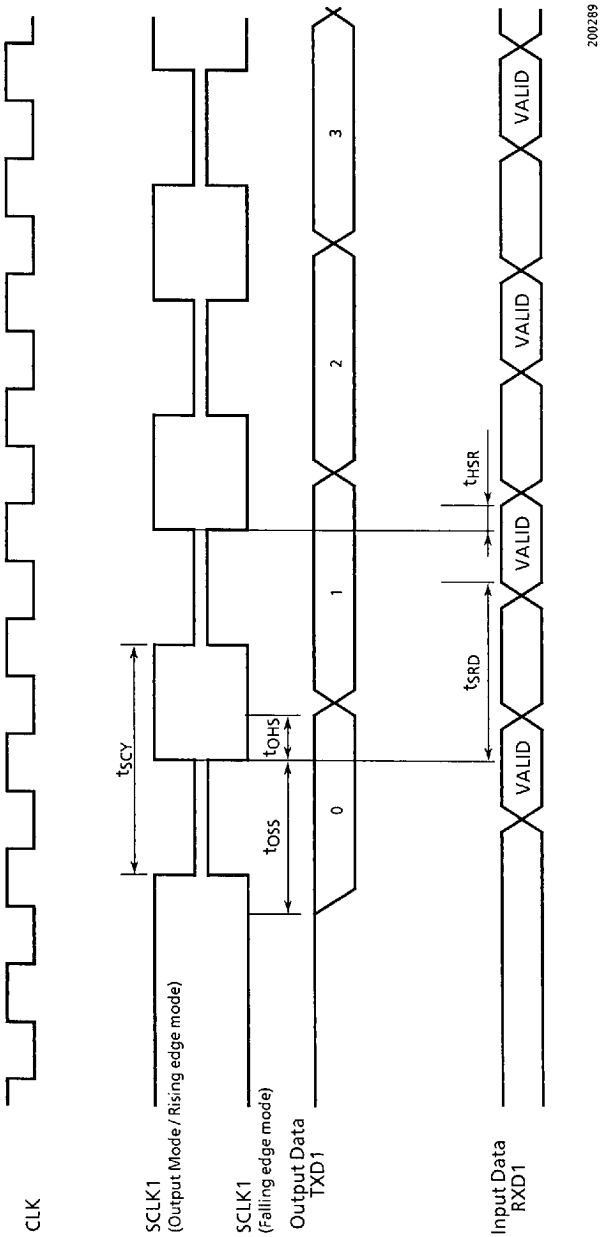
4.8 Serial Channel SIO2 Timing

Symbol	Item	Condition	10MHz Clock		Variable Clock		Unit
			Min	Max	Min	Max	
t_{SCR}	Serial Port Clock Cycle Time	Internal	500	16000	8X	256X	ns
		External	1000		16X		
t_{SCL}	SCLK2 Low Width	Internal	200	300	4X – 50	4X + 50	ns
		External	480	520	8X – 20	8X + 20	
t_{SCH}	SCLK2 High Width	Internal	200	300	4X – 50	4X + 50	ns
		External	480	520	8X – 20	8X + 20	
t_{SKDO}	SCLK2 → TXD2 (Output Data) Delay time	Internal	112.5		X + 50		ns
		External	475		6X + 100		
t_{SRD}	SCLK2 Rising Edge to Input DATA Valid	Internal	377.5		7X – 60		ns
		External	1150		20X – 100		
t_{HSR}	Input Data Hold After SCLK2 Rising Edge	Internal	162.5		X + 100		ns
		External	475		6X + 100		

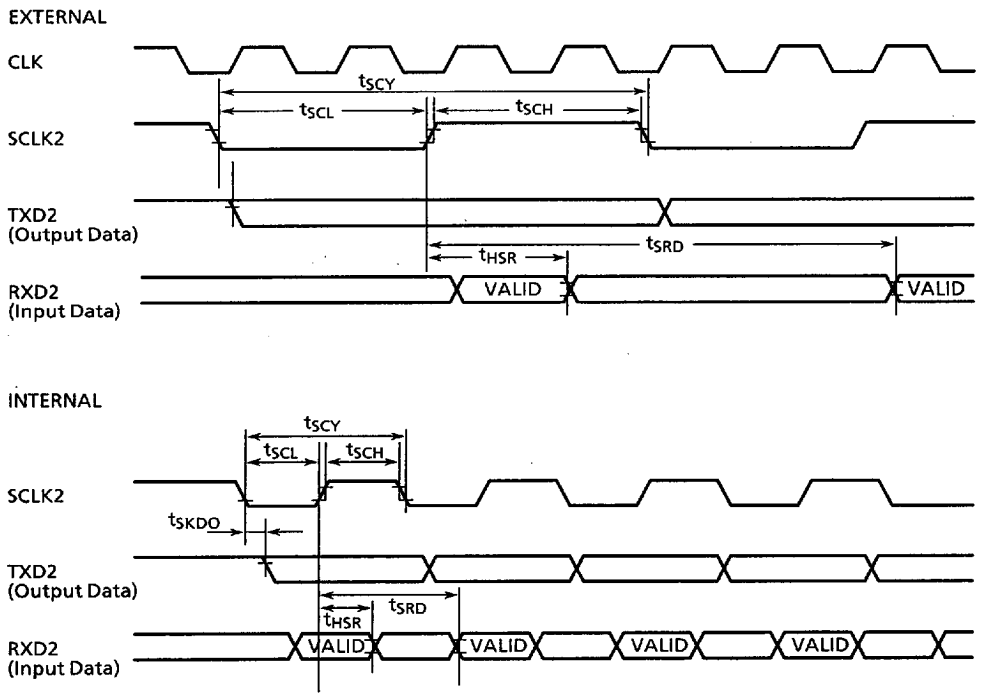
4.9 Timing Chart



4.10 Serial Channel SIO1 I/O Interface Mode Timing Chart



4.11 Serial Channel SIO2 Timing Chart



5. SPECIAL FUNCTION REGISTER LIST

(SFR ; Special Function Register)

The special function registers (SFR) are the input/output ports, peripheral control registers. These SFR are assigned to 96-byte address areas from 0FFA0H to 0FFFFH.

(1) Input/Output ports

(2) Input/Output port Control

(3) Timer/Event counter Control

(4) A/D converter Control

(5) Interrupt Control

(6) HDMA Control

(7) WDT Control

(8) Serial Channel Control

Table configuration

Symbol	Name	Address	7	6	...	1	0	
								→ bit Symbol
								→ Read / Write
								→ initial value after reset
								→ Remarks

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TMP90CS38 SPECIAL FUNCTION REGISTER LIST

Address	Symbol	Address	Symbol	Address	Symbol
FFA0	P0	FFB0	P5FR	FFC0	(Reserved)
FFA1	P0CR	FFB1	P7FR	FFC1	(Reserved)
FFA2	P1	FFB2	P29FR	FFC2	(Reserved)
FFA3	P1CR	FFB3	P9	FFC3	(Reserved)
FFA4	P2	FFB4	P10	FFC4	(Reserved)
FFA5	P29CR	FFB5	P10CR	FFC5	(Reserved)
FFA6	P3	FFB6	(Reserved)	FFC6	TREG0
FFA7	P38CR	FFB7	(Reserved)	FFC7	TREG1
FFA8	P4	FFB8	(Reserved)	FFC8	TREG2
FFA9	P4CR	FFB9	(Reserved)	FFC9	TREG3
FFAA	P5	FFBA	(Reserved)	FFCA	T01MOD
FFAB	P5CR	FFBB	(Reserved)	FFCB	T23MOD
FFAC	P6	FFBC	(Reserved)	FFCC	TFFCR
FFAD	P7	FFBD	(Reserved)	FFCD	TRDC
FFAE	P7CR	FFBE	(Reserved)	FFCE	TRUN
FFAF	P8	FFBF	(Reserved)	FFCF	CAP1L/TREG4L

Address	Symbol	Address	Symbol	Address	Symbol
FFD0	CAP1H/TREG4H	FFE0	IRF0	FFF0	(Reserved)
FFD1	CAP2L/TREG5L	FFE1	IRF1	FFF1	(Reserved)
FFD2	CAP2H/TREG5H	FFE2	IRF2	FFF2	SCMOD1
FFD3	T4MOD	FFE3	INTE0	FFF3	SCCR1
FFD4	T4FFCR	FFE4	INTE1	FFF4	SCBUF1
FFD5	(Reserved)	FFE5	INTE2	FFF5	BRGCR1
FFD6	ADCH	FFE6	(Reserved)	FFF6	SCMOD2
FFD7	ADMOD	FFE7	(Reserved)	FFF7	SCBUF2
FFD8	ADREG04	FFE8	DMAV0	FFF8	(Reserved)
FFD9	ADREG15	FFE9	(Reserved)	FFF9	(Reserved)
FFDA	ADREG26	FFEA	(Reserved)	FFFA	(Reserved)
FFDB	ADREG37	FFEB	DMAV1	FFFB	(Reserved)
FFDC	(Reserved)	FFEC	WDMOD	FFFC	(Reserved)
FFDD	(Reserved)	FFED	WDCR	FFFD	(Reserved)
FFDE	(Reserved)	FFEE	(Reserved)	FFFE	(Reserved)
FFDF	(Reserved)	FFEF	(Reserved)	FFFF	(Reserved)

(1) I/O Port

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
P0	Port 0	FFA0H	P07	P06	P05	P04	P03	P02	P01	P00
			R/W							
			Input mode							
P1	Port 1	FFA2H	P17	P16	P15	P14	P13	P12	P11	P10
			R/W							
			Input mode							
P2	Port 2	FFA4H	SA23	SA22	SA21	SA20	P23	P22	P21	P20
			R/W				R/W			
			Unde fined				Input mode			
			Shift Alternate reg. 0				Shared with (Stepping Motor Control Port 0 / Pattern Generation Port 0			
P3	Port 3	FFA6H	—	—	—	—	P33	P32	P31	P30
							R/W			
							Input	Input	1	1
P4	Port 4	FFA8H	P47	P46	P45	P44	P43	P42	P41	P40
			R/W							
			Input mode							
P5	Port 5	FFAAH	P57	P56	P55	P54	P53	P52	P51	P50
			R/W							
			Input mode							
P6	Port 6	FFACH	P67	P66	P65	P64	P63	P62	P61	P60
			R							
			Input only							
			Shared with analog input pin (AN0 to AN7)							
P7	Port 7	FFADH	P77	P76	P75	P74	P73	P72	P71	P70
			R/W							
			Input mode							
P8	Port 8	FFAFH	—	—	—	—	P83	P82	P81	P80
							R/W	R		R/W
							0	Input		1
P9	Port 9	FFB3H	SA93	SA92	SA91	SA90	P93	P92	P91	P90
			R/W				R/W			
			Unde fined				Input mode			
			Shift Alternate reg. 1				Shared with (Stepping Motor Control Port 1 / Pattern Generation Port 1			
P10	Port 10	FFB4H	—	—	—	—	—	—	P101	P100
									R/W	
									Input mode	

(2) I/O port control (1/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
P0CR	Port 0 Control Register	FFA1H (RMW disable)	P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C
			W							
			0							
			0: IN 1: OUT (I/O selected bit by bit)							
P1CR	Port 1 Control Register	FFA3H (RMW disable)	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT (I/O selected bit by bit)							
P29CR	Port 2/9 Control Register	FFA5H (RMW disable)	P93C	P92C	P91C	P90C	P23C	P22C	P21C	P20C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT (I/O selected bit by bit)							
P29FR	Port 2/9 Function Register	FFB2H	PAT1	CCW1	M1M	M1S	PAT0	CCW0	M0M	M0S
			R/W						R/W	R/W
			0	0	0	0	0	0	0	0
			0: 8Bit 1: 4Bit WR	0: Normal rotation 1: Reverse rotation	0: 1 or 2 excitation 1: 1-2 excitation	0: Port 1: SMC	0: 8Bit 1: 4Bit WR	0: Normal rotation 1: Reverse rotation	0: 1 or 2 excitation 1: 1-2 excitation	0: Port 1: SMC
P38CR	Port 3/8 Control Register	FFA7H (RMW disable)	ALEE	STBYS	–	–	P33C	P32C	WDTOUTC	RDE
			R/W	W			W	W	W	R/W
			(Note)	0			0	0	0	0
			ALE control 0: Port 1: ALE	P82 control 0: Port 1: $\overline{STBY}$			0: IN 1: OUT (I/O selected bit by bit)		P80 control 0: Disable 1: Enable	$\overline{RD}$ control 1: Always $\overline{RD}$ output (When <EXT> = 1)

(Note) Read / Write
R/W : Either read or write is possible
R : Only read is possible
W : Only write is possible
prohibit RMW : Prohibit Read Modefy Write (Prohibit RES / SET Instruction etc.)

(2) I/O port control (2/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
P4CR	Port 4 Control Register	FFA9H (RMW disable)	P47C	P46C	P45C	P44C	P43C	P42C	P41C	P40C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT							
P5CR	Port 5 Control Register	FFABH (RMW disable)	P57C	P56C	P55C	P54C	P53C	P52C	P51C	P50C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT (Select I/O on bit basis)							
P5FR	Port 5 Function Register	FFB0H	—	—	WAITC1	WAITC0	TO5S	TO4S	TO3S	TO1S
					R/W	R/W	R/W			
					0	0	0	0	0	0
					Wait control 00: 2 State Wait 01: Normal Wait 10: Non Wait 11: —		P52 control 0: Port 1: TO5	P51 control 0: Port 1: TO4	P57 control 0: Port 1: TO3	P55 control 0: Port 1: TO1
P7CR	Port 7 Control Register	FFAEH (RMW disable)	P77C	P76C	P75C	P74C	P73C	P72C	P71C	P70C
			W							
			0	0	0	0	0	0	0	0
			0: IN 1: OUT (Select I/O on bit basis)							
P7FR	Port 7 Function Register	FFB1H	ODE2	TXDC2	SCLKC2	ODE1	TXDC1	SCLKC1	—	—
			R/W							
			0	0	0	0	0	0		
			P77 0: CMOS 1: Open Drain	P77 control 0: Port 1: TXD2 output	P76 control 0: Port 1: SCLK2 output	P74 0: CMOS 1: Open Drain	P74 control 0: Port 1: TXD1 output	P73 control 0: Port 1: SCLK1 output		
P10CR	Port 10 Control Register	FFB5H	—	—	—	—	—	—	P101C	P100C
									W	W
									0	0
									0 : In 1 : Out	

(3) Timer/event counter control (1/3)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
TREG0	8Bit Timer Reg. 0	FFC6H (RMW disable)	—							
			W							
			Undefined							
TREG1	8Bit Timer Reg. 1	FFC7H (RMW disable)	—							
			W							
			Undefined							
TREG2	8Bit Timer Reg. 2	FFC8H (RMW disable)	—							
			W							
			Undefined							
TREG3	8Bit Timer Reg. 3	FFC9H (RMW disable)	—							
			W							
			Undefined							
T01MOD	Timer0, 1 Mode Register	FFCAH	T01M1	T01M0	PWM01	PWM00	T1CLK1	T1CLK0	T0CLK1	T0CLK0
			R/W		R/W		R/W		R/W	
			0	0	0	0	0	0	0	0
			00: 8Bit Timer 01: 16Bit Timer 10: 8Bit PPG 11: 8Bit PWM		00: — 01: 2^6-1 PWM 10: 2^7-1 Cycle 11: 2^8-1		00: TO0TRG 01: ϕT1 10: ϕT16 11: ϕT256		00: — 01: ϕT1 10: ϕT4 11: ϕT16	
T23MOD	Timer2, 3 Mode Register	FFCBH	T23M1	T23M0	PWM21	PWM20	T3CLK1	T3CLK0	T2CLK1	T2CLK0
			R/W		R/W		R/W		R/W	
			0	0	0	0	0	0	0	0
			00: 8Bit Timer 01: 16Bit Timer 10: 8Bit PPG 11: 8Bit PWM		00: — 01: 2^6-1 PWM 10: 2^7-1 Cycle 11: 2^8-1		00: TO2TRG 01: ϕT1 10: ϕT16 11: ϕT256		00: TI2 01: ϕT1 10: ϕT4 11: ϕT16	
TFFCR	8 bit Timer Flip-Flop Control Register	FFCCH	FF3C1	FF3C0	FF3IE	FF3IS	FF1C1	FF1C0	FF1IE	FF1IS
			W		R/W		W		R/W	
			—		0	0	—		0	0
			00: Invert TFF3 01: Set TFF3 10: Clear TFF3 11: Don't care		1: TFF3 Invert Enable	0: Inverts by 8-bit Timer 2 1: Inverts by Timer 3	00: Invert TFF1 01: Set TFF1 10: Clear TFF1 11: Don't care		1: TFF1 Invert Enable	0: Inverts by 8-bit Timer 0 1: Inverts by Timer 1

(3) Timer/event counter control (2/3)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
TRDC	Timer Reg. Double Buffer Control Register	FFCDH	M1T	—	—	—	—	TR4DE	TR2DE	TR0DE
			R/W					R/W		
			0					0	0	0
			0: Timer 2, 3 1: Timer 4					0: Duble Buffer Disable 1: Duble Buffer Enable		
TRUN	Timer Run Control Tegister	FFCEH	—	—	PRRUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN
					R/W					
					0	0	0	0	0	0
					Prescaler & Timer Run / Stop Control 0: Stop & Clear 1: Run (Count up)					
CAP1L	Capture Reg. 1	FFCFH	—							
			R							
			Undefined							
CAP1H		FFD0H	—							
			R							
			Undefined							
CAP2L	Capture Reg. 2	FFD1H	—							
			R							
			Undefined							
CAP2H		FFD2H	—							
			R							
			Undefined							
TREG4L	16Bit Timer Reg. 4	FFCFH (RMW disable)	—							
			W							
			Undefined							
TREG4H		FFD0H (RMW disable)	—							
			W							
			Undefined							
TREG5L	16Bit Timer Reg. 5	FFD1H (RMW disable)	—							
			W							
			Undefined							
TREG5H		FFD2H (RMW disable)	—							
			W							
			Undefined							

(3) Timer/event counter control (3/3)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
T4MOD	16 bit Timer Mode Register	FFD3H	CAP2T5	EQ5T5	CAP1IN	CAPM1	CAPM0	CLE	T4CLK1	T4CLK0
			R/W		W	R/W		R/W	R/W	
			0	0	1	0	0	0	0	0
			TFF5 inversion trigger 0: Disable 1: Enable		0: Soft-Capture 1: Don't care	Capture timing 00: Disable INT1 rise edge 01: TI4↑ TI5↑ INT1 rise edge 10: TI4↑ TI4↓ INT1 fall edge 11: TFF1↑ TFF1↓ INT1 rise edge		1: UC16 Clear Enable	Timer 4 Clock 00: TI4 01: φT1 (8/fc) 10: φT4 (32/fc) 11: φT16 (128/fc)	
T4FFCR	16 bit Timer F/F Control Register	FFD4H	TFF5C1	TFF5C0	CAP2T4	CAP1T4	EQ5T4	EQ4T4	TFFC1	TFF4C0
			W		R/W				W	
			—	—	0	0	0	0	—	—
			00: Invert TFF5 01: Set TFF5 10: Clear TFF5 11: Don't care ※ Always set at "11" when read out.		TFF4 inversion trigger 0: Disable Trigger 1: Enable Trigger				00: Invert TFF4 01: Set TFF4 10: Clear TFF4 11: Don't care ※ Always set at "11" when read out.	
					Invert when capturing UC value into CAP2	Invert when capturing UC value into CAP1	Invert when matching UC with TREG5	Invert when matching UC with TREG4		

(4) A/D converter control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
ADCH	A/D Control Select Register	FFD6H	—	—	—	—	—	—	—	ADCH2
										R/W
										0
										0: AN0~3 1: AN4~7
ADMOD	A/D Converter Mode Register	FFD7H	EOCF	ADBF	REPET	SCAN	ADCS	ADS	ADCH1	ADCH0
			R		R/W	R/W	R/W		R/W	
			0	0	0	0	0	0	0	0
			1: END	1: BUSY	1: Repeat Mode Set	1: Scan Mode Set	1: Low speed mode	1: START	Analog Input Channel Select	
ADREG04	A/D Result Register CH0, 4	FFD8H								
			R							
			Undefined							
			A/D conversion result of channel 0 or channel 4 is stored							
ADREG15	A/D Result Register CH1, 5	FFD9H								
			R							
			Undefined							
			A/D conversion result of channel 1 or channel 5 is stored							
ADREG26	A/D Result Register CH2, 6	FFDAH								
			R							
			Undefined							
			A/D conversion result of channel 2 or channel 6 is stored							
ADREG37	A/D Result Register CH3, 7	FFDBH								
			R							
			Undefined							
			A/D conversion result of channel 3 or channel 7 is stored							

(5) Interrupt control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
IRF0	Interrupt Regist Flang & IRF Clear	FFE0H (RMW disable)	IRF3	IRF2	IRF1	IRFAD	—	—	—	IRF0
			R (Only IRF clear code can be used to write)							
			0	0	0	0				0
			Interrupt Request Flag 1: Interrupt being requested (IRF is cleared to "0" by writing IRF clear code)							
IRF1		FFE1H (RMW disable)	EXF	—	IRFT5	IRFT4	IRFT3	IRFT2	IRFT1	IRFT0
			R		R					
			Undefined		0	0	0	0	0	0
			EXX instruction Reverses each time executed		1: Interrupt being requested					
IRF2		FFE2H (RMW disable)	EXT	—	IRFTX2	IRFRX2	IRFTX1	IRFRX1	—	—
			W		R					
			0		0	0	0	0		
			P1 control 0: I/O Port 1: Address $\overline{RD}$, $\overline{WR}$, ALE		1: Interrupt being requested					
INTE0	Interrupt Enable Mask Register	FFE3H	IE3	IE2	IE1	IEAD	—	—	—	IE0
			R/W							R/W
			0	0	0	0				0
			0: Disable 1: Enable							
INTE1		FFE4H	—	—	IET5	IET4	IET3	IET2	IET1	IET0
					0	0	0	0	0	0
			0: Disable 1: Enable							
INTE2		FFE5H	—	EDGE	IETX2	IERX2	IETX1	IERX1	—	—
				R/W	R/W					
				0	0	0	0	0		
				INT0 control 0: Level 1: Edge	0: Disable 1: Enable					

(6) HDMA Control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
DMAV0	HDMA Vector Register CH0	FFE8H	DV07	DV06	DV05	DV04	DV03	DV02	DV01	DV00
			W							
			0	0	0	0	0	0	0	0
DMAV1	HDMA Vector Register CH1	FFEBH	DV17	DV16	DV15	DV14	DV13	DV12	DV11	DV10
			W							
			0	0	0	0	0	0	0	0

(7) WDT Control

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
WDMOD	Watch Dog Timer Mode Register	FFECH	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	RESCR	DRIVE
			R/W			R/W			R/W	R/W
			1	0	0	0	0	0	1	0
			1: WDT Enable	WDT dctecting Time 00: 2^{16}/fc 01: 2^{18}/fc 10: 2^{20}/fc 11: 2^{22}/fc		Warming Up mode 0: 2^{14}/fc 1: 2^{16}/fc	Standby mode 00: RUN 01: STOP1 10: IDLE1 11: —		Watchdog timer out control 1: P80 is set as the WDTOUT pin and is conntected internally to the RESET pin.	1: Drive the pin even in the STOP mode
WDCR	Watch Dog Timer Control Register	FFEDH (RWM disable)	—							
			W							
			—							
			B1H: WDT Disable Code				4EH: WDT Clear Code			

(8) Serial Channel Control (1/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
SCMOD1	Serial Channel 1 Mode Register	FFF2H	TB81	CTSE1	RXE1	WU1	SM11	SM01	SC11	SC01
			R/W							
			Undefined	0	0	0	0	0	0	0
			Transmission bit-8 data	1: CTS Enable	1: Receive Enable	1: Wake Up Enable	00: I/O Interface 01: UART 7Bit 10: UART 8Bit 11: UART 9Bit		00: TO2TRG 01: BRG Mode 10: ϕ1 11: —	
SCCR1	Serial Channel 1 Control Register	FFF3H	RB81	EVEN1	PE1	OERR1	PERR1	FERR1	SCLKC1	IOC1
			R	R/W		R (Cleared to "0" by reading)			R/W	
			Undefined	0	0	0	0	0	0	0
			Bit 8 of receiving data	Parity 0: Odd 1: EVEN	1: Parity Enable	1: Error OverRun	Parity	Framing	0: SCLK1 (⌐↑) 1: SCLK1 (↓⌐)	0: SCLK1 output 1: SCLK1 input

(8) Serial Channel Control (2/2)

Symbol	Name	Address	MSB 7	6	5	4	3	2	1	LSB 0
SCBUF1	Serial Channel 1 Buffer Register	0FFF4H (RMW disable)	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10
			TB17	TB16	TB15	TB14	TB13	TB12	TB11	TB10
			R (Receiving) / W (Transmission)							
			Undefined							
BRGCR1	Serial Channel 1 Baud Rate Generater Control	FFF5H	Fixed to "0"	–	BG11	BG01	PS31	PS21	PS11	PS01
			R/W							
			0		0	0	0	0	0	0
					00: fc/4 01: fc/16 10: fc/64 11: fc/256		Divided frequency from prescaler			
SCMOD2	Serial Channel 2 Mode Register	FFF6H	FFSI	SMD1	SMD0	SIFT	CLK1	CLK0	SCKS2	SIOE
			R	R/W		R/W	R/W		R/W	R/W
			1	0	0	0	0	0	0	0
			0: Busy 1: Stop	Transmission mode 00: RESET 01: trsnsmission 10: receives 11: trsnsmission and receives		Transfer Sift 0: Rising edge 1: Falling edge	Transfer spead 00: fc/4 (ϕT0) 01: fc/8 (ϕT1) 10: fc/32 (ϕT4) 11: fc/128 (ϕT16)		Transfer clock 0: Internal clock 1: External clock	Transfer control 0: Disable 1: Enable
SCBUF2	Serial Channel 2 Buffer Register	FFF7H (RMW disable)	RB27	RB26	RB25	RB24	RB23	RB22	RB21	RB20
			TB27	TB26	TB25	TB24	TB23	TB22	TB21	TB20
			R (Receiving) / W (Transmission)							
			Undefined							