1. Features

- MPEGI/II-Layer 3 Hardwired Decoder
  - Stand-alone MP3 decoder
  - 48, 44.1, 32, 24, 22.05, 16 KHz sampling freq.
  - Separated digital volume control on left and right channels (software control using 31 steps)
  - Bass, medium, and Treble Control (31 steps)
  - Bass Boost sound effect.
  - Ancillary data extraction
  - "CRC Error" and "MPEG Frame Synchronization" indicators
- Programmable Audio Output for interfacing with common audio DAC available on the market
  - PCM format compatible
  - I^2S format compatible
- 8-bit MCU C51 core based (F_{MAX}= 20 MHz)
- 2304 bytes of Internal RAM
- 64 Kbytes of Code Memory
  - FLASH: T89C51SND1, ROM: T83C51SND1
- 4 Kbytes of Boot Flash Memory (T89C51SND1)
  - ISP: download from USB or UART to any external memory cards
- USB Rev 1.1 controller
  - "Full speed" data transmission
- Built-in PLL
  - MP3 Audio clocks
  - USB clock
- MultiMediaCard™ Interface Compatibility
- Atmel DataFlash™ SPI Interface Compatibility
- IDE/ATAPI Interface
- 2 Channels 10-bit ADC, 8KHz (8 true bit)
  - Battery voltage Monitoring
  - Voice recording controlled by software
- Up to 44 bits of General Purpose I/Os for:
  - 4-bit interrupt keyboard port for a 4 x n matrix
  - Smartmedia™ software interface
- Standard Two 16-bit Timers/Counters
- Hardware Watchdog Timer
- Standard Full Duplex UART with Baud Rate Generator
- 2-wire Master and Slave Modes Controller
- SPI Master and Slave Modes Controller
- Power Management
  - Power-On reset
  - Software programmable MCU clock
  - Idle mode, Power-Down mode
- Operating conditions:
  - 3V, ±10%, 25 mA typical operating at 25°C
  - -40°C to +85°C
- Packages
  - TQFP80, PLCC84 (development board)
  - Dice

Single Chip Microcontroller with MP3 Decoder and Man Machine Interface

T8xC51SND1

Rev. D – 15-Nov-01

2. Description

The T8xC51SND1 product is a fully integrated stand-alone hardwired MPEGI/II-Layer 3 decoder with a C51 microcontroller core handling data flow and MP3-player control.

The T89C51SND1 includes 64 Kbytes of FLASH memory and allows In System Programming through an embedded 4 Kbytes of Boot FLASH Memory.

The T83C51SND1 includes 64 Kbytes of ROM memory.

The T8xC51SND1 includes 2304 bytes of RAM memory.

The T8xC51SND1 provides all necessary features for man machine interface like timers, keyboard port, serial or parallel interface (USB, 2-wire, SPI, IDE), ADC input, I^2S output, and all external memory interface (NAND or NOR FLASH, SmartMedia, MultiMedia).

3. Typical Applications

- MP3-Player
- PDA, Camera, Mobile Phone MP3
- Car Audio/Multimedia MP3
- Home Audio/Multimedia MP3

4. Pin Description

4.1 Pinouts

Figure 1. T8xC51SND1 80-pin QFP Package

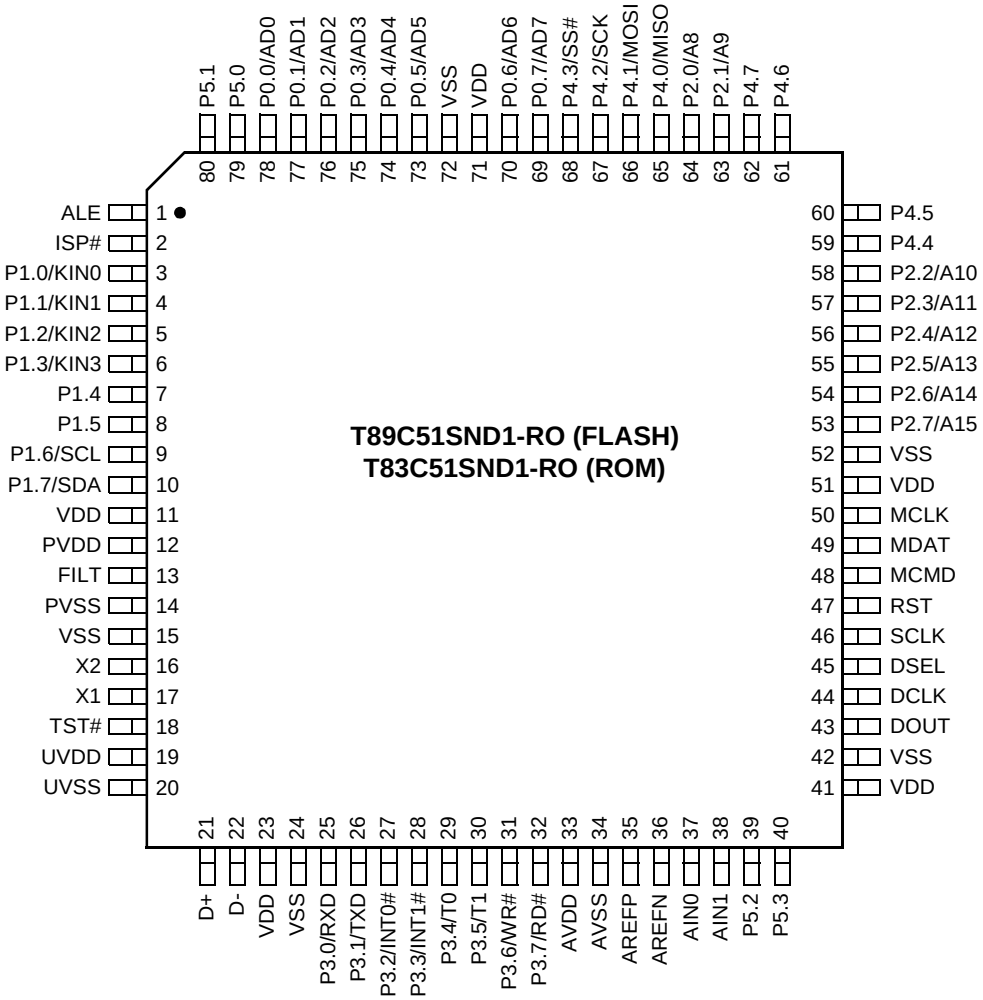
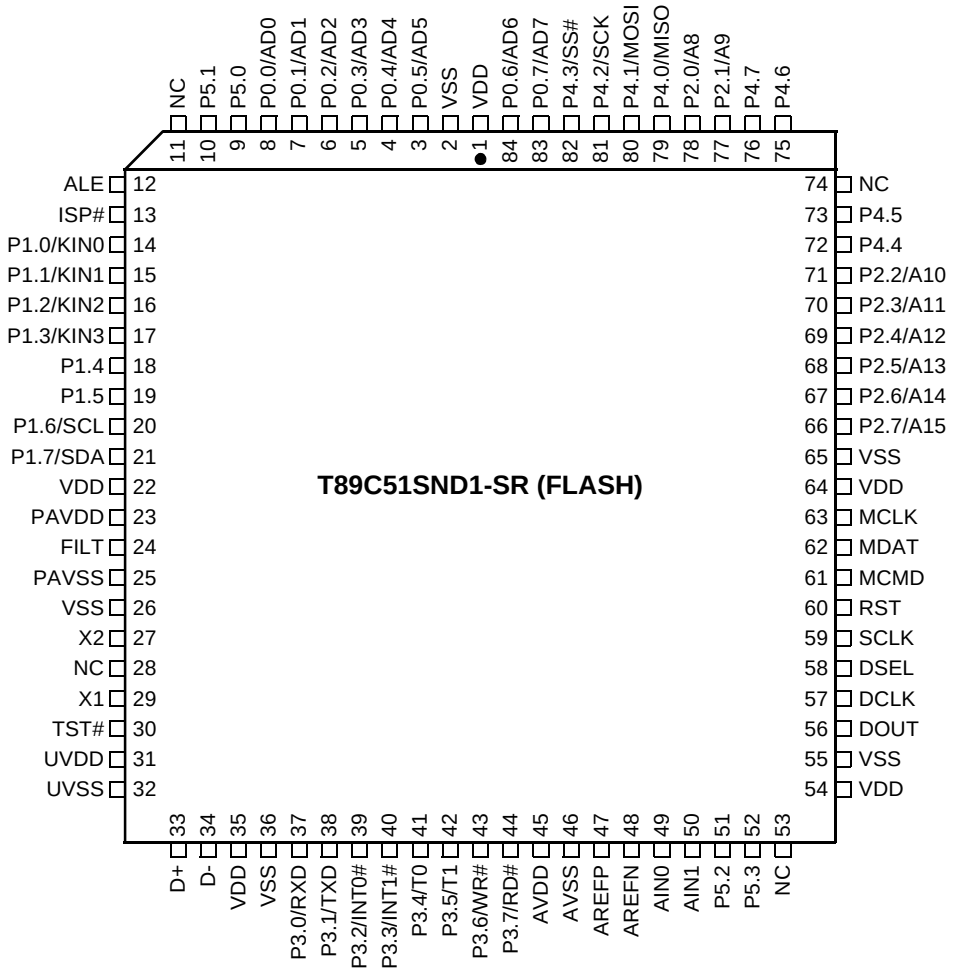


Figure 2. T8xC51SND1 84-pin PLCC Package



4.2 Signals

All the T8xC51SND1 signals are detailed by functionality in Table 1 to Table 14.

Table 1. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0.7:0	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.7:0	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups.	KIN3:0 SCL SDA

Signal Name	Type	Description	Alternate Function
P2.7:0	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.7:0	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	RXD TXD INT0# INT1# T0 T1 WR# RD#
P4.7:0	I/O	**Port 4** P4 is an 8-bit bidirectional I/O port with internal pull-ups.	MISO MOSI SCK SS#
P5.3:0	I/O	**Port 5** P5 is a 4-bit bidirectional I/O port with internal pull-ups.	-

Table 2. Clock Signal Description

Signal Name	Type	Description	Alternate Function
X1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. X1 is the clock source for internal timing.	-
X2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave X2 unconnected.	-
FILT	I	**PLL Low Pass Filter input** FILT receives the RC network of the PLL low pass filter.	-

Table 3. Timer 0 and Timer 1 Signal Description

Signal Name	Type	Description	Alternate Function
INT0#	I	**Timer 0 Gate Input** INT0# serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** INT0# input sets IE0 in the TCON register. If bit IT0 in this register is set, bit IE0 is set by a falling edge on INT0#. If bit IT0 is cleared, bit IE0 is set by a low level on INT0#.	P3.2
INT1#	I	**Timer 1 Gate Input** INT1# serves as external run control for timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** INT1# input sets IE1 in the TCON register. If bit IT1 in this register is set, bit IE1 is set by a falling edge on INT1#. If bit IT1 is cleared, bit IE1 is set by a low level on INT1#.	P3.3

Signal Name	Type	Description	Alternate Function
T0	I	**Timer 0 External Clock Input** When timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer 1 External Clock Input** When timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5

Table 4. Audio Interface Signal Description

Signal Name	Type	Description	Alternate Function
DCLK	O	**DAC Data Bit Clock**	-
DOUT	O	**DAC Audio Data**	-
DSEL	O	**DAC Channel Select Signal** DSEL is the sample rate clock output.	-
SCLK	O	**DAC System Clock** SCLK is the oversampling clock synchronized to the digital audio data (DOUT) and the channel selection signal (DSEL).	-

Table 5. USB Controller Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	**USB Positive Data Upstream Port** This pin requires an external 1.5 KΩ pull-up to V_{DD} for full speed operation.	-
D-	I/O	**USB Negative Data Upstream Port**	-

Table 6. MutiMediaCard Interface Signal Description

Signal Name	Type	Description	Alternate Function
MCLK	O	**MMC Clock output** Data or command clock transfer.	-
MCMD	I/O	**MMC Command line** Bidirectional command channel used for card initialization and data transfer commands. To avoid any parasitic current consumption, unused MCMD input must be polarized to V_{DD} or V_{SS}.	-
MDAT	I/O	**MMC Data line** Bidirectional data channel. To avoid any parasitic current consumption, unused MDAT input must be polarized to V_{DD} or V_{SS}.	-

Table 7. UART Signal Description

Signal Name	Type	Description	Alternate Function
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1

Table 8. SPI Controller Signal Description

Signal Name	Type	Description	Alternate Function
MISO	I/O	**SPI Master Input Slave Output Data Line** When in master mode, MISO receives data from the slave peripheral. When in slave mode, MISO outputs data to the master controller.	P4.0
MOSI	I/O	**SPI Master Output Slave Input Data Line** When in master mode, MOSI outputs data to the slave peripheral. When in slave mode, MOSI receives data from the master controller.	P4.1
SCK	I/O	**SPI Clock Line** When in master mode, SCK outputs clock to the slave peripheral. When in slave mode, SCK receives clock from the master controller.	P4.2
SS#	I	**SPI Slave Select Line** When in controlled slave mode, SS# enables the slave mode.	P4.3

Table 9. 2-wire Controller Signal Description

Signal Name	Type	Description	Alternate Function
SCL	I/O	**2-wire Serial Clock** When 2-wire controller is in master mode, SCL outputs the serial clock to the slave peripherals. When 2-wire controller is in slave mode, SCL receives clock from the master controller.	P1.6
SDA	I/O	**2-wire Serial Data** SDA is the bidirectional 2-wire data line.	P1.7

Table 10. A/D Converter Signal Description

Signal Name	Type	Description	Alternate Function
AIN1:0	I	**A/D Converter Analog Inputs**	-
AREFP	I	**Analog Positive Voltage Reference Input**	-
AREFN	I	**Analog Negative Voltage Reference Input** This pin is internally connected to AVSS.	-

Table 11. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN3:0	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt.	P1.3:0

Table 12. External Access Signal Description

Signal Name	Type	Description	Alternate Function
A15:8	I/O	**Address Lines** Upper address lines for the external bus. Multiplexed higher address and data lines for the IDE interface.	P2.7:0
AD7:0	I/O	**Address/Data Lines** Multiplexed lower address and data lines for the external memory or the IDE interface.	P0.7:0
ALE	O	**Address Latch Enable Output** ALE signals the start of an external bus cycle and indicates that valid address information is available on lines A7:0. An external latch is used to demultiplex the address from address/data bus.	-
ISP#	I/O	**ISP Enable Input** This signal must be held to GND through a pull-down resistor at the falling reset to force execution of the internal bootloader.	-
RD#	O	**Read Signal** Read signal asserted during external data memory read operation.	P3.7
WR#	O	**Write Signal** Write signal asserted during external data memory write operation.	P3.6

Table 13. System Signal Description

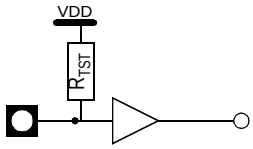
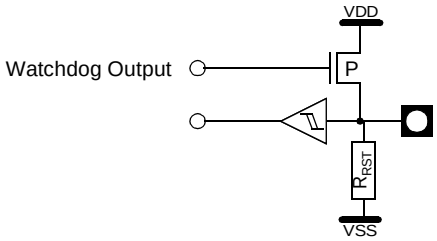
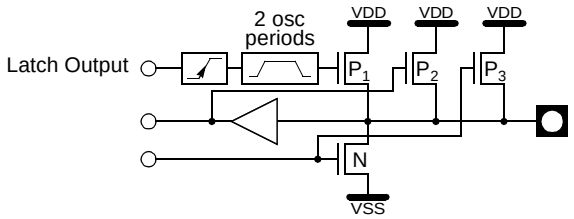
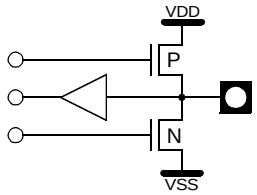
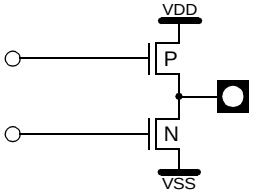
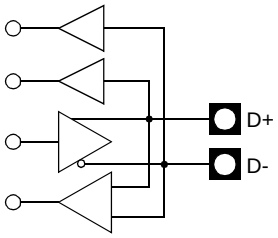
Signal Name	Type	Description	Alternate Function
RST	I	**Reset Input** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and V_{DD}. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	-
TST#	I	**Test Input** Test mode entry signal. This pin must be set to V_{DD}.	-

Table 14. Power Signal Description

Signal Name	Type	Description	Alternate Function
VDD	PWR	**Digital Supply Voltage** Connect these pins to +3V supply voltage.	-
VSS	GND	**Circuit Ground** Connect these pins to ground.	-
AVDD	PWR	**Analog Supply Voltage** Connect this pin to +3V supply voltage.	-
AVSS	GND	**Analog Ground** Connect this pin to ground.	-
PVDD	PWR	**PLL Supply voltage** Connect this pin to +3V supply voltage.	-
PVSS	GND	**PLL Circuit Ground** Connect this pin to ground.	-
UVDD	PWR	**USB Supply Voltage** Connect this pin to +3V supply voltage.	-
UVSS	GND	**USB Ground** Connect this pin to ground.	-

4.3 Internal Pin Structure

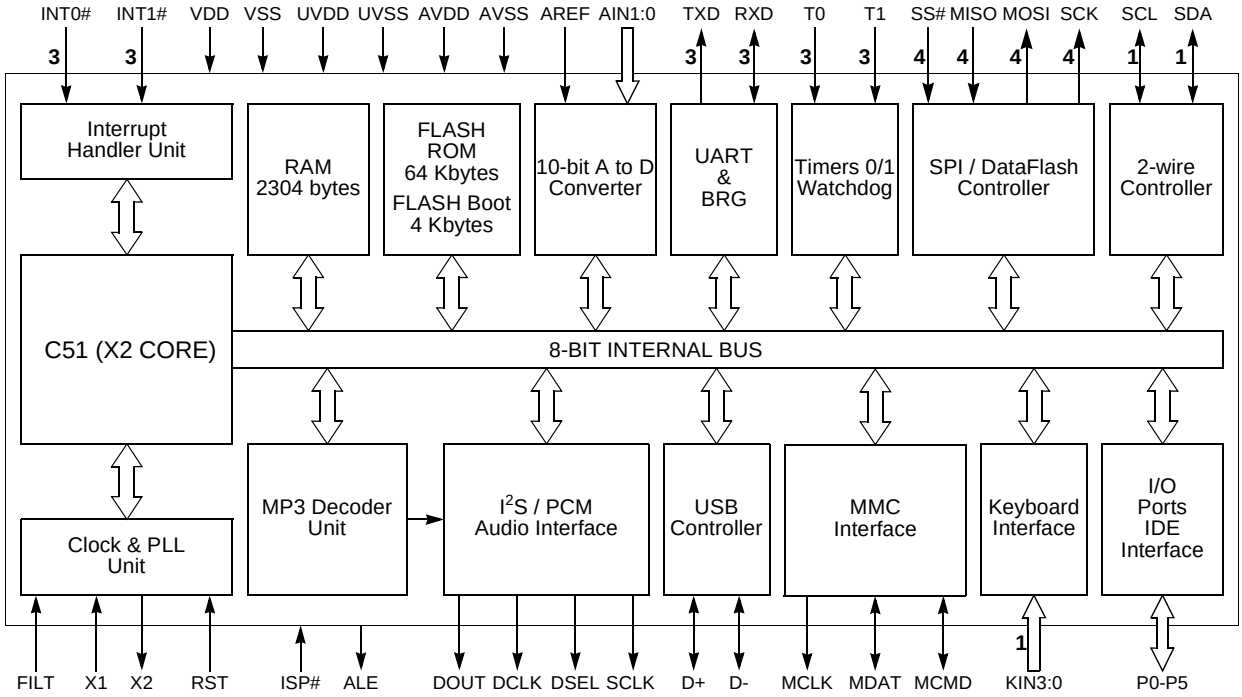
Table 15. Detailed Internal Pin Structure

Circuit[1]	Type	Pins
	Input	TST#
	Input/Output	RST
	Input/Output	P1[2] P2[3] P3 P4 P53:0
	Input/Output	P0 MCMD MDAT ISP#
	Output	ALE SCLK DCLK DOUT DSEL MCLK
	Input/Output	D+ D-

Notes:
1. For information on resistors value, input/output levels, and drive capability, refer to the Section “DC Characteristics”, page 34.
2. When the 2-wire controller is enabled, P_1, P_2, and P_3 transistors are disabled allowing pseudo open-drain structure.
3. In Port 2, P_1 transistor is continuously driven when outputting a high level bit address (A15:8).

5. Block Diagram

Figure 3. T8xC51SND1 Block Diagram



1 Alternate function of Port 1
3 Alternate function of Port 3
4 Alternate function of Port 4

6. Application Information

Figure 4. T8xC51SND1 Typical Application with On-Board Atmel DataFlash and 2-wire LCD

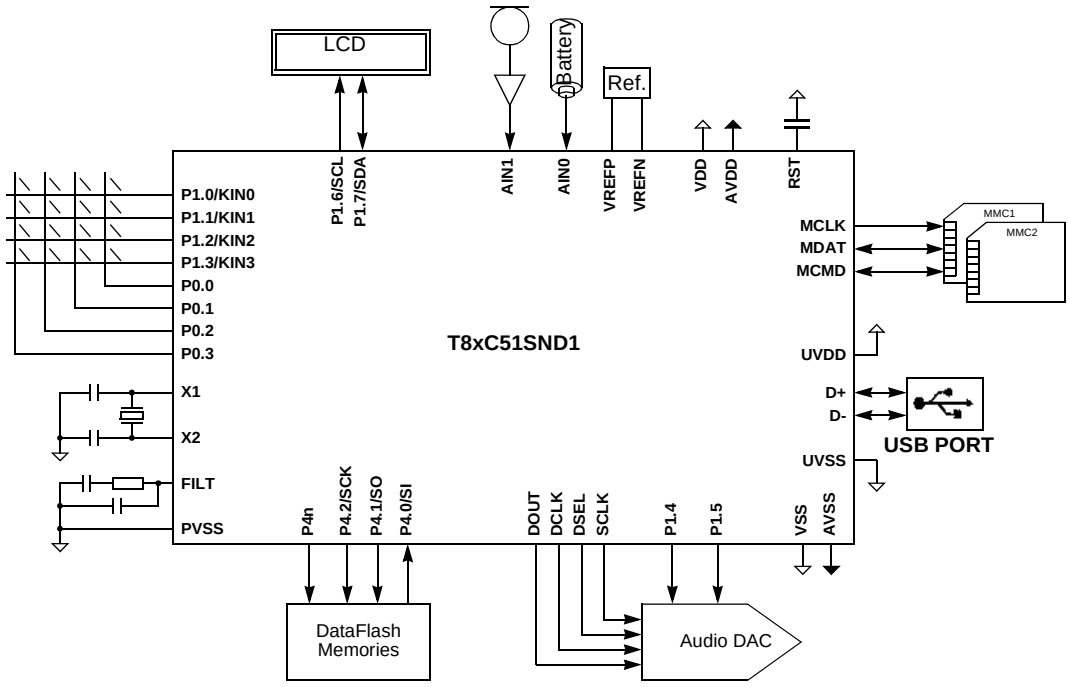


Figure 5. T8xC51SND1 Typical Application with On-Board Atmel DataFlash and // LCD

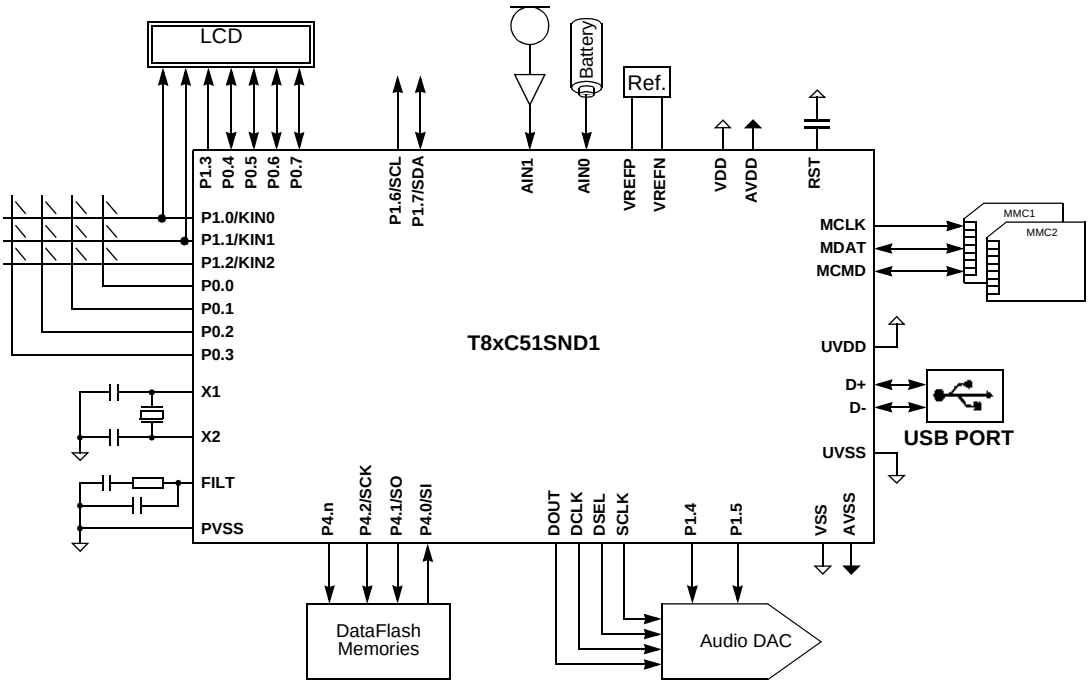


Figure 6. T8xC51SND1 Typical Application with On-Board SSFDC Flash

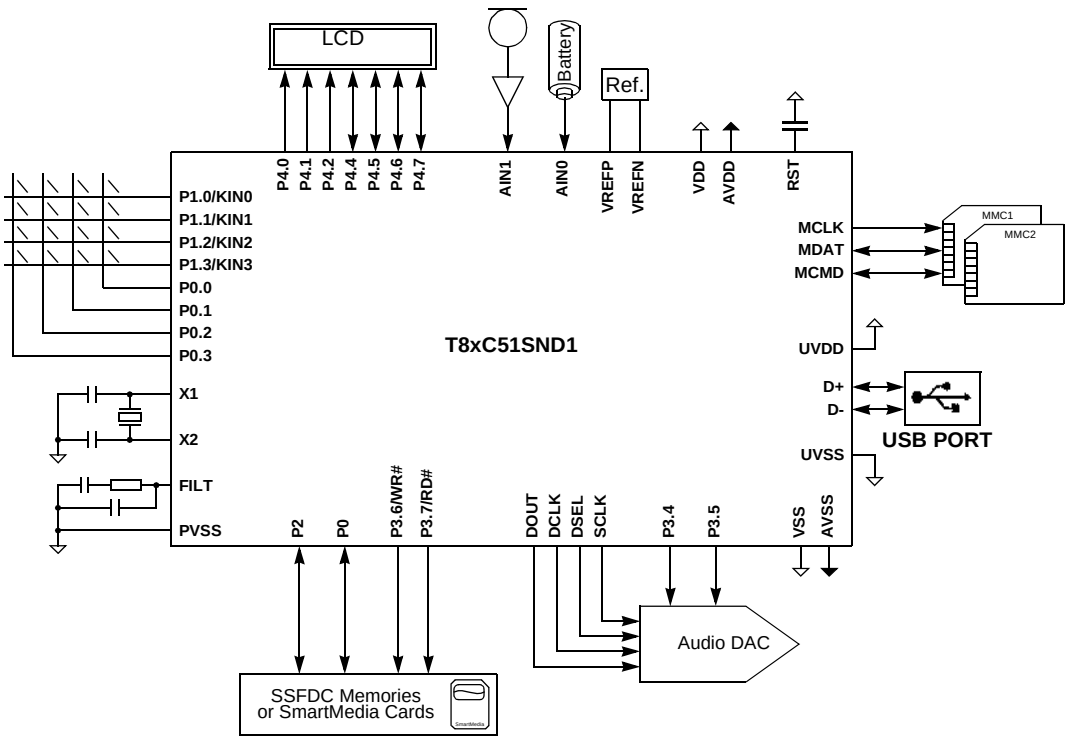
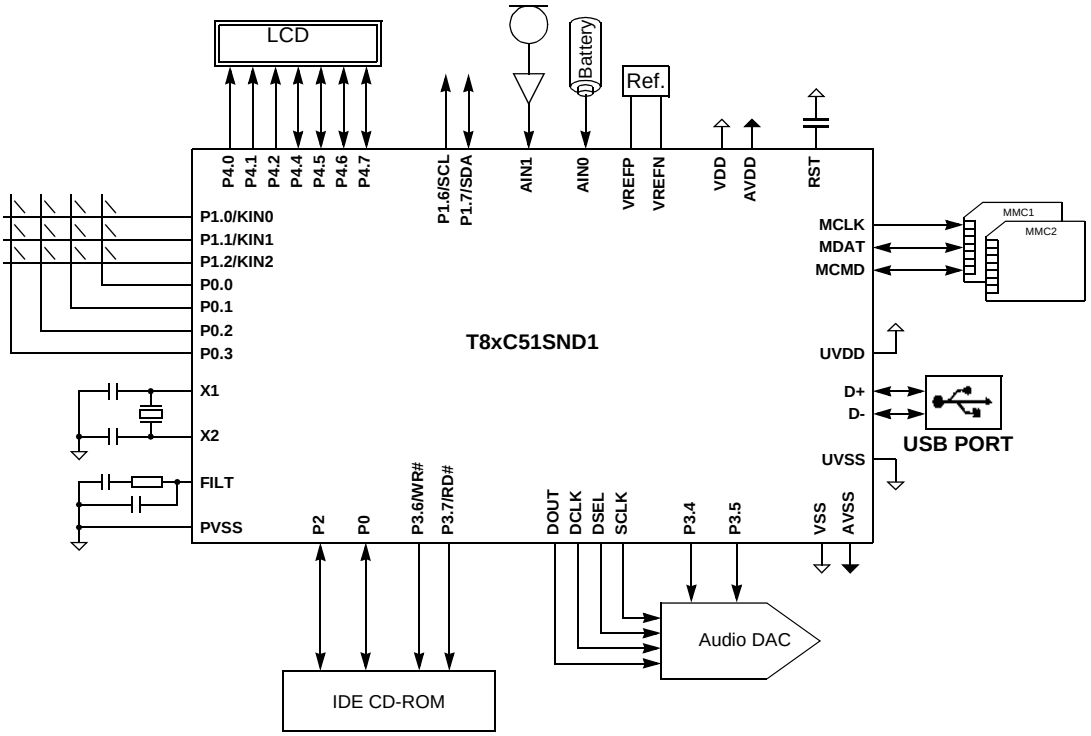


Figure 7. T8xC51SND1 Typical Application with IDE CD-ROM Drive



7. Address Spaces

The T8xC51SND1 derivatives implement four different address spaces:

- Program/Code Memory
- Boot Memory
- Data Memory
- Special Function Registers (SFRs)

7.1 Code Memory

The T89C51SND1 and T83C51SND1 implement 64 Kbytes of on-chip program/code memory. The T83C51SND1 product provides the internal program/code memory in ROM technology while the T89C51SND1 product provides it in FLASH technology.

The FLASH memory increases EPROM and ROM functionality by in-circuit electrical erasure and programming. Thanks to the internal charge pump, the high voltage needed for programming or erasing FLASH cells is generated on-chip using the standard VDD voltage. Thus, the T89C51SND1 can be programmed using only one voltage and allows in application software programming commonly known as IAP. Hardware programming mode is also available using specific programming tool.

7.2 Boot Memory

The T89C51SND1 implements 4 Kbytes of on-chip boot memory provided in FLASH technology. This boot memory is delivered programmed with a standard boot loader software allowing in system programming commonly known as ISP. It also contains some Application Programming Interfaces routines commonly known as API allowing user to develop its own boot loader.

7.3 Data Memory

The T89C51CC01 derivatives implement 2304 bytes of on-chip data RAM. This memory is divided in two separate areas:

- 256 bytes of on-chip RAM memory (standard C51 memory).
- 2048 bytes of on-chip expanded RAM memory (ERAM accessible via MOVX instructions).

7.4 Special Function Registers

The Special Function Registers (SFRs) of the T89C51CC01 derivatives fall into the categories detailed in Table 16 to Table 32. The relative addresses of these SFRs are provided together with their reset values in Table 33. In this table, the bit-addressable registers are identified by Note 1.

Table 16. C51 Core SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ACC	E0h	Accumulator								
B	F0h	B Register								
PSW	D0h	Program Status Word	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81h	Stack Pointer								
DPL	82h	Data Pointer Low byte								
DPH	83h	Data Pointer High byte								

Table 17. System Management SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
PCON	87h	Power Control	SMOD1	SMOD0	-	-	GF1	GF0	PD	IDL
AUXR	8Eh	Auxiliary Register 0	-	EXT16	M0	DPHDIS	XRS1	XRS0	EXTRAM	AO
AUXR1	A2h	Auxiliary Register 1	-	-	ENBOOT	-	GF3	0	-	DPS
NVERS	FBh	Version Number	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0

Table 18. PLL & System Clock SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
CKCON	8Fh	Clock Control	-	-	-	-	-	-	-	X2
PLLCON	E9h	PLL Control	R1	R0	-	-	PLLRES	-	PLLEN	PLOCK
PLLNDIV	EEh	PLL N Divider	-	N6	N5	N4	N3	N2	N1	N0
PLLRDIV	EFh	PLL R Divider	R9	R8	R7	R6	R5	R4	R3	R2

Table 19. Interrupt SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
IEN0	A8h	Interrupt Enable Control 0	EA	EAUD	EMP3	ES	ET1	EX1	ET0	EX0
IEN1	B1h	Interrupt Enable Control 1	-	EUSB	-	EKB	EADC	ESPI	EI2C	EMMC
IPH0	B7h	Interrupt Priority Control High 0	-	IPHAUD	IPHMP3	IPHS	IPHT1	IPHX1	IPHT0	IPHX0
IPL0	B8h	Interrupt Priority Control Low 0	-	IPLAUD	IPLMP3	IPLS	IPLT1	IPLX1	IPLT0	IPLX0
IPH1	B3h	Interrupt Priority Control High 1	-	IPHUSB	-	IPHKB	IPHADC	IPHSPI	IPHI2C	IPHMMC
IPL1	B2h	Interrupt Priority Control Low 1	-	IPLUSB	-	IPLKB	IPLADC	IPLSPI	IPLI2C	IPLMMC

Table 20. Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
P0	80h	8-bit Port 0								
P1	90h	8-bit Port 1								
P2	A0h	8-bit Port 2								
P3	B0h	8-bit Port 3								
P4	C0h	8-bit Port 4								
P5	D8h	4-bit Port 5	-	-	-	-				

Table 21. Flash Memory SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
FCON	D1h	Flash Control	FPL3	FPL2	FPL1	FPL0	FPS	FMOD1	FMOD0	FBUSY

Table 22. Timer SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
TCON	88h	Timer/Counter 0 and 1 Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
TMOD	89h	Timer/Counter 0 and 1 Modes	GATE1	C/T1#	M11	M01	GATE0	C/T0#	M10	M00
TL0	8Ah	Timer/Counter 0 Low Byte								
TH0	8Ch	Timer/Counter 0 High Byte								
TL1	8Bh	Timer/Counter 1 Low Byte								
TH1	8Dh	Timer/Counter 1 High Byte								
WDTRST	A6h	WatchDog Timer Reset								
WDTPRG	A7h	WatchDog Timer Program	-	-	-	-	-	WTO2	WTO1	WTO0

Table 23. MP3 Decoder SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MP3CON	AAh	MP3 Control	MPEN	MPBBST	CRCEN	MSKANC	MSKREQ	MSKLAY	MSKSYN	MSKCRC
MP3STA	C8h	MP3 Status	MPANC	MPREQ	ERRLAY	ERRSYN	ERRCRC	MPFS1	MPFS0	MPVER
MP3STA1	AFh	MP3 Status 1	-	-	-	MPFREQ	MPBREQ	-	-	-

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MP3DAT	ACh	MP3 Data	MPD7	MPD6	MPD5	MPD4	MPD3	MPD2	MPD1	MPD0
MP3ANC	ADh	MP3 Ancillary Data	AND7	AND6	AND5	AND4	AND3	AND2	AND1	AND0
MP3VOL	9Eh	MP3 Audio Volume Control Left	-	-	-	VOL4	VOL3	VOL2	VOL1	VOL0
MP3VOR	9Fh	MP3 Audio Volume Control Right	-	-	-	VOR4	VOR3	VOR2	VOR1	VOR0
MP3BAS	B4h	MP3 Audio Bass Control	-	-	-	BAS4	BAS3	BAS2	BAS1	BAS0
MP3MED	B5h	MP3 Audio Medium Control	-	-	-	MED4	MED3	MED2	MED1	MED0
MP3TRE	B6h	MP3 Audio Treble Control	-	-	-	TRE4	TRE3	TRE2	TRE1	TRE0
MP3CLK	EBh	MP3 Clock Divider	-	-	-	MPCD4	MPCD3	MPCD2	MPCD1	MPCD0

Table 24. Audio Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
AUDCON0	9Ah	Audio Control 0	JUST4	JUST3	JUST2	JUST1	JUST0	POL	DSIZ	HLR
AUDCON1	9Bh	Audio Control 1	SRC	DRQEN	MSREQ	MUDRN	-	DUP1	DUP0	AUDEN
AUDSTA	9Ch	Audio Status	SREQ	UDRN	AUBUSY	-	-	-	-	-
AUDDAT	9Dh	Audio Data	AUD7	AUD6	AUD5	AUD4	AUD3	AUD2	AUD1	AUD0
AUDCLK	ECh	Audio Clock Divider	-	-	-	AUCD4	AUCD3	AUCD2	AUCD1	AUCD0

Table 25. USB Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
USBCON	BCh	USB Global Control	USBE	SUSPCLK	SDRMWUP	-	UPRSM	RMWUPE	CONFG	FADDEN
USBADDR	C6h	USB Address	FEN	UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
USBINT	BDh	USB Global Interrupt	-	-	WUPCPU	EORINT	SOFINT	-	-	SPINT
USBIEN	BEh	USB Global Interrupt Enable	-	-	EWUPCPU	EEORINT	ESOFINT	-	-	ESPINT
UEPNUM	C7h	USB Endpoint Number	-	-	-	-	-	-	EPNUM1	EPNUM0
UEPCONX	D4h	USB Endpoint X Control	EPEN	-	-	-	DTGL	EPDIR	EPTYPE1	EPTYPE0
UEPSTAX	CEh	USB Endpoint X Status	DIR	-	STALLRQ	TXRDY	STLCRC	RXSETUP	RXOUT	TXCMP
UEPRST	D5h	USB Endpoint Reset	-	-	-	-	EP3RST	EP2RST	EP1RST	EP0RST
UEPINT	F8h	USB Endpoint Interrupt	-	-	-	-	EP3INT	EP2INT	EP1INT	EP0INT
UEPIEN	C2h	USB Endpoint Interrupt Enable	-	-	-	-	EP3INTE	EP2INTE	EP1INTE	EP0INTE

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
UEPDATX	CFh	USB Endpoint X Fifo Data	FDAT7	FDAT6	FDAT5	FDAT4	FDAT3	FDAT2	FDAT1	FDAT0
UBYCTX	E2h	USB Endpoint X Byte Counter	-	BYCT6	BYCT5	BYCT4	BYCT3	BYCT2	BYCT1	BYCT0
UFNUML	BAh	USB Frame Number Low	FNUM7	FNUM6	FNUM5	FNUM4	FNUM3	FNUM2	FNUM1	FNUM0
UFNUMH	BBh	USB Frame Number High	-	-	CRCOK	CRCERR	-	FNUM10	FNUM9	FNUM8
USBCLK	EAh	USB Clock Divider	-	-	-	-	-	-	USBCD1	USBCD0

Table 26. MMC Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
MMCON0	E4h	MMC Control 0	DRPTR	DTPTR	CRPTR	CTPTR	MBLOCK	DFMT	RFMT	CRCDIS
MMCON1	E5h	MMC Control 1	BLEN3	BLEN2	BLEN1	BLEN0	DATDIR	DATEN	RESPEN	CMDEN
MMCON2	E6h	MMC Control 2	MMCEN	DCR	CCR	-	-	DATD1	DATD0	FLOWC
MMSTA	DEh	MMC Control and Status	-	-	CBUSY	CRC16S	DATFS	CRC7S	RESPFS	CFLCK
MMINT	E7h	MMC Interrupt	MCBI	EORI	EOCI	EOFI	F2FI	F1FI	F2EI	F1EI
MMMSK	DFh	MMC Interrupt Mask	MCBM	EORM	EOCM	EOFM	F2FM	F1FM	F2EM	F1EM
MMCMD	DDh	MMC Command	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
MMDAT	DCh	MMC Data	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0
MMCLK	EDh	MMC Clock Divider	MMCD7	MMCD6	MMCD5	MMCD4	MMCD3	MMCD2	MMCD1	MMCD0

Table 27. IDE Interface SFR

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
DAT16H	F9h	High Order Data Byte	D15	D14	D13	D12	D11	D10	D9	D8

Table 28. Serial I/O Port SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SCON	98h	Serial Control	FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI
SBUF	99h	Serial Data Buffer								
SADEN	B9h	Slave Address Mask								
SADDR	A9h	Slave Address								
BDRCON	92h	Baud Rate Control				BRR	TBCK	RBCK	SPD	SRC
BRL	91h	Baud Rate Reload								

Table 29. SPI Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SPCON	C3h	SPI Control	SPR2	SPEN	SSDIS	MSTR	CPOL	CPHA	SPR1	SPR0
SPSTA	C4h	SPI Status	SPIF	WCOL	-	MODF	-	-	-	-
SPDAT	C5h	SPI Data	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0

Table 30. 2-wire Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
SSCON	93h	Synchronous Serial control	SSCR2	SSPE	SSSTA	SSSTO	SSI	SSAA	SSCR1	SSCR0
SSSTA	94h	Synchronous Serial Status	SSC4	SSC3	SSC2	SSC1	SSC0	0	0	0
SSDAT	95h	Synchronous Serial Data	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
SSADR	96h	Synchronous Serial Address	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSGC

Table 31. Keyboard Interface SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
KBCON	A3h	Keyboard Control	KINL3	KINL2	KINL1	KINL0	KINM3	KINM2	KINM1	KINM0
KBSTA	A4h	Keyboard Status	KPDE	-	-	-	KINF3	KINF2	KINF1	KINF0

Table 32. A/D Controller SFRs

Mnemonic	Add	Name	7	6	5	4	3	2	1	0
ADCON	F3h	ADC Control	-	ADIDL	ADEN	ADEOC	ADSST	-	-	ADCS
ADCLK	F2h	ADC Clock Divider	-	-	-	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0
ADDL	F4h	ADC Data Low Byte	-	-	-	-	-	-	ADAT1	ADAT0
ADDH	F5h	ADC Data High Byte	ADAT9	ADAT8	ADAT7	ADAT6	ADAT5	ADAT4	ADAT3	ADAT2

Table 33. SFR Addresses and Reset Values

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h	UEPINT 0000 0000	DAT16H XXXX XXXX		NVERS[2] 1000 0010					FFh
F0h	B[1] 0000 0000		ADCLK 0000 0000	ADCON 0000 0000	ADDL 0000 0000	ADDH 0000 0000			F7h
E8h		PLLCON 0000 1000	USBCLK 0000 0000	MP3CLK 0000 0000	AUDCLK 0000 0000	MMCLK 0000 0000	PLLNDIV 0000 0000	PLLRDIV 0000 0000	EFh
E0h	ACC[1] 0000 0000		UBYCTLX 0000 0000		MMCON0 0000 0000	MMCON1 0000 0000	MMCON2 0000 0000	MMINT 0000 0011	E7h
D8h	P5[1] XXXX 1111				MMDAT 1111 1111	MMCMD 1111 1111	MMSTA 0000 0000	MMMSK 1111 1111	DFh
D0h	PSW[1] 0000 0000	FCON[3] 1111 0000[4]			UEPCONX 0000 0000	UEPRST 0000 0000			D7h
C8h	MP3STA[1] 0000 0001						UEPSTAX 0000 0000	UEPDATX 0000 0000	CFh
C0h	P4[1] 1111 1111		UEPIEN 0000 0000	SPCON 0001 0100	SPSTA 0000 0000	SPDAT XXXX XXXX	USBADDR 1000 0000	UEPNUM 0000 0000	C7h
B8h	IPL0[1] X000 0000	SADEN 0000 0000	UFNUML 0000 0000	UFNUMH 0000 0000	USBCON 0000 0000	USBINT 0000 0000	USBIEN 0001 0000		BFh
B0h	P3[1] 1111 1111	IEN1 0000 0000	IPL1 0000 0000	IPH1 0000 0000	MP3BAS 0000 0000	MP3MED 0000 0000	MP3TRE 0000 0000	IPH0 X000 0000	B7h
A8h	IEN0[1] 0000 0000	SADDR 0000 0000	MP3CON 0011 1111		MP3DAT 0000 0000	MP3ANC 0000 0000		MP3STA1 0100 0001	AFh
A0h	P2[1] 1111 1111		AUXR1 XXXX 00X0	KBCON 0000 1111	KBSTA 0000 0000		WDTRST 0000 1000	WDTPRG 0000 1000	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	AUDCON0 0000 1000	AUDCON1 1011 0010	AUDSTA 1100 0000	AUDDAT 1111 1111	MP3VOL 0000 0000	MP3VOR 0000 0000	9Fh
90h	P1[1] 1111 1111	BRL 0000 0000	BDRCON XXX0 0000	SSCON 0000 0000	SSSTA 1111 1000	SSDAT 1111 1111	SSADR 1111 1110		97h
88h	TCON[1] 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR X000 1101	CKCON 0000 000X[5]	8Fh
80h	P0[1] 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON XXXX 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. SFR registers with least significant nibble address equal to 0 or 8 are bit-addressable.
2. NVERS reset value depends on the silicon version.
3. FCON register is only available in T89C51SND1 product.
4. FCON reset value is 00h in case of reset with hardware condition.
5. CKCON reset value depends on the X2B bit (programmed or unprogrammed) in the Hardware Byte.

8. In System & In Application Programming

8.1 Introduction

As described in the section “Program/Code Memory” of the T8xC51SND1 design guide, The T89C51SND1 implements a 4 Kbytes FLASH boot memory. This boot memory is delivered programmed with a standard boot loader software allowing In System Programming (ISP). It also contains some Application Programming Interface routines named API routines allowing In Application Programming (IAP) by using user’s own boot loader.

8.2 In System Programming

The ISP boot process is divided in two different processes: the hardware and software boot process detailed in the following sections.

8.3.1 Hardware Boot Process

As detailed in Figure 8 there are two hardware conditions that allow user executing the boot loader: the hardware and the programmed conditions.

Hardware condition

The hardware condition is based on the ISP# pin. When driving this pin to low level, the chip reset forces the execution of the boot loader software.
The hardware condition takes precedence on the programmed condition and always allows in system recovery when user’s memory has been corrupted.

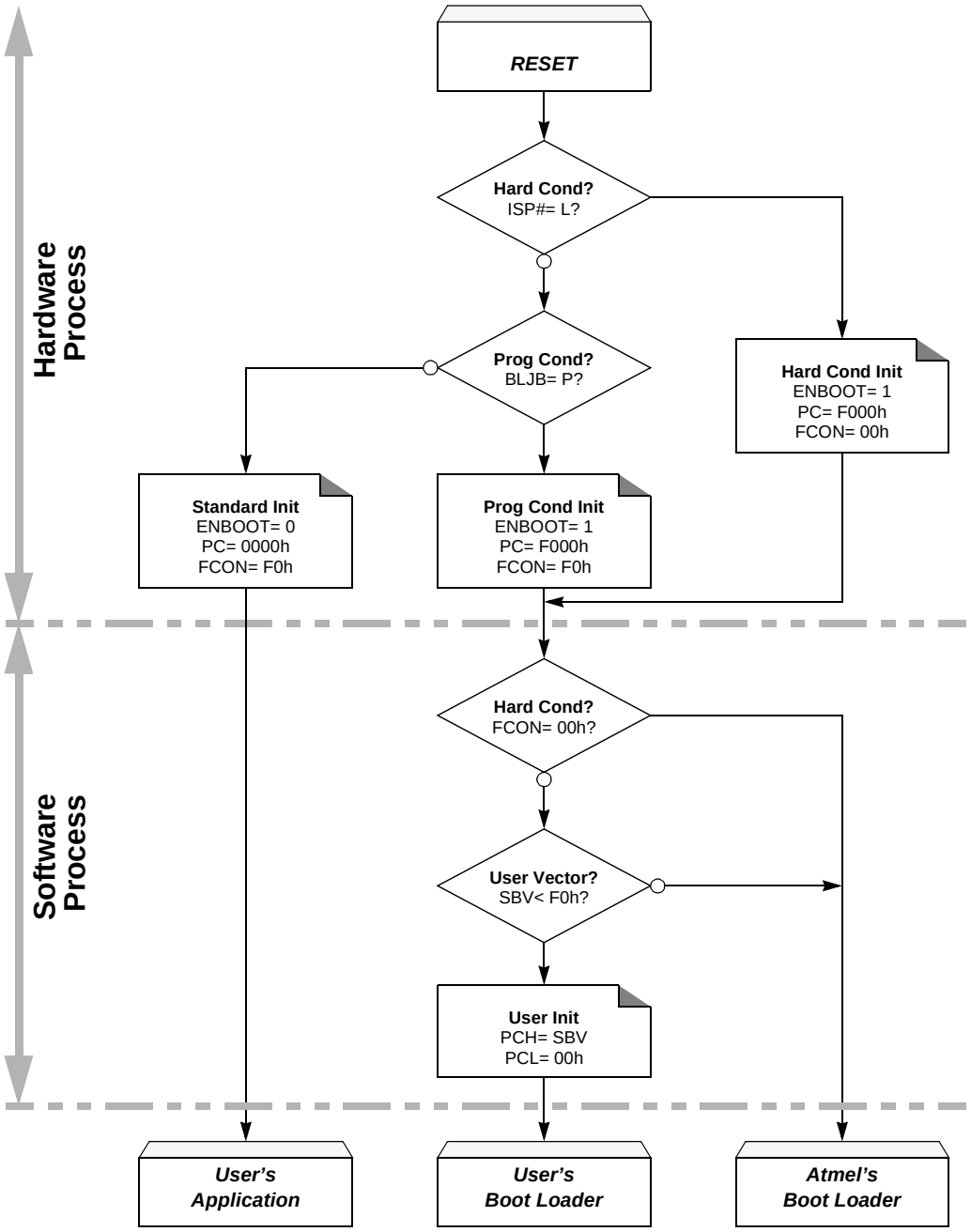
Programmed Condition

The programmed condition is based on the Boot Loader Jump Bit (BLJB) in the hardware security bytes (HSB). When this bit is programmed (by hardware or software programming mode), the chip reset forces the execution of the boot loader software.

8.4.2 Software Boot Process

Whatever the physical medium may be, the boot loader software always starts execution by testing FCON to know if execution comes from hardware or programmed condition. If it is from hardware condition, the Atmel’s boot loader is executed. If it is from programmed condition, the Software Boot Vector (SBV) is used to build a 16-bit address, SBV content being the MSB and the LSB being 00h. If this address is valid (< F000h), jump is done to this address to execute user’s boot loader. Otherwise jump is done to the Atmel’s boot loader. This implies that user’s boot loader does not execute any code mapped from F000h to FFFFh.

Figure 8. Boot Process Algorithm



8.5 Serial Boot Loader

8.6.1 Configuration

The serial boot loader is based on the internal UART and needs only 3 pins: the TXD and RXD pins of the UART and the VSS pin.
The data transmission format on the serial link must be set to 8 data bits with 1 stop bit. The baud rate is automatically recognized during the synchronization phase.

8.7.2 Synchronization Phase

Before any data may be sent to the boot loader, a synchronization must be achieved with the host so that both side converse at the same baud rate. This is done by sending the “U” character (ASCII 35h) to the boot loader. The boot loader acknowledges the synchronization by responding the same “U” character.
At this time, the boot loader is able to receive data, then all data received are echoed to the host.

8.8.3 Command Protocol

Definition

The protocol is based on the INTEL, HEX type records. These records are composed of seven fields of ASCII characters as detailed in Table 34. All fields except SOR (Start Of Record) end EOR (End Of Record) are ASCII coded hexadecimal values. The SOR field is always a “:” character. The EOR field is always a Carriage Return (ASCII 13h) followed by a Line Feed (ASCII 0Ah). The SIZE field is the size of the DATA field. The ADDRESS field is the address where to store data contained in the DATA field. The TYPE field is the record type detailed in Table 35. The DATA field contains the data and must never exceed 128 data bytes (256 ASCII characters). The CKSUM field is the checksum computed on the SIZE, ADDRESS, TYPE, DATA fields.

Table 34. Hex Record Format

SOR	SIZE	ADDRESS	TYPE	DATA	CKSUM	EOR
:	NN	AAAA	RR	DD…DD	CC	CR LF

Error Handling

All received records that present a checksum error, a data length greater than 128 bytes or a bad type record are immediately acknowledged to the host by sending a “X” character followed by a CRLF sequence.

Command description

Table 35. Hex Record Commands

TYPE	SIZE	ADDRESS	Description
00h	01h to 80h	0000h to FFFFh	**Program Data** Program the data in the DATA field at the address contained in the ADDRESS field. **Return** “.” Done. “P” Not done. Part protected (secured by level 1 or 2).
01h	00h	0000h	**End of File** No operation. **Return** “.”

TYPE	SIZE	ADDRESS	Description
03h	02h	XXXX	**Block Erase: DATA[0]= 01h** DATA[1]= 00h Erase block 0 from address 0000h to 1FFFh. DATA[1]= 20h Erase block 1 from address 2000h to 3FFFh. DATA[1]= 40h Erase block 2 from address 4000h to 7FFFh. DATA[1]= 80h Erase block 3 from address 8000h to BFFFh. DATA[1]= C0h Erase block 4 from address C000h to FFFFh. **Return** "." Done. "P" Not done. Part protected (secured by level 1 or 2).
	01h	XXXX	**Reset Software Boot Vector and Boot Status Byte: DATA[0]= 04h** Set SBV to F0h and BSB to FFh. **Return** "." Done. "P" Not done. Part protected (secured by level 1 or 2).
	02h	XXXX	**Program Software Security Bits: DATA[0]= 05h** DATA[1]= 00h Program level 1. Disable FLASH programming. DATA[1]= 01h Program level 2. Disable FLASH programming & verifying. **Return** "." Done. "P" Not done. Part protected (secured by level 1 or 2).
	03h	XXXX	**Program Software Boot Vector or Boot Status Byte: DATA[0]= 06h** DATA[1]= 00h Program BSB with DATA[2]. DATA[1]= 01h Program SBV with DATA[2]. **Return** "." Done. "P" Not done. Part already protected (secured by level 2).
	01h	XXXX	**Full Chip Erase: DATA[0]= 07h** Erase user memory from address 0000h to FFFFh. Set SBV to F0h and BSB to FFh. Program software security to level 0. **Return** "."
	03h	XXXX	**Program Fuse bits: DATA[0]= 0Ah** DATA[1]= 04h DATA[2]= 00h Program BLJB bit. DATA[2]= 01h Erase BLJB bit. DATA[1]= 08h DATA[2]= 00h Program X2 bit. DATA[2]= 01h Erase X2 bit. **Return** "." Done. "P" Not done. Part protected (secured by level 1 or 2).

TYPE	SIZE	ADDRESS	Description
04h	05h	XXXX	**Read Data: DATA[4]= 00h** Read data from address given by DATA[1:0] (start address) to address given by DATA[3:2] (end address). **Return** "AAAA=DD…DD" up to 16 data bytes by line.
	05h	XXXX	**Blank Check: DATA[4]= 01h** Check blanked data from address given by DATA[1:0] (start address) to address given by DATA[3:2] (end address). **Return** "." Done. "XXXX" First address not blanked.
05h	02h	XXXX	**Read Id: DATA[0]= 00h** DATA[1]= 00h Return manufacturer id. DATA[1]= 01h Return device id 1. DATA[1]= 02h Return device id 2. DATA[1]= 03h Return device id 3. **Return** "XX" Selected id value.
	02h	XXXX	**Read Special Bytes: DATA[0]= 07h** DATA[1]= 00h Return SSB. DATA[1]= 01h Return BSB. DATA[1]= 02h Return SBV. **Return** "XX" Selected byte value.
	01h	XXXX	**Read HSB: DATA[0]= 0Bh** Return HSB. **Return** "XX" HSB value.
	02h	XXXX	**Read Boot Id: DATA[0]= 0Eh** DATA[1]= 00h Return boot id 1. DATA[1]= 01h Return boot id 1. **Return** "XX" Selected id value.
	01h	XXXX	**Read Boot Loader Version: DATA[0]= 0Fh** Return boot loader version. **Return** "XX" Boot loader version.

8.9 In Application Programming

The IAP is based on several Application Program Interface routines (APIs) that may be called by the user's boot loader to allow programming of the FLASH memory.

The APIs are executed by calling the API_CALL function at address FFF0h and by passing the API routine number in R1 register. Some other parameters may also be passed in registers as detailed in Table 36.

Table 36. API Routines and Parameters

R1	Description
02h	**PROGRAM DATA BYTE** Program a data in the FLASH memory at a given address. **Parameters** DPTR Address of the byte to program. ACC Data to program. **Return** None.
09h	**PROGRAM DATA PAGE** Program a page of data in the FLASH memory at a given page address. **Parameters** DPTR0 Address of the page to program. DPTR1 Address in ERAM of the first data to program. ACC Number of bytes to program limited to 128. **Return** None.
05h	**PROGRAM SOFTWARE SECURITY BYTE** Program SSB. **Parameters** DPL 00h Program level 1. Disable FLASH programming. 01h Program level 2. Disable FLASH programming & verifying. **Return** None.
06h	**PROGRAM BOOT STATUS BYTE** Program BSB. **Parameters** DPL 00h Select BSB programming. ACC Data to program in BSB. **Return** None.
06h	**PROGRAM SOFTWARE BOOT VECTOR** Program SBV. **Parameters** DPL 01h Select SBV programming. ACC Data to program in SBV. **Return** None.
06h	**PROGRAM BOOT LOADER JUMP BIT** Program BLJB. **Parameters** DPL 04h Select BLJB programming. ACC 00h Program BLJB. 01h Erase BLJB. **Return** None.

R1	Description
06h	**PROGRAM X2 BIT** Program X2B. **Parameters** DPL 08h Select X2B programming. ACC 00h Program X2B. 01h Erase X2B. **Return** None.
01h	**Erase BLOCK** Erase one of the 5 available blocks. **Parameters** DPH 00h Erase block 0 from address 0000h to 1FFFh. 20h Erase block 1 from address 2000h to 3FFFh. 40h Erase block 2 from address 4000h to 7FFFh. 80h Erase block 3 from address 8000h to BFFFh. C0h Erase block 4 from address C000h to FFFFh. **Return** None.
04h	**ERASE SOFTWARE BOOT VECTOR and BOOT STATUS BYTE** Erase SBV and BSB. **Parameters** None. **Return** None.
03h	**READ DATA BYTE** Read data at a given address. **Parameters** DPTR Address of the byte to program. **Return** ACC Data read.
00h	**READ MANUFACTURER ID** Read manufacturer Id. **Parameters** DPL 00h Select manufacturer Id. **Return** ACC Id value.
00h	**READ DEVICE ID 1** Read device Id 1 **Parameters** DPL 01h Select device Id 1. **Return** ACC Id value.
00h	**READ DEVICE ID 2** Read device Id 2. **Parameters** DPL 02h Select device Id 2. **Return** ACC Id value.

R1	Description
00h	**READ DEVICE ID 3** Read device Id 3. **Parameters** DPL 03h Select device Id 3. **Return** ACC Id value.
07h	**READ SOFTWARE SECURITY BYTE** Read SSB. **Parameters** DPL 00h Select SSB. **Return** ACC SSB value.
07h	**READ BOOT STATUS BYTE** Read BSB. **Parameters** DPL 01h Select BSB. **Return** ACC BSB value.
07h	**READ SOFTWARE BOOT VECTOR** Read SBV. **Parameters** DPL 02h Select SBV. **Return** ACC SBV value.
0Bh	**READ HARDWARE SECURITY BYTE** Read HSB. **Parameters** None. **Return** ACC HSB value.
0Eh	**READ BOOT ID 1** Read boot Id 1. **Parameters** DPL 00h Select boot Id 1. **Return** ACC Id value.
0Eh	**READ BOOT ID 2** Read boot Id 2. **Parameters** DPL 01h Select boot Id 2. **Return** ACC Id value.
0Fh	**READ BOOT LOADER VERSION** Read BLV. **Parameters** None. **Return** ACC BLV value.

9. Peripherals

The T8xC51SND1 peripherals are briefly described in the following sections. For further details on how to interface (hardware and software) to these peripherals, please refer to the T8xC51SND1 design guide.

9.1 Clock Generator System

The T8xC51SND1 internal clocks are extracted from an on-chip PLL fed by an on-chip oscillator. Four clocks are generated respectively for the C51 core, the MP3 decoder, the audio interface, and the other peripherals. The C51 and peripheral clocks are derived from the oscillator clock. The MP3 decoder clock is generated by dividing the PLL output clock. The audio interface sample rates are also obtained by dividing the PLL output clock.

9.2 Ports

The T8xC51SND1 implements five 8-bit ports (P0 to P4) and one 4-bit port (P5). In addition to performing general-purpose I/O, some ports are capable of external data memory operations; others allow for alternate functions. All I/O Ports are bidirectional. Each Port contains a latch, an output driver and an input buffer. Port 0 and Port 2 output drivers and input buffers facilitate external memory operations. Some Port 1, Port 3 and Port 4 pins serve for both general-purpose I/O and alternate functions.

9.3 Timers/Counters

The T8xC51SND1 implements the two general-purpose, 16-bit Timers/Counters of a standard C51. They are identified as Timer 0, Timer 1, and can independently be configured each to operate in a variety of modes as a Timer or as an event Counter. When operating as a Timer, a Timer/Counter runs for a programmed length of time, then issues an interrupt request. When operating as a Counter, a Timer/Counter counts negative transitions on an external pin. After a preset number of counts, the Counter issues an interrupt request.

9.4 Watchdog Timer

The T8xC51SND1 implements a hardware Watchdog Timer that automatically resets the chip if it is allowed to time out. The WDT provides a means of recovering from routines that do not complete successfully due to software or hardware malfunctions.

9.5 MP3 Decoder

The T8xC51SND1 implements a MPEG I/II audio layer 3 decoder (known as MP3 decoder).
In MPEG I (ISO 11172-3) three layers of compression have been standardized supporting three sampling frequencies: 48, 44.1, and 32 KHz. Among these layers, layer 3 allows highest compression rate of about 12:1 while still maintaining CD audio quality. For example, 3 minutes of CD audio (16-bit PCM, 44.1 KHz) data, which needs about 32 MBytes of storage, can be encoded into only 2.7 MBytes of MPEG I audio layer 3 data.
In MPEG II (ISO 13818-3), three additional sampling frequencies: 24, 22.05, and 16 KHz are supported for low bit rates applications.
The T8xC51SND1 can decode in real-time the MPEG I audio layer 3 encoded data into a PCM audio data, and also supports MPEG II audio layer 3 additional frequencies.

Additional features are supported by the T8xC51SND1 MP3 decoder such as volume, bass, medium, and treble controls, bass boost effect and ancillary data extraction.

9.6 Audio Output Interface

The T8xC51SND1 implements an audio output interface allowing the decoded audio bit-stream to be output in various formats. It is compatible with right and left justification PCM and I^2S formats and thanks to the on-chip PLL (see Section 9.1) allows connection of almost all of the commercial audio DAC families available on the market.

9.7 Universal Serial Bus Interface

The T8xC51SND1 implements a full speed Universal Serial Bus Interface. It can be used for the following purposes:

- Download of MP3 encoded audio files by supporting the USB mass storage class.
- In System Programming by supporting the USB firmware upgrade class.

9.8 MultiMediaCard Interface

The T8xC51SND1 implements a MultiMediaCard (MMC) interface compliant to the V2.2 specification in MultiMediaCard Mode. The MMC allows storage of MP3 encoded audio files in removable flash memory cards that can be easily plugged or removed from the application. It can also be used for In System Programming.

9.9 IDE/ATAPI interface

The T8xC51SND1 provides an IDE/ATAPI interface allowing connexion of devices such as CD-ROM reader, CompactFlash cards, Hard Disk Drive… It consists in a 16-bit bidirectional bus part of the low-level ANSI ATA/ATAPI specification. It is provided for mass storage interface but could be used for In System Programming using CD-ROM.

9.10 Serial I/O Interface

The T8xC51SND1 implements a serial port with its own baud rate generator providing one single synchronous communication mode and three full-duplex Universal Asynchronous Receiver Transmitter (UART) communication modes. It is provided for the following purposes:

- In System Programming.
- Remote control of the T8xC51SND1 by a host.

9.11 Serial Peripheral Interface

The T8xC51SND1 implements a Serial Peripheral Interface (SPI) supporting master and slave modes. It is provided for the following purposes:

- Interfacing DataFlash memory for MP3 encoded audio files storage.
- Remote control of the T8xC51SND1 by a host.
- In System Programming.

9.12 2-wire Controller

The T8xC51SND1 implements a 2-wire controller supporting the four standard master and slave modes with multimaster capability. It is provided for the following purposes:

- Connection of slave devices like LCD controller, audio DAC…
- Remote control of the T8xC51SND1 by a host.
- In System Programming.

9.13 A/D Controller

The T8xC51SND1 implements a 2-channel 10-bit (8 true bits) analog to digital converter (ADC). It is provided for the following purposes:

- Battery monitoring.
- Voice recording.
- Corded remote control.

9.14 Keyboard Interface

The T8xC51SND1 implements a keyboard interface allowing connection of 4 x n matrix keyboard. It is based on 4 inputs with programmable interrupt capability on both high or low level. These inputs are available as alternate function of P1.3:0 and allow exit from idle and power down modes.

10. Absolute Maximum Rating and Operating Conditions

10.1 Absolute Maximum Rating

Table 37. Absolute Maximum Ratings

Storage Temperature	-65 to +150°C
Voltage on any other Pin to V_{SS}	-0.3 to +4.0 V
I_{OL} per I/O Pin	5 mA
Power Dissipation	1 W

10.2 Operating Conditions

Table 38. Operating Conditions

Ambient Temperature Under Bias	-40 to +85°C
V_{DD}	2.7 to 3.3V

Note: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

11. DC Characteristics

11.1 DC Characteristics - Digital Logic

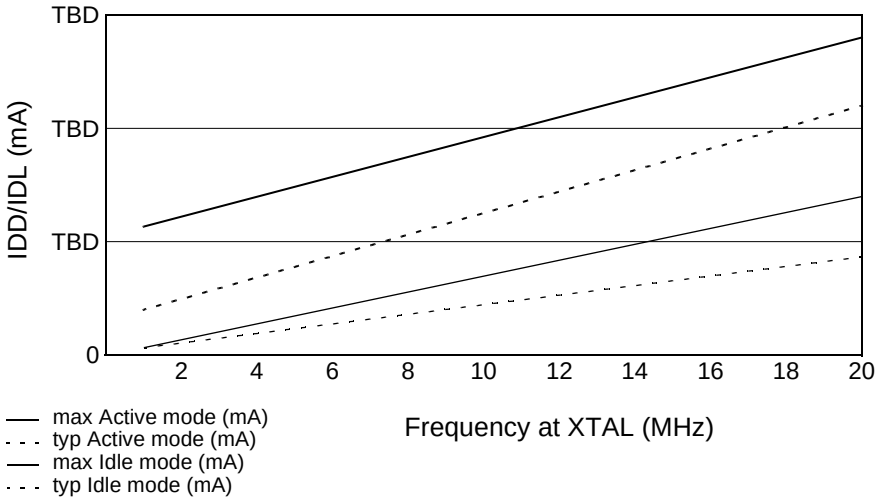
Table 39. Digital DC Characteristics

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Min	Typ[1]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IH1}	Input High Voltage (except RST)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD}	V	
V_{IH2}	Input High Voltage (RST)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL1}	Output Low Voltage (except P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL}= 1.6 mA
V_{OL2}	Output Low Voltage (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			0.45	V	I_{OL}= 3.2 mA
V_{OH1}	Output High Voltage (P1, P2, P3, P4 and P5)	V_{DD} - 0.7			V	I_{OH}= -30 µA
V_{OH2}	Output High Voltage (P0, P2 address mode, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)	V_{DD} - 0.7			V	I_{OH}= -3.2 mA
I_{IL}	Logical 0 Input Current (P1, P2, P3, P4 and P5)			-50	µA	Vin = 0.45 V
I_{LI}	Input Leakage Current (P0, ALE, MCMD, MDAT, MCLK, SCLK, DCLK, DSEL, DOUT)			10	µA	$0.45 < V_{IN} < V_{DD}$
I_{TL}	Logical 1 to 0 Transition Current (P1, P2, P3, P4 and P5)			-650	µA	Vin = 2.0 V
R_{RST}	Pull-Down Resistor	50	90	200	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A= 25°C
V_{RET}	V_{DD} Data Retention Limit			1.8	V	
I_{DD}	Operating Current		TBD	TBD	mA	12 MHz, V_{DD} < 3.3 V 16 MHz, V_{DD} < 3.3 V 20 MHz, V_{DD} < 3.3 V
I_{DL}	Idle Mode Current		TBD	TBD	mA	12 MHz, V_{DD} < 3.3 V 16 MHz, V_{DD} < 3.3 V 20 MHz, V_{DD} < 3.3 V
I_{PD}	Power-Down Current		TBD	TBD	µA	$V_{RET} < V_{DD} < 3.3$ V

Notes: 1. Typical values are obtained using V_{DD}= 3 V and T_A= 25°C. They are not tested and there is no guarantee on these values.

Figure 9. I_{DD}/I_{DL} Versus X_{TAL} Frequency; V_{DD}= 2.7 to 3.3 V



11.2 DC Characteristics - I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 10. I_{DD} Test Condition, Active Mode

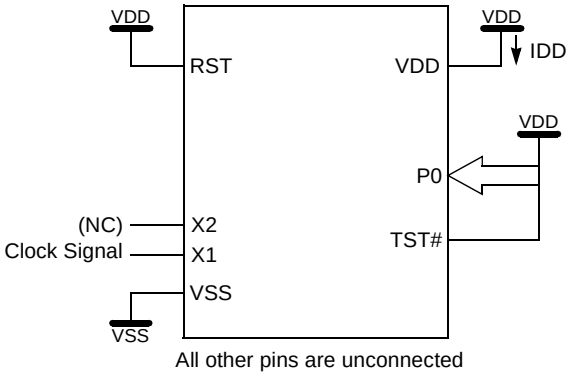


Figure 11. I_{DL} Test Condition, Idle Mode

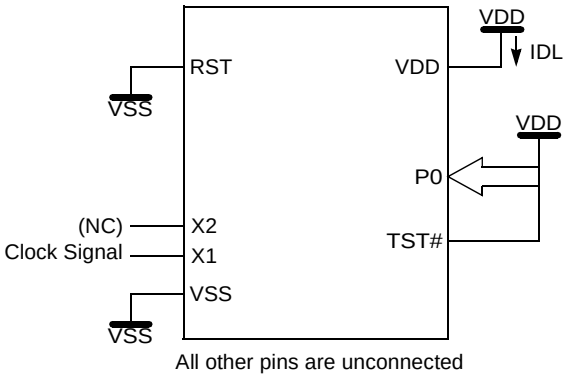
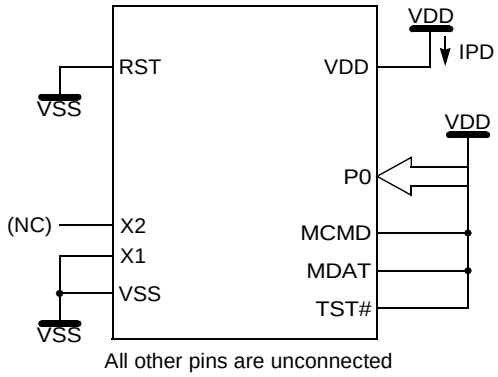


Figure 12. I_{PD} Test Condition, Power-Down Mode



11.3 DC Characteristics - A to D Converter

Table 40. A to D Converter DC Characteristics

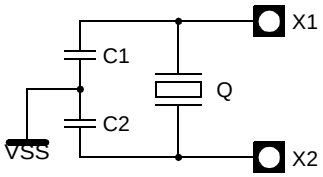
VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
AV_{DD}	Analog Supply Voltage	2.7		3.3	V	
AI_{DD}	Analog Operating Supply Current			600	µA	AV_{DD}= 3.3V AIN1:0= 0 to AV_{DD}
AI_{PD}	Analog Standby Current			2	µA	AV_{DD}= 3.3V ADEN= 0 or PD= 1
AV_{IN}	Analog Input Voltage	AV_{SS}		AV_{DD}	V	
AV_{REF}	Reference Voltage A_{REFN} A_{REFP}	 AV_{SS} 2.4		 AV_{DD}	 V V	
R_{REF}	AREF Input Resistance	10		30	KΩ	T_A= 25°C
C_{IA}	Analog Input capacitance			10	pF	T_A= 25°C

11.4 DC Characteristics - Oscillator & Crystal

11.5.1 Schematic

Figure 13. Crystal Connection



Note: For operation with most standard crystals, no external components are needed on X1 and X2. It may be necessary to add external capacitors on X1 and X2 to ground in special cases (max 10 pF). X1 and X2 may not be used to drive other circuits.

11.6.2 Parameters

Table 41. Oscillator & Crystal Characteristics

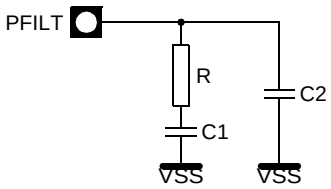
VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
C_{X1}	Internal Capacitance (X1 - VSS)		10		pF
C_{X2}	Internal Capacitance (X2 - VSS)		10		pF
C_L	Equivalent Load Capacitance (X1 - X2)		5		pF
DL	Drive Level			50	µW
F	Crystal Frequency			20	MHz
RS	Crystal Series Resistance			40	Ω
CS	Crystal Shunt Capacitance			6	pF

11.7 DC Characteristics - Phase Lock Loop

11.8.1 Schematic

Figure 14. PLL Filter Connection



11.9.2 Parameters

Table 42. PLL Filter Characteristics

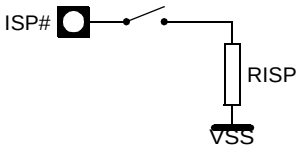
VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R	Filter Resistor		100		Ω
C1	Filter Capacitance 1		10		nF
C2	Filter Capacitance 2		2.2		nF

11.10 DC Characteristics - In System Programming

11.11.1 Schematic

Figure 15. ISP Pull-Down Connection



11.12.2 Parameters

Table 43. ISP Pull-Down Characteristics

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
R_{ISP}	ISP Pull-Down Resistor		2.2		KΩ

12. AC Characteristics

12.1 AC Characteristics - External 8-bit Bus Cycles

12.2.1 Definition of symbols

Table 44. External 8-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

12.3.2 Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 45. External 8-bit Bus Cycle - Data Read AC Timings

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLRL}	ALE Low to RD# Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{RLRH}	RD# Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	RD# high to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to RD# Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	RD# Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	RD# Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After RD# High	0		0		ns
T_{RHDZ}	Instruction Float After RD# High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

Table 46. External 8-bit Bus Cycle - Data Write AC Timings

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to WR# Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	WR# Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	WR# High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to WR# Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to WR# High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after WR# High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

12.4.3 Waveforms

Figure 16. External 8-bit Bus Cycle - Data Read Waveforms

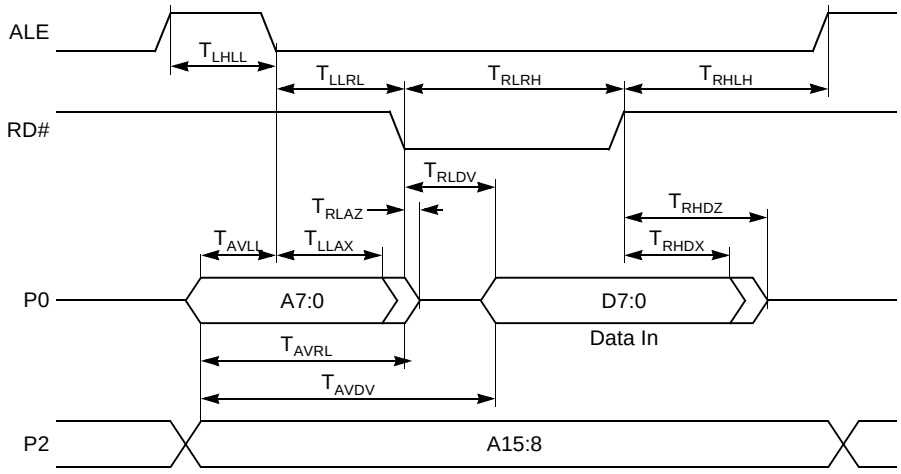
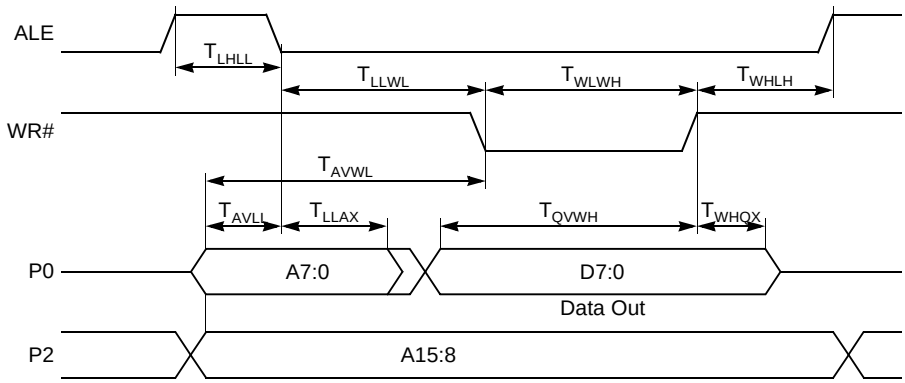


Figure 17. External 8-bit Bus Cycle - Data Write Waveforms


ALE
WR#
P0
P2
T_{LHLL}
T_{LLWL}
T_{WLWH}
T_{WHLH}
T_{AVWL}
T_{AVLL}
T_{LLAX}
T_{QVWH}
T_{WHQX}
A7:0
D7:0
Data Out
A15:8

12.5 AC Characteristics - External IDE 16-bit Bus Cycles

12.6.1 Definition of symbols

Table 47. External IDE 16-bit Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

12.7.2 Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 48. External IDE 16-bit Bus Cycle - Data Read AC Timings

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}-15$		$T_{CLCL}-15$		ns
T_{AVLL}	Address Valid to ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLAX}	Address hold after ALE Low	$T_{CLCL}-20$		$0.5 \cdot T_{CLCL}-20$		ns
T_{LLRL}	ALE Low to RD# Low	$3 \cdot T_{CLCL}-30$		$1.5 \cdot T_{CLCL}-30$		ns
T_{RLRH}	RD# Pulse Width	$6 \cdot T_{CLCL}-25$		$3 \cdot T_{CLCL}-25$		ns
T_{RHLH}	RD# high to ALE High	$T_{CLCL}-20$	$T_{CLCL}+20$	$0.5 \cdot T_{CLCL}-20$	$0.5 \cdot T_{CLCL}+20$	ns
T_{AVDV}	Address Valid to Valid Data In		$9 \cdot T_{CLCL}-65$		$4.5 \cdot T_{CLCL}-65$	ns
T_{AVRL}	Address Valid to RD# Low	$4 \cdot T_{CLCL}-30$		$2 \cdot T_{CLCL}-30$		ns
T_{RLDV}	RD# Low to Valid Data		$5 \cdot T_{CLCL}-30$		$2.5 \cdot T_{CLCL}-30$	ns
T_{RLAZ}	RD# Low to Address Float		0		0	ns
T_{RHDX}	Data Hold After RD# High	0		0		ns
T_{RHDZ}	Instruction Float After RD# High		$2 \cdot T_{CLCL}-25$		$T_{CLCL}-25$	ns

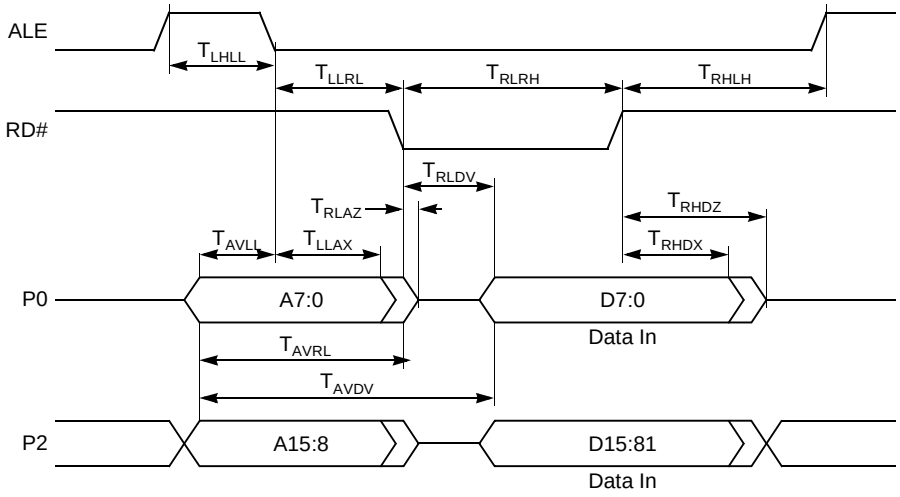
Table 49. External IDE 16-bit Bus Cycle - Data Write AC Timings

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Variable Clock Standard Mode		Variable Clock X2 Mode		Unit
		Min	Max	Min	Max	
T_{CLCL}	Clock Period	50		50		ns
T_{LHLL}	ALE Pulse Width	$2 \cdot T_{CLCL}$-15		T_{CLCL}-15		ns
T_{AVLL}	Address Valid to ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLAX}	Address hold after ALE Low	T_{CLCL}-20		$0.5 \cdot T_{CLCL}$-20		ns
T_{LLWL}	ALE Low to WR# Low	$3 \cdot T_{CLCL}$-30		$1.5 \cdot T_{CLCL}$-30		ns
T_{WLWH}	WR# Pulse Width	$6 \cdot T_{CLCL}$-25		$3 \cdot T_{CLCL}$-25		ns
T_{WHLH}	WR# High to ALE High	T_{CLCL}-20	T_{CLCL}+20	$0.5 \cdot T_{CLCL}$-20	$0.5 \cdot T_{CLCL}$+20	ns
T_{AVWL}	Address Valid to WR# Low	$4 \cdot T_{CLCL}$-30		$2 \cdot T_{CLCL}$-30		ns
T_{QVWH}	Data Valid to WR# High	$7 \cdot T_{CLCL}$-20		$3.5 \cdot T_{CLCL}$-20		ns
T_{WHQX}	Data Hold after WR# High	T_{CLCL}-15		$0.5 \cdot T_{CLCL}$-15		ns

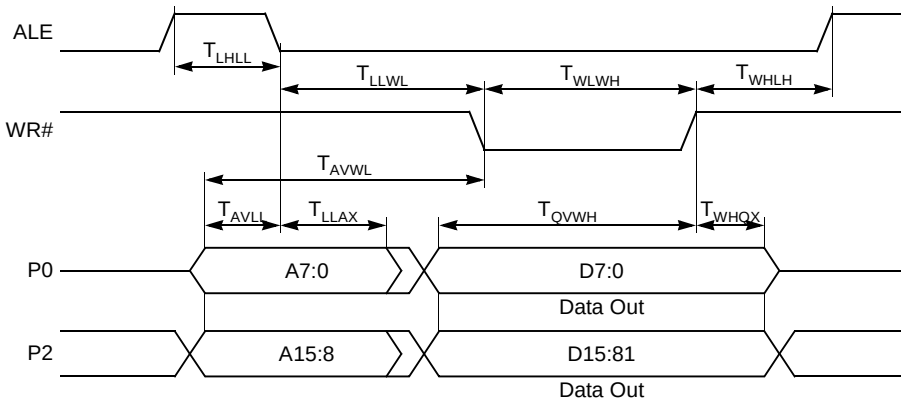
12.8.3 Waveforms

Figure 18. External IDE 16-bit Bus Cycle - Data Read Waveforms



Note: D15:8 is written in DAT16H SFR.

Figure 19. External IDE 16-bit Bus Cycle - Data Write Waveforms



Note: D15:8 is the content of DAT16H SFR.

12.9 AC Characteristics - SPI Interface

12.10.1 Definition of symbols

Table 50. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

12.11.2 Timings

Test conditions: capacitive load on all pins= 100 pF.

Table 51. SPI Interface Master AC Timing

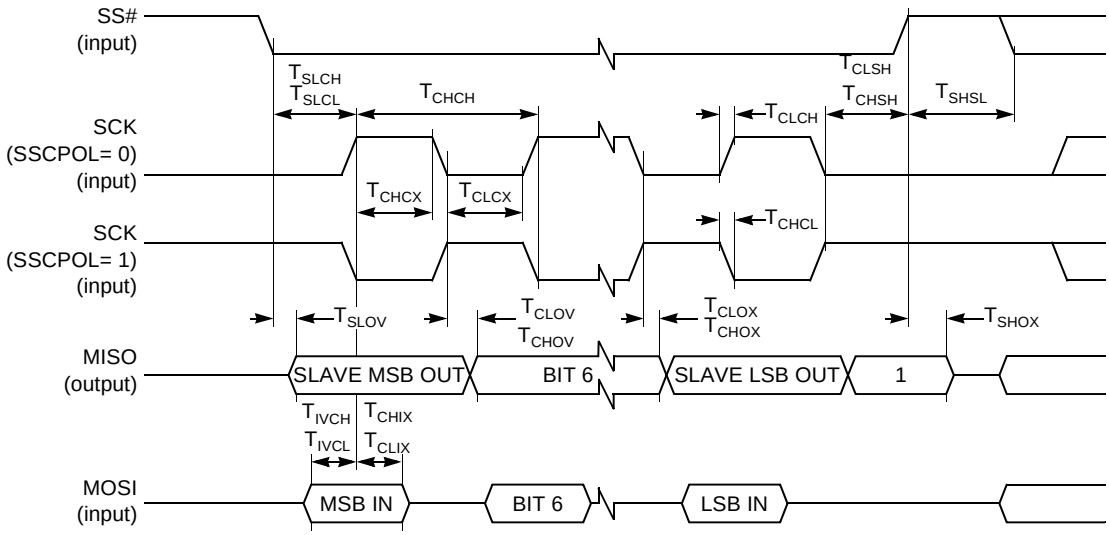
VDD= 2.7 to 3.3 V, T_A= -40 to +85°C

Symbol	Parameter	Min	Max	Unit
Slave mode				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(1)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master mode				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Value of this parameter depends on software.

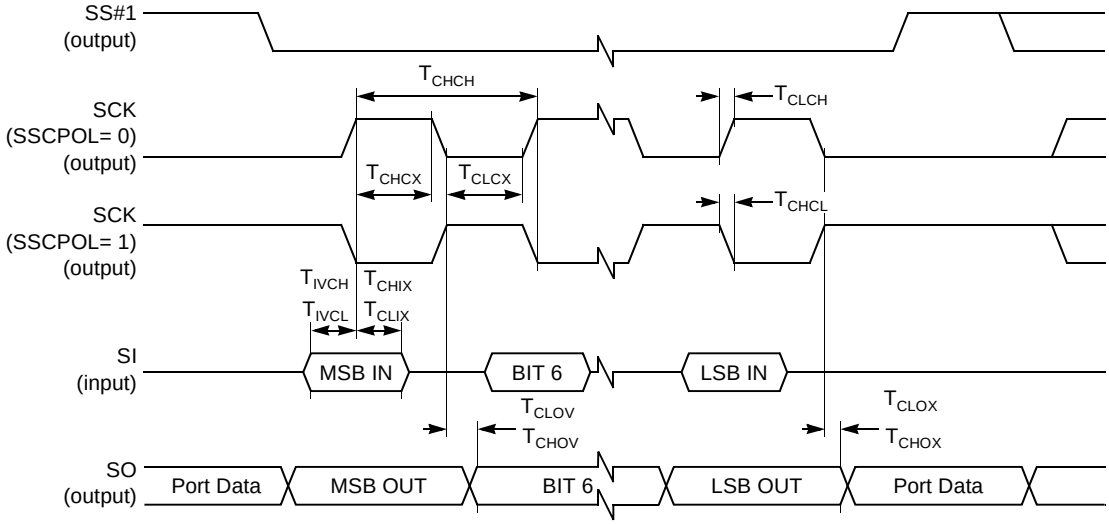
12.12.3 Waveforms

Figure 20. SPI Slave Waveforms (SSCPHA= 0)



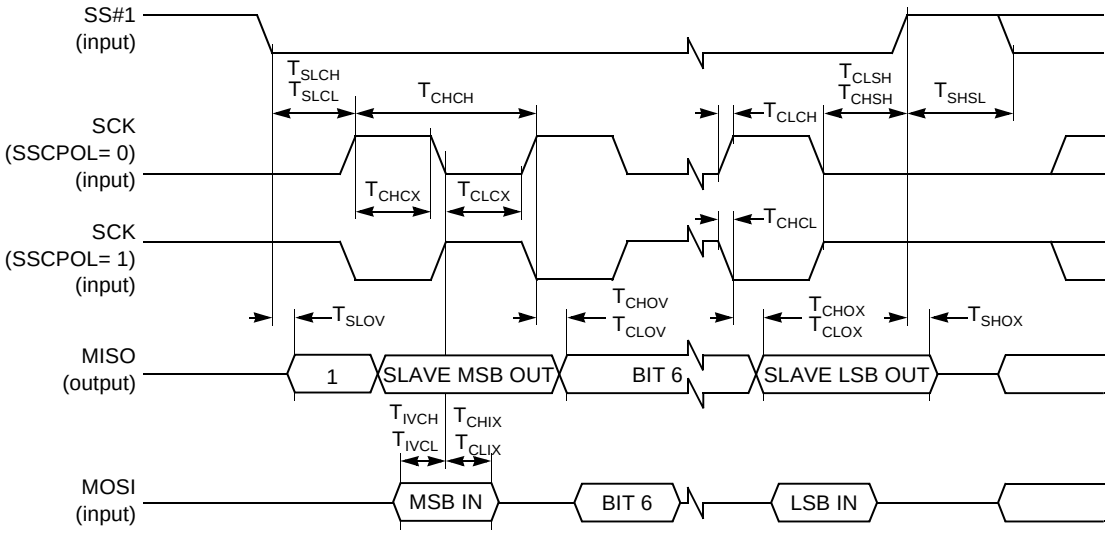
Note: Not Defined but generally the MSB of the character which has just been received.

Figure 21. SPI Slave Waveforms (SSCPHA= 1)



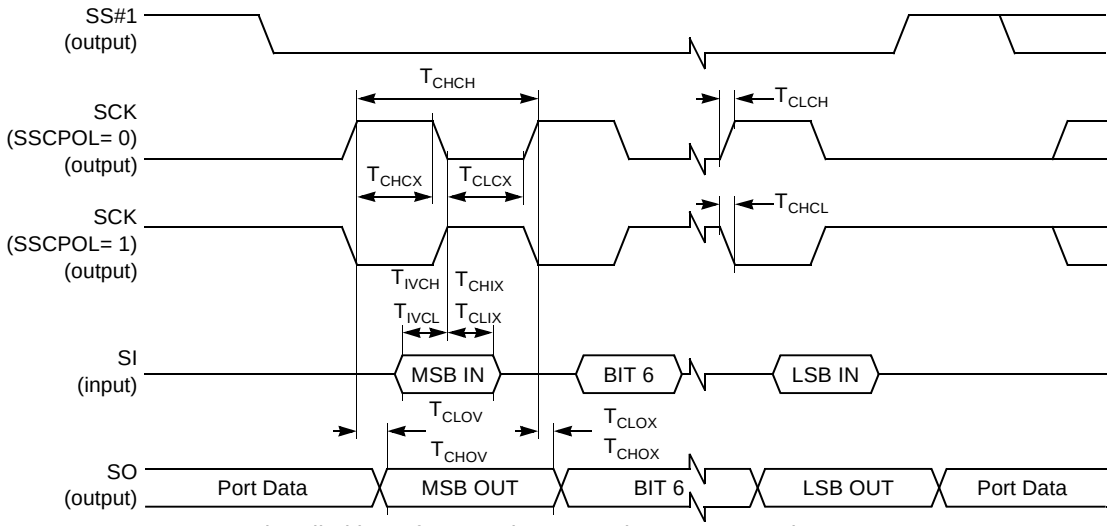
Note: Not Defined but generally the LSB of the character which has just been received.

Figure 22. SPI Master Waveforms (SSCPHA= 0)



Note: SS# handled by software using general purpose port pin.

Figure 23. SPI Master Waveforms (SSCPHA= 1)



Note: SS# handled by software using general purpose port pin.

12.13 AC Characteristics - 2-wire Interface

12.14.1 Timings

Table 52. 2-wire Interface AC Timing

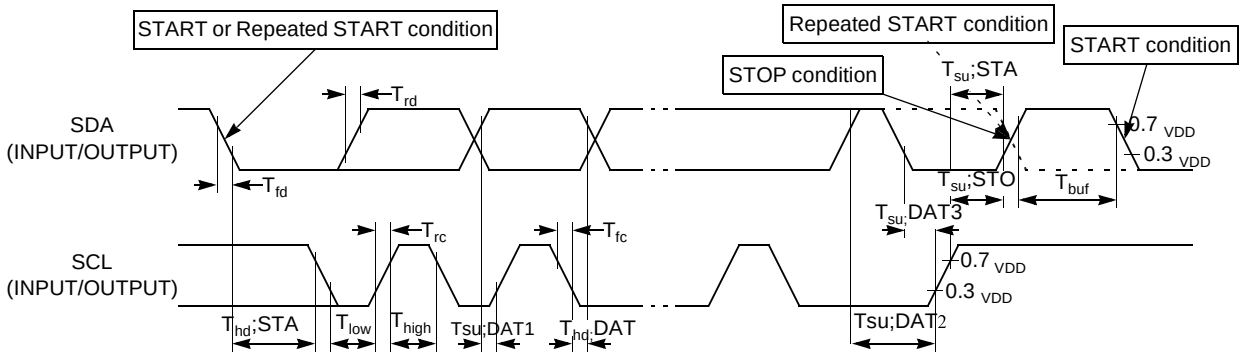
VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	INPUT Min Max	OUTPUT Min Max
T_{HD}; STA	Start condition hold time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{LOW}	SCL low time	$16 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{HIGH}	SCL high time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{RC}	SCL rise time	1 µs	-(2)
T_{FC}	SCL fall time	0.3 µs	0.3 µs(3)
T_{SU}; DAT1	Data set-up time	250 ns	$20 \cdot T_{CLCL}$(4)- T_{RD}
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns	1 µs(1)
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns	$8 \cdot T_{CLCL}$(4)
T_{HD}; DAT	Data hold time	0 ns	$8 \cdot T_{CLCL}$(4) - T_{FC}
T_{SU}; STA	Repeated START set-up time	$14 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{SU}; STO	STOP condition set-up time	$14 \cdot T_{CLCL}$(4)	4.0 µs(1)
T_{BUF}	Bus free time	$14 \cdot T_{CLCL}$(4)	4.7 µs(1)
T_{RD}	SDA rise time	1 µs	-(2)
T_{FD}	SDA fall time	0.3 µs	0.3 µs(3)

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than $3 \cdot T_{CLCL}$ will be filtered out. Maximum capacitance on bus-lines SDA and SCL= 400 pF.
4. T_{CLCL}= T_{OSC}= one oscillator clock period.

12.15.2 Waveforms

Figure 24. 2-wire Waveforms



12.16 AC Characteristics - MMC Interface

12.17.1 Definition of symbols

Table 53. MMC Interface Timing Symbol Definitions

Signals	
C	Clock
D	Data In
O	Data Out

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

12.18.2 Timings

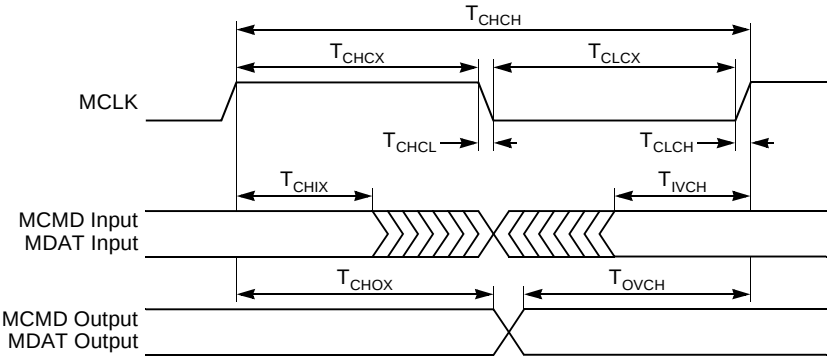
Table 54. MMC Interface AC timings

VDD= 2.7 to 3.3 V, TA= 0 to 70°C, CL ≤ 100pF (10 cards)

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period	50		ns
T_{CHCX}	Clock High Time	10		ns
T_{CLCX}	Clock Low Time	10		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{DVCH}	Input Data Valid to Clock High	3		ns
T_{CHDX}	Input Data Hold after Clock High	3		ns
T_{CHOX}	Output Data Hold after Clock High	5		ns
T_{OVCH}	Output Data Valid to Clock High	5		ns

12.19.3 Waveforms

Figure 25. MMC Input-Output Waveforms



12.20 AC Characteristics - Audio Interface

12.21.1 Definition of symbols

Table 55. Audio Interface Timing Symbol Definitions

Signals	
C	Clock
O	Data Out
S	Data Select

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

12.22.2 Timings

Table 56. Audio Interface AC timings

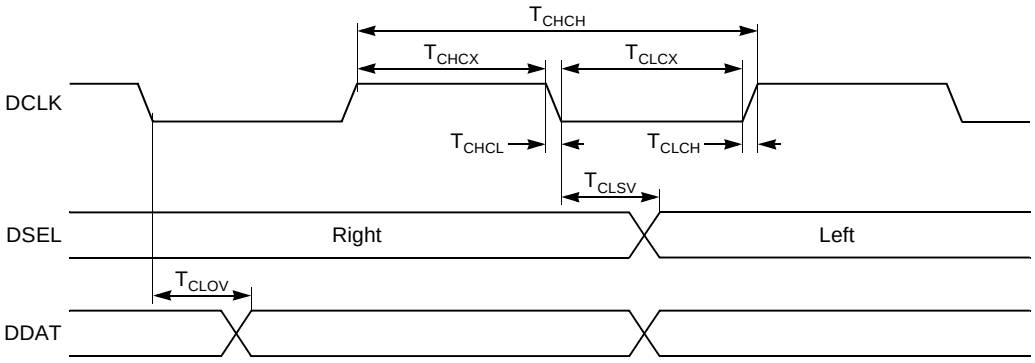
VDD= 2.7 to 3.3 V, TA= 0 to 70°C, CL≤ 30pF

Symbol	Parameter	Min	Max	Unit
T_{CHCH}	Clock Period		325.5(1)	ns
T_{CHCX}	Clock High Time	30		ns
T_{CLCX}	Clock Low Time	30		ns
T_{CLCH}	Clock Rise Time		10	ns
T_{CHCL}	Clock Fall Time		10	ns
T_{CLSV}	Clock Low to Select Valid		10	ns
T_{CLOV}	Clock Low to Data Valid		10	ns

Notes: 1. 32-bit format with Fs= 48 KHz.

12.23.3 Waveforms

Figure 26. Audio Interface Waveforms



12.24 AC Characteristics - Analog to Digital Converter

12.25.1 Definition of symbols

Table 57. Analog to Digital Converter Timing Symbol Definitions

Signals	
C	Clock
E	Enable (ADEN bit)
S	Start Conversion (ADSST bit)

Conditions	
H	High
L	Low

12.26.2 Characteristics

Table 58. Analog to Digital Converter AC Characteristics

VDD= 2.7 to 3.3 V, TA= 0 to 70°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	1.43		µs
T_{EHSH}	Start-up Time		4	µs
T_{SHSL}	Conversion Time		$11 \cdot T_{CLCL}$	µs
DLe	Differential non-linearity error[1, 2]		TBD	LSB
ILe	Integral non-linearity error[1, 3]		TBD	LSB
OSe	Offset error[1, 4]		TBD	LSB
Ge	Gain error[1, 5]		TBD	%

Notes:
1. AV_{DD}= AV_{REFP}= 3.0 V, AV_{SS}= AV_{REFN}= 0 V. ADC is monotonic with no missing code.
2. The differential non-linearity is the difference between the actual step width and the ideal step width (see Figure 28).
3. The integral non-linearity is the peak difference between the center of the actual step and the ideal transfer curve after appropriate adjustment of gain and offset errors (see Figure 28).
4. The offset error is the absolute difference between the straight line which fits the actual transfer curve (after removing of gain error), and the straight line which fits the ideal transfer curve (see Figure 28).
5. The gain error is the relative difference in percent between the straight line which fits the actual transfer curve (after removing of offset error), and the straight line which fits the ideal transfer curve (see Figure 28).

12.27.3 Waveforms

Figure 27. Analog to Digital Converter Internal Waveforms

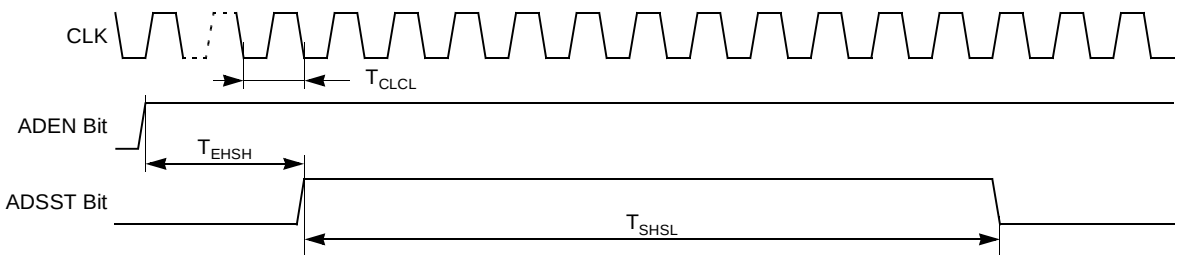
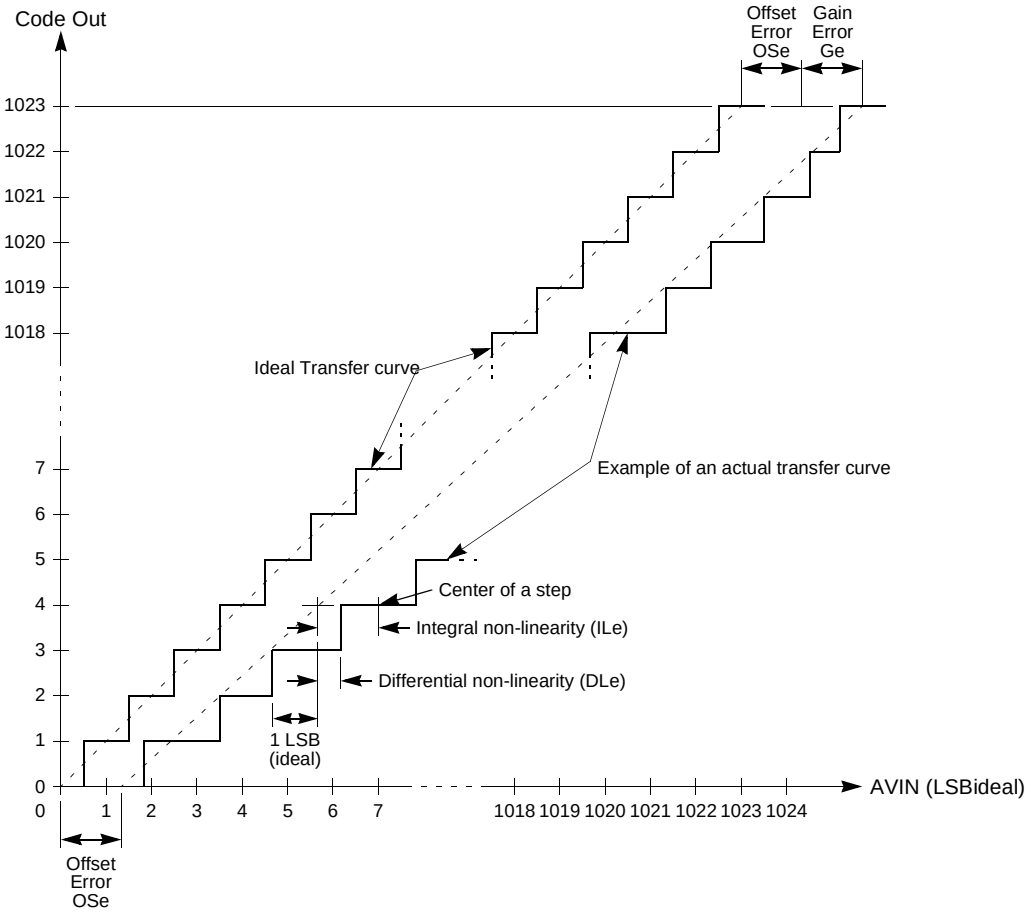


Figure 28. Analog to Digital Converter Characteristics



12.28 AC Characteristics - FLASH Memory

12.29.1 Definition of symbols

Table 59. FLASH Memory Timing Symbol Definitions

Signals	
S	ISP#
R	RST
B	FBUSY flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

12.30.2 Timings

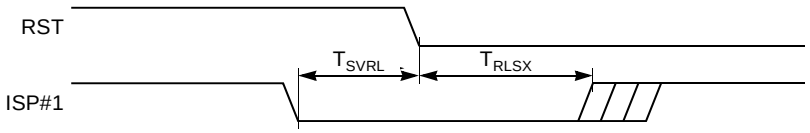
Table 60. FLASH Memory AC Timing

VDD= 2.7 to 3.3 V, TA= -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input ISP# Valid to RST Edge	50			ns
T_{RLSX}	Input ISP# Hold after RST Edge	50			ns
T_{BHBL}	FLASH Internal Busy (Programming) Time		10		ms

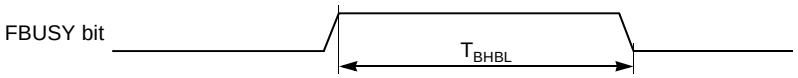
12.31.3 Waveforms

Figure 29. FLASH Memory - ISP Waveforms



Note: ISP# must be driven through a pull-down resistor (see Section 11.10, page 38).

Figure 30. FLASH Memory - Internal Busy Waveforms



12.32 AC Characteristics - External Clock Drive and Logic Level References

12.33.1 Definition of symbols

Table 61. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

12.34.2 Timings

Table 62. External Clock AC Timings

VDD= 2.7 to 3.3 V, TA= 0 to 70°C

Symbol	Parameter	Min	Max	Unit
T_{CLCL}	Clock Period	50		ns
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns
T_{CR}	Cyclic Ratio in X2 mode	40	60	%

12.35.3 Waveforms

Figure 31. External Clock Waveform

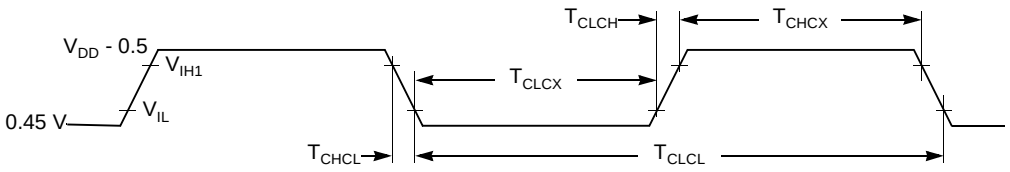
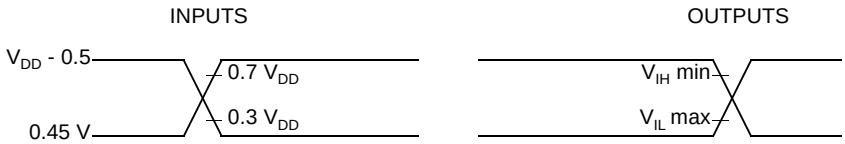


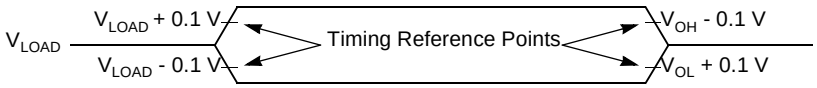
Figure 32. AC Testing Input/Output Waveforms



Note: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.

2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 33. Float Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH}= ±20 mA.

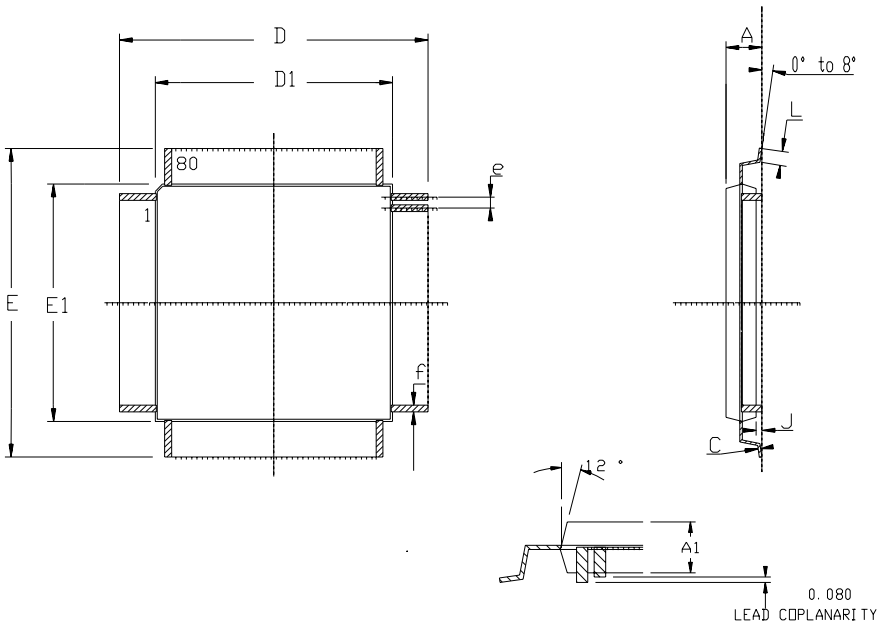
13. Packages

13.1 List of Packages

- TQFP80
- PLCC84

13.2 TQFP80 - Mechanical Outline

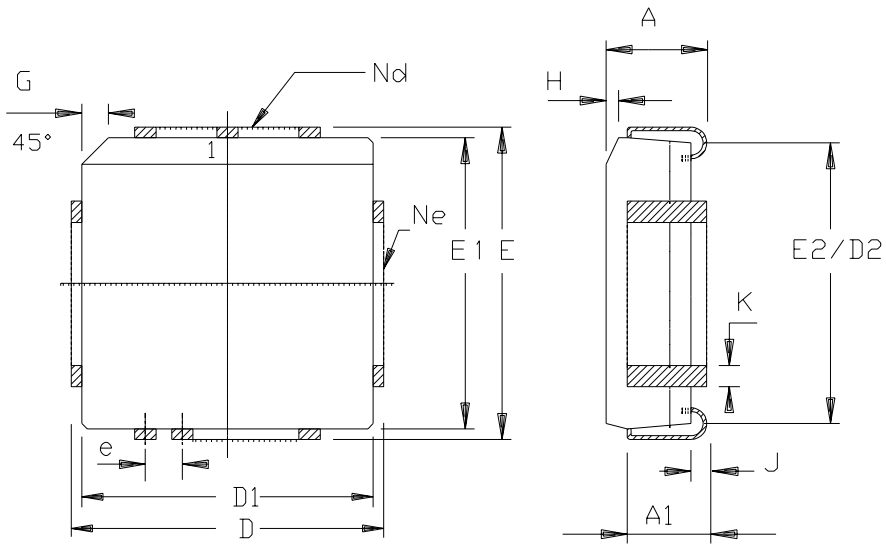
Figure 34. TQFP80 - Mechanical Outline



	MM		INCH	
	Min	Max	Min	Max
A	1.40	1.60	.055	.063
A1	1.35	1.45	.053	.057
C	0.17 BSC		.007 BSC	
D	15.80	16.20	.622	.638
D1	13.90	14.10	.547	.555
E	15.80	16.20	.622	.638
E1	13.90	14.10	.547	.555
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.65 BSC		.0256 BSC	
f	0.30 BSC		.012 BSC	

13.3 PLCC84 - Mechanical Outline

Figure 35. PLCC84 - Mechanical Outline



	MM		INCH	
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	30.10	30.35	1.185	1.195
D1	29.21	29.41	1.150	1.158
D2	27.69	28.70	1.090	1.130
E	30.10	30.35	1.185	1.195
E1	29.21	29.41	1.150	1.158
E2	27.69	28.70	1.090	1.130
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	21		21	
Ne	21		21	
PKG STD	00			

14. Ordering Information

Part-number	Memory size	Supply voltage	Temperature range	Max frequency	Package	Packing
T89C51SND1-ROTIL	64K Flash	3V	Industrial	40MHZ	TQFP80	Tray
T83C51SND1*-ROTIL	64K ROM	3V	Industrial	40MHZ	TQFP80	Tray

(*)check for availability.

PLCC84 package only available for development board.

Table of Contents

Atmel Sales Offices

France
3, Avenue du Centre
78054 St.-Quentin-en-Yvelines
Cedex
France
Tel: 33130 60 70 00
Fax: 33130 60 71 11

Germany
Erfurter Strasse 31
85386 Eching
Germany
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Fax: 49893 19 46 21

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45128 Essen
Germany
Tel: 492 012 47 30 0
Fax: 492 012 47 30 47

Theresienstrasse 2
74072 Heilbronn
Germany
Tel: 4971 3167 36 36
Fax: 4971 3167 31 63

Italy
Via Grosio, 10/8
20151 Milano
Italy
Tel: 390238037-1
Fax: 390238037-234

Spain
Principe de Vergara, 112
28002 Madrid
Spain
Tel: 3491564 51 81
Fax: 3491562 75 14

Sweden
Kavallerivaegen 24, Rissne
17402 Sundbyberg
Sweden
Tel: 468587 48 800
Fax: 468587 48 850

United Kingdom
Easthampstead Road
Bracknell, Berkshire RG12 1LX
United Kingdom
Tel: 441344707 300
Fax: 441344427 371

USA
2325 Orchard Parkway
San Jose
California 95131
USA-California
Tel: 1408441 0311
Fax: 1408436 4200

1465 Route 31, 5th Floor
Annandale
New Jersey 08801
USA-New Jersey
Tel: 1908848 5208
Fax: 1908848 5232

Hong Kong
77 Mody Rd., Tsimshatsui East,
Rm.1219
East Kowloon
Hong Kong
Tel: 85223789 789
Fax: 85223755 733

Korea
Ste.605,Singsong Bldg. Young-
deungpo-ku
150-010 Seoul
Korea
Tel: 8227851136
Fax: 8227851137

Singapore
25 Tampines Street 92
Singapore 528877
Rep. of Singapore
Tel: 65260 8223
Fax: 65787 9819

Taiwan
Wen Hwa 2 Road, Lin Kou
Hsiang
244 Taipei Hsien 244
Taiwan, R.O.C.
Tel: 88622609 5581
Fax: 88622600 2735

Japan
1-24-8 Shinkawa, Chuo-Ku
104-0033 Tokyo
Japan
Tel: 8133523 3551
Fax: 8133523 7581

Web site
http://www.atmel-wm.com