JAGUAR ET9000
486 WRITE BACK CACHE "AT" SINGLE CHIP

* **100% IBM PC/AT Compatible 1-Chip AT Solution**
* **1X clock source**
* **Designed to work at 16, 20, 25, 33, and 50MHz for 486SX/486DX system**
* **Flexible architecture to support 64KB 128KB, 256KB and 512KB Write Back Cache Subsystems**
* **Supports 2-1-1-1, 3-1-1-1, 2-2-2-2, and 3-2-2-2 cache Burst move-in cycles**
* **Built-in Comparator**
* **Support two programmable non-cacheable regions**
* **Up to 64MB DRAM memory support with Page Mode**
* **Mixing DRAM configurations - 256K, 1M and 4M devices**
* **Software Programmable DRAM Wait States**
* **Shadow RAM option**
* **Support 80487SX and Weitek 4167 Coprocessors**
* **Option for write protected, cacheable main and video BIOS**
* **Fast Reset and Gate A20 to optimize OS/2**
* **Asynchronous and Synchronous AT Bus Clock with programmable clock division options:CLK2 divided by 2, 3, 4, 5, 6, 8, 10**
* **Concurrent Refresh and slow refresh supported**
* **Support 8Kx8 and 8Kx9 Tag RAM**
* **Hardware and Software Turbo Clock Switching**
* **Support Local Bus**
* **1.0 Micron Low Power, High Speed CMOS Technology**
* **Less than 12 components plus memory to implement an 486 system**
* **184 Pin PQFP package**

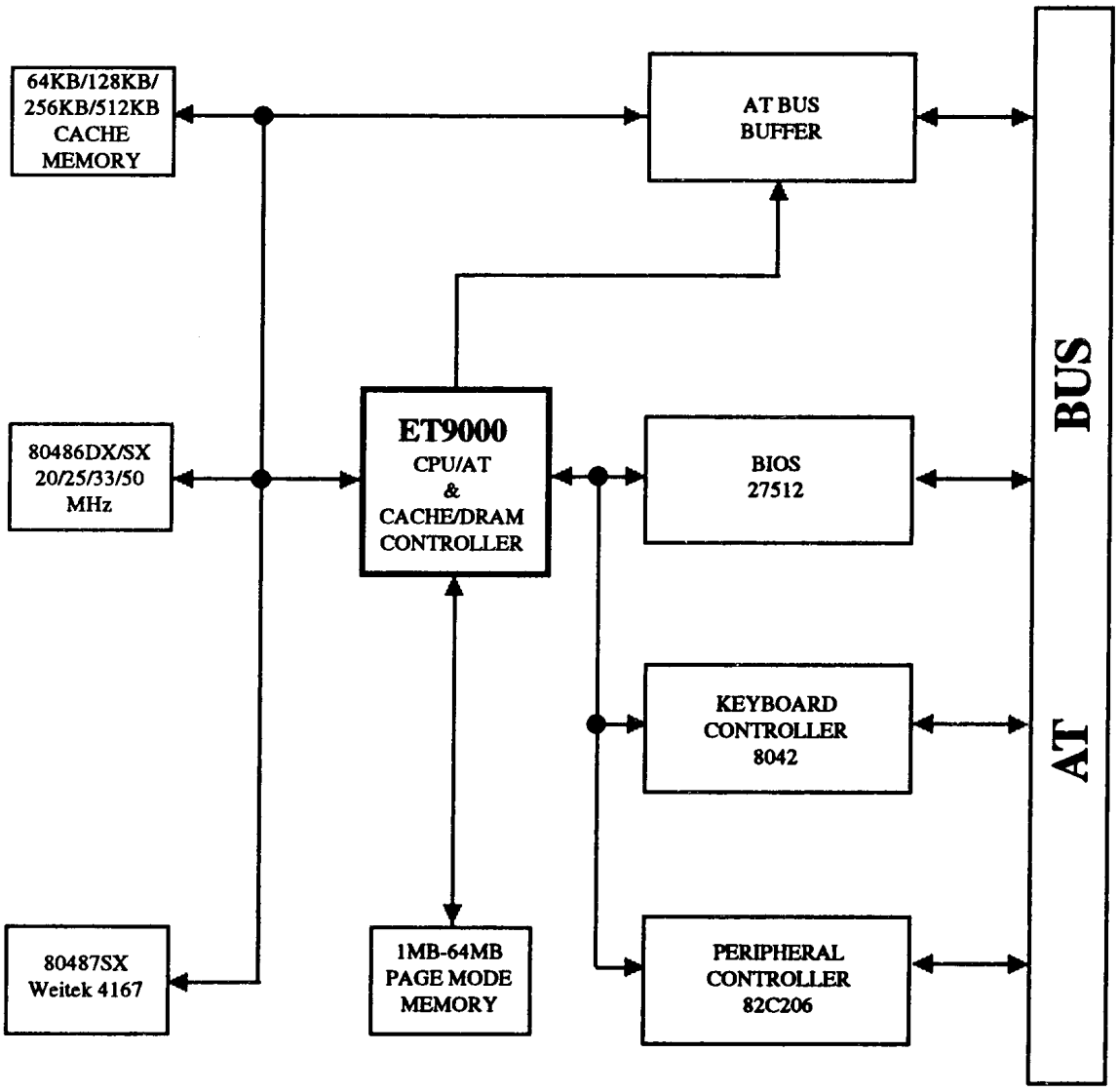
The JAGUAR single chip provides high integration and low cost solution for a 16, 20, 25, 33 and 50MHz 486/AT based system design. Its flexible architecture allows Direct Mapped Cache Implementation with 64KB/128KB/256KB/512KB Cache. The JAGUAR combined with 82C206 or compatible peripheral controller offers a 100% PC/AT compatible system using less than 12 components plus memory devices. The ET9000 is available in the 184-pin Plastic Quad Flatpack package. The 1.0u high speed, low power CMOS Technology allows for substantial stability when running at 33 and 50MHz.

The JAGUAR includes 486 CPU control, write-back cache control, Page Mode DRAM Control, a local DRAM control, AT Bus Control, Synchronous AT Bus Clock Generation, Clock Switching Logic, data bus conversion logic which performs the conversion necessary between the 8, 16 and 32-bit data paths. A Coprocessor Interface Logic to support Intel 487SX and Weitek 4167 are also included.

The JAGUAR ET9000 provides very flexible cache based system implementation and a Page Mode DRAM memory to improve performance during read miss cycles. System performance is further enhanced by allowing Refresh and CPU cache hit cycles to occur concurrently without holding the CPU during Refresh cycle.

The system cost is also minimized by allowing the use of slow SRAMs and DRAMs. The "Write Back" cache is implemented to minimize DRAM access time during write cycle.

The JAGUAR is designed to be 100% compatible with the IBM PC/AT. With its optimized Cache and DRAM design, enhanced features like Shadow RAM BIOS, and Concurrent Refresh; a high performance / low cost 486/ AT can be implemented.



Jaguar 486 System Block Diagram

ET9000 SINGLE CHIP CACHE SOLUTION

1.0 Overview

The JAGUAR provides an efficient cost/performance ratio as a high rate of integration in a 486 based, IBM PC/AT compatible system. It is implemented using 1.0u CMOS Technology and can run at 20MHz, 25MHz , 33MHz and 50MHz of CPU system clcok.

The ET9000 contains the Memory Controller, AT Bus Controller, CPU Controller, data buffer and clock circuitry. The Cache and DRAM Controllers are the main factors affecting the performance/cost ratio of the system. With the built-in direct mapped Cache Controller, a 0WS read cycle can be achieved during the read hit cycle. The penalty during the read miss cycle is compensated by a Page Mode DRAM Controller and the write cycle is greatly reduced by using the write back cache feature.

The ET9000 interfaces directly with the 80486 and implements the state machines required for controlling all bus accesses. The AT Bus Clock is synchronous with the processor clock and generated through a clock divider to insure that the system is 100% IBM compatible.

The Data Buffer performs all of the data buffering functions required for a 486 based PC/AT compatible personal computer system. The chip routes the data to and from the CPU Data Bus (CD Bus), the MAXD Bus and the ISA Bus (SD Bus) under CPU control.

2.0 Functional Description

The ET9000 has the following function modules:

* **Reset and Shudown Logic**
* **Clock Generation and Switching Logic**
* **CPU and AT Bus Control**
* **Master, DMA and Refresh Arbitration Logic**
* **Port B Register and NMI Logic**
* **OS/2 Optimization Logic**
* **Cache Controller Logic**
* **DRAM Controller Logic**
* **DMA and Master Access DRAM Logic**
* **Concurrent Refresh**
* **CPU Burst-Mode Control**
* **Shadow RAM**
* **Bus Interface between CD, MAXD and SD Buses**
* **Local Bus Interface**
* **Numerical Coprocessor Interface Logic**
* **14.318MHz and Counter Divided by 12**

2.1 Reset and Shutdown

The system contains four different resets: RESET1 is derived from the power-good signal at the power supply. Some power supplies have glitches on this signal, therefore, a de-dounce circuit is required before tying it to the RESET1 pin. RESET1 will generate both RESET3 (CPU Reset) and RESET4 (System Reset) for power-on initialization. This can only happen at system power-on. RESET2 is generated from the Jaguar; it triggers RESET3 to reset the CPU either to perform a shutdown or to activate a software reset. It can also be generated by programming the internal register. RESET3 is activated for power-on, shutdown and for changing the CPU from protect mode back to real mode. RESET4 is activated when the entire system is reset.

2.2 Clock Generation

The ET9000 uses a single oscillator to generate the CPU and AT Bus clocks. The oscillator input should be the same speed of the CPU. Depending upon the oscillator's frequency, the AT Bus Clock is divided between 2, 3, 4, 6 and 8. When the CPU is in normal mode, it runs at the same frequency as the AT Bus. For example: a 33MHz system will require an 33MHz Oscillator input. This 33MHz clock is divided by 4 to make it a 8.25MHz clock. A 8.25MHz clock will be used for AT Bus peripherals.

2.3 CPU and AT Bus Control

The CPU starts a cycle by asserting ADS- if the M/IO-, D/C- and W/R- signals plus address code turn out to be a internal local memory, LOCRAM- will assert LOW and the memory cycle begins. Otherwise, an AT Bus cycle will begin. ROM cycle is considered to be an AT Bus cycle because it is fixed at 8MHz and does not vary in relation to the CPU's speed. Therefore, a 200 nanosecond access time ROM will be sufficient. Shadow RAM is supported to increase the performance. Since the CPU is running at its maximum speed, and the AT Bus is running at 8MHz, synchronization is required. A DRAM
does not need this handshaking because it is running at the same frequency as the CPU, thus, everything is synchronized. For the AT Bus cycle, ALE is where the AT Bus starts and the synchronized CPU ready is where it ends. This synchronization overhead can be significant when the AT Bus cycle is continuously accessed. The ET9000 synchronizes ALE with an option by switching the phase of the AT clock, not the signal itself, therefore, increasing the speed.

2.4 Master, DMA and Refresh

The Master Device uses the same pin as DMA for bus arbitration, and Refresh operates from a different pin so that it is easy to identify. The Master Device or DMA can be identified by the signals AEN8- and AEN16-. When either one is asserted LOW, it is a DMA cycle. The 82C9000 supports both AT and Concurrent Refresh. No hold signal is sent back to the CPU in Concurrent Refresh. The AT Bus needs the full time to refresh as DRAMs do not need as much time. The ET9000 keeps track of when CPU to start its next instruction parallel to AT Bus Refresh. If the CPU needs to access the AT Bus, it must wait until refresh is completed.

2.5 Port B and NMI

A parity error detected will cause ET9000 to generate NMI to the CPU. NMI can also be generated through software. The ET9000 provides access to the Port B register defined for a PC/AT. The chart below illustrates bit definition:

Bit Definition Chart

Address	Bits	Function	Description
61H	7	Read Only	System Memory Parity Check
	6	Read Only	IO Channel Check
	5	Read Only	Timer 2 Output
	4	Read Only	Refresh Detection
	3	Read/Write	0: Enable IO Channel Check 1: Disable IO Channel Check
	2	Read/Write	0: Enable System Memory Parity Check 1: Disable System Memory Parity Check
	1	Read/Write	Speaker Data
	0	Read/Write	Timer 2 Gate

2.6 OS/2 Optimization

When running OS/2, 8742 needs to be programmed to activate the signal GATE A20 before entering Protected Mode. When it returns from the Protected Mode, some types of software use RESET2 by programming 8742 again. The Keyboard controller is a very slow device. Thus, the system is slowed down dramatically. 82C9000 supports the fast Gate A20 and fast Reset to speed up performance.

2.7 Cache Control Logic

2.7.1 Introduction

The ET9000 has a Direct Mapped Cache Controller inside to support a "0" wait state 80486 Microprocessor. It stores a copy of frequently accessed data/code from main memory in a "0" wait local Cache RAM. With this Cache Controller almost all critical paths are relocated to relatively small Cache RAMs (SRAM) and DRAM timing is no longer a major issue. Total cost is also decreased as expensive high speed DRAMs are not required.

Cache design issues: Our goal is to design a cache which has the best cost/performance ratio in the industry, therefore, availability, price, stability and manufacturability are all integral parts of our design. A Direct Mapped write back cache is implemented in ET9000 The following sections will be discussed in detail.

2.7.2 Write Back Cache

The ET9000 has a internal comparator to compare TAG address and current CPU address. If it is a CACHE READ HIT cycle, the data will be driven by SRAM. If it is a CACHE READ MISS cycle, ET9000 will further check if DIRTY BIT is "1" or "0". If DIRTY BIT =1, ET9000 will first write the DIRTY SRAM data back to DRAM in 4 consccutive DRAM write cycles (line size=4 DWORD), and then move in new data from DRAM also in 4 consccutive DRAM read cycles. If DIRTY BIT=0, no move out cycles, only move in cycles will be performed.

When CACHE WRITE HIT cycle happens, the data are written into SRAM, also DIRTY BIT will be set to 1, no data will be written to DRAM. If it is a WRITE MISS, data will bypass SRAM and written into DRAM directly.

The following table shows the TAG RAM / DATA RAM sizes supported by ET9000:

CPU SPEED	TAG RAM SPEED	DATA RAM SPEED
486-20MHz	25ns	30ns
486-25MHz	25ns	25ns
486-33MHz	20ns	25ns
486-50MHz	20ns	20ns
External TAG RAM/DATA RAM Speed for 486 system		

CACHE Size	TAG Field Address	TAG RAM Size	CACHE RAM Address	CACHE Size	Cacheable Range
64K	A23-A16	4KX8	A15-A4	8Kx8x8	16M
128K	A24-A17	8KX8	A16-A4	32Kx8x4	32M
256K	A25-A18	16KX8	A17-A4	32Kx8x8	64M
512K	A25-A19	32KX8	A18-A4	128Kx8x4	64M
TAG RAM / DATA RAM Size for 486 system					

2.8 DRAM Control Logic

2.8.1 Introduction

The DRAM Control Logic is designed and optimized for the 486 CPU. Unlike most systems with an external Cache Controller, the ET9000 DRAM Controller is tightly coupled with the on-chip Cache Controller. When CPU Address becomes available, both controllers operate in paralled. At the time when the Cache Controller discovers it is a read miss or write cycle, the DRAM Controller is ready to generate RAS (Page Miss) or CAS (Page Hit) right away!

To optimize memory performance, the DRAM Controller has built-in support for Page Mode. When more than one bank of the DRAM is installed, the size of the page will increase linearly to increase the hit rate.

The DRAM Controller supports up to 4 banks of DRAM with sizes up to 64MByte and three types of DRAM are supported: 256K, 1M and 4M.

2.8.2 DRAM Sizes/Bank Configuration

The local DRAM System can be configured into 1 to 4 banks of DRAM. There is no limitation on the configuration of DRAM as long as no previous banks are empty. The DRAM Banks have to be filled in the following order. Bank0 -> Bank1 -> Bank2 -> Bank3. (See Table A on page 6)

2.8.3 DRAM Speed and Wait State

In order to work with different types of DRAM speed, ET9000 supports wait state for memory read cycle as well as memory write cycle. For read cycle, a configuration of 1 to 4 wait state is available: R1WT, R2WT, R3WT, and R4WT. For write cycle, the ET9000 supports: W0WT, W1WT and W2WT. (See Table B on page 7.)

The ET9000 has a built-in Cache Controller, and the hit rate is fairly high (99% for a 64K SRAM). Most of the memory read cycle will be hit, and the data is accessed from the SRAM instead of the DRAM. Hence the DRAM wait state penalty becomes insignificant.

TABLE A

Bank 0	Bank 1	Bank 2	Bank3	Total Memory Size	Page Size
256K	NONE	NONE	NONE	1M	2K
256K	256K	NONE	NONE	2M	4K
256K	256K	256K	NONE	3M	6K
256K	256K	256K	256K	4M	8K
1M	256K	NONE	NONE	5M	6K
256K	256K	1M	NONE	6M	8K
256K	256K	256K	1M	7M	10K
1M	1M	NONE	NONE	8M	8K
1M	1M	256K	NONE	9M	10K
256K	256K	1M	1M	10M	12K
1M	1M	1M	NONE	12M	12K
1M	1M	1M	256K	13M	14K
1M	1M	1M	1M	16M	16K
1M	4M	NONE	NONE	20M	12K
1M	1M	4M	NONE	24M	16K
1M	1M	1M	4M	28M	20K
4M	4M	NONE	NONE	32M	16K
4M	4M	1M	NONE	36M	20K
256K	1M	4M	4M	37M	22K
1M	1M	4M	4M	40M	24K
4M	4M	4M	NONE	48M	24K
256K	4M	4M	4M	49M	26K
1M	4M	4M	4M	52M	28K
4M	4M	4M	4M	64M	32K

Table A : Partial Possible DRAM Configuration

2.8.4 Row and Column Address

Table C, below, illustrates row/column address for different types of DRAM. For easy debugging, all row and column addresses are continuous, no scramble is needed.

2.9 DMA and Master Access DRAM Logic

The DMA Master can access the local DRAM through ET9000. When HLDA1 and SMEMR/SMEMW become active, a memory read/write cycle will be performed. To guarantee cache coherence, the SRAM data will be updated when a memory write hit occurs.

2.10 Concurrent Refresh

In order to alleviate refresh penalty, ET9000 supports "Concurrent Refresh" in addition to normal PC Refresh. Traditional PC Refresh will send a HOLD to stop the CPU, then, after receiving HLDA from the CPU, refresh will begin. Concurrent Refresh can execute the refresh cycle concurrently with the CPU as long as there is no DRAM conflict. (i.e. we can enhance performance by allowing refresh to work on the DRAM and the CPU to work on the Cache RAM at the same time.) To quiet refresh noise on the Motherboard, all RAS are staggered during refresh cycle.

2.11 CPU Burst Mode Control

The JAGUAR single chip fully supports 486 burst cycles. The ET9000 cache and DRAM controllers insure that data is burst into the CPU whenever the 486 requests a burst line fill. The secondary cache provides data on read-hits and the DRAM supplies the data during cache read-misses. DRAM burst mode is supported only with the 486 CPU and when the cache is disabled.

For the cache read-hit cycle, BRDY- (Burst Ready) is asserted at the middle of the first T2 state when a 2-1-1-1 (zero wait state) cache burst cycle is chosen, otherwise, it is asserted at the middle of the second T2 state when one wait state is required. If a read-miss occurs, the DRAM data is first written into cache memory, then it is burst from the cache to the 486 CPU. BRDY- is asserted after cache memory is updated for cache read-misses. Once asserted, BRDY- stays active unitl BLAST- (Burst Last) is detected. BRDY- is never active during DMA or MASTER cycles.

The ET9000 contains separate burst counters to support DRAM and External Cache Burst cycles. The DRAM burst counter performs the cache read-miss line fill (DRAM to external cache) and the cache burst counter supports the 486 burst line fill (external cache to the 486 CPU). The burst order of the cache burst counter exactly matches the double-word order expected by the CPU, 0-1-2-3. The DRAM burst counter is used for cache read-miss cycles and dirty line fill write operations.

CPU SPEED	DRAM SPEED	DRAM WAIT STATE
486-20MHz	80NS (CMOS)	(W0WS, R2WS)
486-25MHz	80NS (CMOS)	(W0WS, R2WS)
486-33MHz	80NS (CMOS)	(W0WS, R3WS)
486-50MHz	80NS (CMOS)	(W1WS, R4WS)

Table B: Wait States / DRAM Speeds for 486 systems

DRAM Configuration	Row Address	Column Address
256K Page Mode	(A19-A11)	(A10-A2)
1M Page Mode	(A21-A12)	(A11-A2)
4M Page Mode	(A23-A13)	(A12-A2)

Table C : Row / Column Address for Different Types of DRAM

2.12 Shadow RAM

For those BIOS Call Intensive Application Softwares, it is not efficient to run BIOS Call in low speed ROM. Moving all ROM contents to a high speed DRAM will largely improve the performance of a BIOS Call intensive program.

ET9000 allows all Motherboard ROM and Adapter Card ROM to be shadowed on the Motherboard DRAM as long as they are resident in (C0000-CFFFF), (D0000-DFFFF), (E0000-EFFFF), or (F0000-FFFFF) range. If the Adapter ROM is on the Motherboard, it can still be shadowed.

2.13 Bus Interface Between CD, MD, MAXD and SD Bus

The ET9000 Data Buffer provides interface between three distinct buses: the CD Bus,MAXD Bus and the SD Bus. The CD Bus (CD<31:0>) is the CPU Data Bus. The Memory Data Bus connects to the CD BUS. The MAXD Bus (MAXD<15:0>) are Memory Address Bus and 16-bit bus for on board I/O devices which use the XD bus. Off board I/O devices would situate on the SD bus (SD<15:0>).

The data conversion can be done on either an 8-bit, 16 bit or 32-bit wide bus. The bus size 16(BS16-) feature is supported allowing the 486 to directly connect to 32-bit and 16-bit data buses. The 486 will make adjustments for correct transfer of the upper bytes using only physical data signal, D<15:0>.

2.14 Local Bus Interface

The ET9000 allows select peripheral devices to share the "local bus" with the CPU and numerics coprocessor. The performance of these devices (which may include video sub-system, hard disk adapters, LAN and other PC/AT controllers) will dramatically increase when allowed to operate in the high-speed environment. These devices are responsible for their own address and bus cycle decode and must be able to operate compatibly at the elevated frequencies required for operation on the local CPU bus.

2.15 Numerical Coprocessor Interface Logic

The ET9000 Data Buffer supports the floating point errors handled with the i486 microprocessor.

The trailing edge of NPIRQ will trigger flip-flop to generate the IRQ signal which will be ORed with WTINTR and become interrupt level 13 (IRQ13-). After interrupt is asserted, the interrupt service routine handles the error and then clears the interrupt by executing a dummy write to I/O port F0h. The IGNNE-signal is also activated by this. It allows non-control instructions to be executed prior to the time the FERR-signal is reset by the i486. This is implemented for AT compatibility.

2.17 14.318MHz and Divided by 12 Counter

The ET9000 Data Buffer also provides the logic to generate a 14.318MHz OSC signal and a divided by 12 OSC119 signal which are used on the system board.

3.0 Configuration Registers

The ET9000 has internal registers used for system configuration and internal control. These areas are accessed through IO Ports 22H and 23H. Each access to an internal register is accomplished by first, writing its index into Port 22H. This index is then used to gate the appropriate internal register and the control data is accessed through Port 23H.

There are eight configuration registers in ET9000. The definitions of these registers are as follows:

TABLE D

System Configuration Register

Index	Bits	Values and Functions	Default
10H	2:0	AT BUS Clock Select 000: ATCLK= CLK2IN/10 001: ATCLK= CLK2IN/8 010: ATCLK= CLK2IN/6 011: ATCLK= CLK2IN/5 100: ATCLK= CLK2IN/4 110: Reserved 111: ATCLK = External ATCLK/2	111
	3	Slow refresh at 95us 0: Disable slow refresh 1: Enable slow refresh	0
	4	Refresh Selection 0: AT Type Refresh 1: Concurrent Refresh	0
	5	Reserved	0
	6	RAM at A0000H to BFFFFH 0: AT Bus Cycle 1: Local Bus Cycle	0
	7	Reserved	0

TABLE E

CACHE Configuration and Non-Cacheable Block Size Register

Index	Bits	Values and Functions	Default
11H	0	0: Set valid# output to 1 to flush cache 1: Set valid# output to 0	0
	1	0: Disable slow refresh 1: Enable slow refresh	0
	2	SRAM Banks 0: 1 Bank SRAM installed 1: 2 Banks SRAM installed	0
	4:3	SRAM Size 00: 32K (386 mode), 512K (486 mode) 01: 64K 10: 128K 11: 256K	00
	7:5	Non-Cacheable Block Size 000: Disabled 001: 512KB 010: 1MB 011: 2MB 100: 3MB 101: 8MB 110: 16MB 111: 32MB	000

TABLE F

Non-Cacheable Block Address Register

Index	Bits	Values and Functions	Default
12H	0	WriteBack Cache Move Out Wait State	0
	7:1	Non-Cacheable Address A25 to A19	0

TABLE G

DRAM Bank and Type Configuration Register

Index	Bits	Values and Functions	Default
13H	1:0	Bank0 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	01
	3:2	Bank1 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00
	5:4	Bank2 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00
	7:6	Bank3 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00

TABLE H

DRAM Configuration Register

Index	Bits	Values and Functions	Default
14H	1:0	Write Cycle Wait States 00: 0WS 01: 1WS 10: 2WS 11: Reserved	10
	4:2	Read Cycle Wait States 000: 0WS 001: 1WS 010: 2WS 011: 3WS 100: 4WS 101: Reserved 110: Reserved 111: Reserved	100
	5	0: Disable ROMCS at memory range C0000-DFFFF 1: Enable ROMCS at memory range C0000-DFFFF (NOTE: if C0000-DFFFF is enabled for ROMCS, then memory address cannot be SHADOWED)	0
	6	0: Enable on-board memory range 512K-640K 1: Disable on-board memory range 512K-640K	0
	7	0: Enable on-board memory range 15M-16M 1: Disable on-board memory range 15M-16M	0

TABLE I

Shadow RAM Configuration Register

Index	Bits	Values and Functions	Default
15H	0	RAM at C0000H-CFFFFH 0: Read/Write 1: Read Only	0
	1	Access ROM/RAM at C0000H-CFFFFH 0: Accessed on-board ROM, ie AT bus cycle 1: Access Shadow RAM C0000H-CFFFFH enabled	0
	2	RAM AT D0000H-DFFFFH 0: Read/Write 1: Read Only	0
	3	Access ROM/RAM at D0000H-DFFFFH 0: Accessed on-board ROM, ie AT bus cycle 1: Access Shadow RAM D0000H-DFFFFH enabled	0
	4	RAM AT E0000H-EFFFFH 0: Read/Write 1: Read Only	0
	5	Access ROM/RAM at E0000H-EFFFFH 0: Accessed on-board ROM, ie AT bus cycle 1: Access Shadow RAM E0000H-EFFFFH enabled	0
	6	Access ROM/RAM at F0000H-FFFFFH (System BIOS ROM) 0: Read from ROM, Write to RAM 1: Read from Shadow RAM, Write will be protected (will not be written into RAM)	0
	7	Shadow RAM at C0000H-FFFFFH 0: Non Cacheable 1: Cacheable and Cache write protected	0

TABLE J

TAG RAM and SRAM Configuration Register

Index	Bits	Values and Functions	Default
16H	0	Tag RAM 0: when use 8Kx8 Tag RAM 1: when use 8Kx9 Tag RAM	0
	1	Tag Field 0: 8 bit tag field 1: 7 bit tag field	0
	3:2	486 Burst Cycle 00: 2-1-1-1 01: 3-1-1-1 10: 2-2-2-2 11: 3-2-2-2	01
	5:4	SRAM Write Wait State 00: 2 WS 01: 1WS 10: 0WS 11: reserved	00
	6	Reserved	0
	7	0: 2 Banks of DRAM 1: 4 Banks of DRAM	0

TABLE K

System configuration Register II

Index	Bits	Values and Functions	Default
17H	3:0	Reserved	0000
	4	Wait for HALT after KBDRST 0: Do not wait for HALT 1: Wait for HALT	0
	5	Fast RESET delay 0: Do not use delay 1: Wait for 2us delay	0
	7:6	MISC input pin definition 00: Turbo/Non-Turbo 01: Local Device Decode 10: Suspend mode 11: Reserved	00

ET9000 Pin Description

Pin No.	Pin Type	Symbol	Description
Clocks			
27	I	CLK2IN	CLOCK2 INPUT to avoid clockskew due to the chip dely. This way, each chip sees the clock at the same time.
28	I	EXACLK	AT BUS CLOCK input from crystal.
29	I	ECLK2IN	Oscillator input. The frequency should be the same as the CPU's clock
183	O	OSC119	14.318MHz divided by 12 for utilization by peripheral chips.
152	O	BUSCLK	8MHz AT BUS CLOCK. Needs to be buffered.
26	I	CX1	14.318MHz input from crystal.
25	O	CX2	14.318MHz output to crystal.
Reset Contrl			
133	I	PWRGD	Power On Reset.
34	O	RESET3	CPU Reset. Assereted by either power on initializing the CPU or bringing the CPU back to real mode from the protected mode.
136	O	RESET4	System Reset. Assereted during Power On to reset the whole system.
CPU Control			
48	I	ADS-	An input from the CPU indicates address and cycle definitions are valid. It is an active low.
32	I	MIO-	CPU Status. A high means this is a memory cycle and low indicates an IO cycle.
31	I	WR-	CPU Status. A high means this is a write cycle and a low indicates a read cycle.
33	I	DC-	CPU status. A HIGH means it is a data access cycle, and a Low indicates code access.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
CPU Control (Continued)			
68	I/O	RDY-	This pin generates the CPU READY signal to alert the CPU that the cycle has finished with the exception of the coprocessor cycle. The MATH co-processor will generate its own CPU ready, thus, RDY- acts as an input in this case.
42, 41 40, 39	I/O	BE<3:0>-	INPUT BYTE ENABLE signals from the CPU. They become output signals at the DMA cycles to reflect XA0, XA1 and XBHE-.
30	I	PHLDA	When active, it indicates the processor has released the bus in response to HOLD request. This signal is connected to the processor HLDA signal.
38	O	NMI	Non-Maskable Interrupt to the CPU.
36	O	HOLD	An active HIGH used to request the CPU to relinquish the bus to DMA, Master or Refresh cycle.
77-75, 67-65, 89-87, 140, 96-94, 91 97	I I I I I I I	A<7:5> A<4:2> A<19:17> CAS3-/A25 A<24:22> A21 A31	CPU Address.
86-78,- 90	I/O I/O	A<16:8> A20	CPU Address. Output signals during DMA and MASTER MODE.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Cache Control			
50	O	CRD0-	Cache Read for Bank0 of the SRAMs. It should tie to the Cache RAMs output enable. It is qualified with A2=0 internally when two bank SRAM is selected, and not qualified with A2=0 if only one bank SRAM is selected.
49	O	CDR1-	Cache Read for Bank1 of the SRAMs. It should tie to the Cache RAM's output enable. It is internally qualified with A2=1 when two bank SRAM is selected.
52	O	CWE0-	Cache Write for Bank0. It should tie to the Cache RAM's write enable. It is qualified with A2=0 internally when two bank SRAM is selected, and not qualified with A2=0 if only one bank SRAM is selected.
51	O	CWE1-	Cache Write for Bank1. It should tie to the second bank of the Cache RAM's write enable. It is internally qualified with A2=1 when two bank SRAM is selected.
74	O	CCA2	Toggle Address 2. Address A2 needs to be toggled to support the move in 8 Byte and 16Byte.
73	O	CCA3	Toggle Address 3. Address A3 needs to be stoggled to support the move in 16Byte.
56	I/O	DIRTY	CACHE DIRTY bit. OUTPUT during WRITE Hit cycle. INPUT for all other cases.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Cache Control (Continued)			
53	O	TOEDWS	Control signal to write DIRYT bit into SRAMs.
57-64	I	TAG<7:0>	Cache TAG RAM address input.
54	O	TAGWT-	TAG RAM Write Command. Active LOW.
35	O	BSY6KEN-	Active low signal to indicate that the current cycle is cacheable.
72	O	Q6BRDY-	Active low signal. Burst Ready to 486
44	I	BS7BLST-	BLAST- input from 486. Indicates that the burst cycle is complete after the next BRDY- is returned. Active low.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
DRAM Control			
151	O	DWROMS-	Dual functional pin. It is data write enable for DRAM write cycle and ROM chip select for ROM cycle.
143	O	CAS0-	Column Address Strobe for DRAM bank 0.
142	O	CAS1-	Column Address Strobe for DRAM bank 1.
141	O	CAS2-	Column Address Strobe for DRAM bank 2. By combining with BE<3:0> each byte can be controlled individually
140	O	CAS3-	Column Address Strobe for DRAM bank 3. By combining with BE<3:0> each byte can be controlled individually
145-144, 143, 142	O	RAS<1:0>- RAS2-/CAS0- RAS3-/CAS1-	Row Address Strobe 0 to 3 corresponding to bank 0 to 3. It should be buffered before tying to the DRAMs. These are active low signals.
16-14, 12-5	O	MAXD<10:8> MAXD<7:0>	DRAM Memory Address. They should be buffered before tying to the DRAMs and also used as refresh address output during REF cycle.
Data Bus Control			
98-114, 117-131,	I/O	CD<31:15> CD<14:0>	Regular Mode: Connect to the CPU Data Bus. CD<31:0> would be driven during CPU read and DMA write memory cycle Bypass Mode: Connect to CPU Data and DRAM Data Bus. CD<31:0> will pass through transparent latch to parity generation and checking logic.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Data Bus Control (Continued)			
150-147	I/O	MP<3:0>	Memory Parity Bit 3 to 0. Output for CPU or DMA write to memory, and inputfor CPU or DMA read from memory. EVEN parity bit is generated on all writedata cycles. This information must bedriven back into MP<3:0> with thesame timing as read data to insure the correct parity check. MP3 refers to Byte3 Parity, MP2 refers to Byte2 Parity ans so on.
21-14, 12-5	I/O I/O	MAXD<15:8> MAXD<7:0>	ISA Data Bus Bits <15:0>
AT Control			
166	O	L1MCS-	Low 1 Meg Chip Select to generate SMEMR- and SMEMW- for the AT Bus command which is an indication that it is within the first 1 Meg address range. It is an active low signal.
164	I/O	XBHE-	Peripheral Byte High Enable. An active LOW signal which indicates that the data is on the upper byte. It is an output during the CPU and DMA cycle and an input during the master cycle.
171-170, 181	I/O	XA<1:0> XA20M	These signals are latched at address outputs during CPU cycles and inputs during DMA or Master cycles.
163	O	BALE	Bus Address Latch Enable. The trailing edge latches the valid address for the AT Slot.
156	I/O	MEMR-	AT Bus Memory Read. It is an output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
AT Control (Continued)			
157	I/O	MEMW-	AT Bus Memory Write. An output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.
154	I/O	IOR-	AT Bus IO Read. It is an output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.
155	I/O	IOW-	AT Bus IO Write. It is an output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.
158	I	0WS-	Zero Wait State. When LOW, the AT Bus will terminate its current cycle without additional wait state.
153	I/O	CHRDY	IO Channel Ready. When LOW, the AT Bus will insert wait states until this signal returns to HIGH.
165	I	MCS16-	16 Bit Memory Chip Select. When LOW, it is a 16 bit memory transfer from the AT Slot. When HIGH, an 8 bit memory transfer
160	I	IOCS16-	16 Bit IO Chip Select. When LOW, it is a 16 bit IO transfer. When HIGH, an 8 bit memory transfer.
135	I	IOCHCK-	An AT Bus error condition will cause an NMI to be generated.
167	O	SDEN-	Slot Data Enable. Enables the buffer that drives the data bus onto the slot an back.
178	O	INTA-	Interrupt Acknowledge. Asserted for CPU to read the interrupt vector from the MAXD Bus.
182	O	ACK-	An active LOW, tied to the C206 ACK - pin.
134	I/O	MISC	An active LOW signal indicating a local BUS cycle, not an AT cycle.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
AT Control (Continued)			
168	O	SDIR0-	System Data Bus Direction for the low byte. The data is moved from SD Bus to MD Bus when SDIR0- is LOW. The data is moved from MD Bus to SD Bus when SDIR0- is HIGH
169	O	SDIR1-	System Data Bus Direction for the high byte. The data is moved from SD Bus to MD Bus when SDIR1- is LOW. The data is moved from MD Bus to SD Bus when SDIR1- is HIGH
45	O	BS16-	A bus size of 16 caused the CPU to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a singale cycle. BS16- is an active LOW.
Refresh			
159	I/O	REF-	An output to indicate a refresh cycle. For Master Mode, it is an input from the Master Device to indicate a refresh cycle.
DMA Control			
177	I	DMAHRQ	HOLD REQUEST from DMA or other Bus Master for bus control.
172	I	AEN8-	Address Enable for 8 bit DMA transfer. An active LOW signal.
173	I	AEN16-	Address Enable for 16 bit DMA transfer. An active LOW signal.
176	O	HLDAOUT-	Indicates that the CPU has relinquished the bus to other masters or DMA.
4	I	MASTER-	When LOW, it indicates that a bus master other than the CPU or DMA is owning the bus.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
DMA Control (Continued)			
175	I	ADSTB8	Address Strobe for 8 bit DMA transfer.
174	I	ADSTB16	Address Strobe for 16 bit DMA transfer.
Decodes			
137	O	8042CS-	8742 Keyboard Controller Chip Select. An active LOW signal.
180	O	RTCAS-	Real Time Clock Address Strobe. It should tie to the 82C206. The trailing edge latches the address onto the MAXD Bus.
Floating Point Interface			
43	I	ER7FERR-	Tied to the 486 FERR- pin.
37	O	ER36IGN-	Connected to the 486 IGNNE- pin.
71	I	RDYIN-	This pin generates the NPU READY signal to alert the NPU that the cycle has finished.
2	O	IRQ387	Generated when a FERR- is asserted, or WTINER is asserrted.
22	O	NPRST	Connected to the RESET pin of WEITEK 4167, NPRST is asserted when either RESET3 is asserted or asynchronous software reset is initiated.

ET9000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Miscellaneous			
179	I	TMOUT2	Output from the 8254 timer located inside the 82C206.
3	O	TMGATE	TIMER GATE 2 enables the counter two of the 8254. Used for tone generation for the speaker.
132	O	SPKOUT	Speaker data used to drive the speaker. Buffer required.
134	I	MISC	This pin will connect to a hardwired clock switching control signal, if it exists. If bit 2 of register 10 is programmed to 0 then a high on this signal will keep the system in high speed mode. Otherwise, the system will enter low speed mode if this pin is low. The system will stay in low speed mode and does not count on this signal at all if bit 2 of register 10 is programmed to 1. Tied to high if not used.
Power			
23, 46 69, 92 115, 138 161, 184	I	VDD	Power Supply
Ground			
1, 13 24, 47 55, 70 93, 116 139, 146 162	I	VSS	Ground

4.0 ET9000 Pin Driving Definition

Pin Number	Pin Name	I/O Type	Driving
1	VSS	I	
2	IRQ387	O	4 ma
3	TMGATE	O	4 ma
4	MASTER-	I	
5	MAXD0	I/O	6 ma
6	MAXD1	I/O	6 ma
7	MAXD2	I/O	6 ma
8	MAXD3	I/O	6 ma
9	MAXD4	I/O	6 ma
10	MAXD5	I/O	6 ma
11	MAXD6	I/O	6 ma
12	MAXD7	I/O	6 ma
13	VSS	I	
14	MAXD8	I/O	6 ma
15	MAXD9	I/O	6 ma
16	MAXD10	I/O	6 ma
17	MAXD11	I/O	6 ma
18	MAXD12	I/O	6 ma
19	MAXD13	I/O	6 ma
20	MAXD14	I/O	6 ma
21	MAXD15	I/O	6 ma
22	NPRST	O	12 ma
23	VDD	I	
24	VSS	I	
25	CX2	O	4 ma
26	CX1	I	
27	CLK2IN	I	
28	EXACLK	I	

4.0 ET9000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
29	ECLK2IN	I	
30	PHLDA	I	
31	WR-	O	4 ma
32	MIO-	O	4 ma
33	DC-	O	4 ma
34	RESET3	O	12 ma
35	BSY6KEN-	O	12 ma
36	HOLD	O	4 ma
37	ER36IGN-	O	4 ma
38	NMI	O	4 ma
39	BE0-	I/O	4 ma
40	BE1-	I/O	4 ma
41	BE2-	I/O	4 ma
42	BE3-	I/O	4 ma
43	ER7FERR-	I	
44	BS7BLST-	I	
45	BS16-	O	4 ma
46	VDD	I	
47	VSS	I	
48	ADS-	O	4 ma
49	CRD1-	O	12 ma
50	CRD0-	O	12 ma
51	CWE1-	O	12 ma
52	CWE0-	O	12 ma
53	TOEDWE-	O	4 ma
54	TAGWT-	O	6 ma
55	VSS	I	
56	DIRTY	I/O	6 ma

4.0 ET9000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
57	TAGA0	O	6 ma
58	TAGA1	O	6 ma
59	TAGA2	O	6 ma
60	TAGA3	O	6 ma
61	TAGA4	O	6 ma
62	TAGA5	O	6 ma
63	TAGA6	O	6 ma
64	TAGA7	O	6 ma
65	A2	I	
66	A3	I	
67	A4	I	
68	RDY-	I/O	12 ma
69	VDD	I	
70	VSS	I	
71	RDYIN-	I	
72	Q6BRDY-	O	12 ma
73	CCA3	O	6 ma
74	CCA2	O	6 ma
75	A5	I	
76	A6	I	
77	A7	I	
78	A8	I/O	4 ma
79	A9	I/O	4 ma
80	A10	I/O	4 ma
81	A11	I/O	4 ma
82	A12	I/O	4 ma
83	A13	I/O	4 ma
84	A14	I/O	4 ma

4.0 ET9000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
85	A15	I/O	4 ma
86	A16	I/O	4 ma
87	A17	I	
88	A18	I	
89	A19	I	
90	A20	I/O	4 ma
91	A21	I	
92	VDD	I	
93	VSS	I	
94	A22	I	
95	A23	I	
96	A24	O	4 ma
97	A31	I	
98	CD31	I/O	4 ma
99	CD30	I/O	4 ma
100	CD29	I/O	4 ma
101	CD28	I/O	4 ma
102	CD27	I/O	4 ma
103	CD26	I/O	4 ma
104	CD25	I/O	4 ma
105	CD24	I/O	4 ma
106	CD23	I/O	4 ma
107	CD22	I/O	4 ma
108	CD21	I/O	4 ma
109	CD20	I/O	4 ma
110	CD19	I/O	4 ma
111	CD18	I/O	4 ma
112	CD17	I/O	4 ma

4.0 ET9000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
113	CD16	I/O	4 ma
114	CD15	I/O	4 ma
115	VDD	I	
116	VSS	I	
117	CD14	I/O	4 ma
118	CD13	I/O	4 ma
119	CD12	I/O	4 ma
120	CD11	I/O	4 ma
121	CD10	I/O	4 ma
122	CD9	I/O	4 ma
123	CD8	I/O	4 ma
124	CD7	I/O	4 ma
125	CD6	I/O	4 ma
126	CD5	I/O	4 ma
127	CD4	I/O	4 ma
128	CD3	I/O	4 ma
129	CD2	I/O	4 ma
130	CD1	I/O	4 ma
131	CD0	I/O	4 ma
132	SPKOUT	O	4 ma
133	PWRGD	I	
134	MISC	I	
135	IOCHCK-	I	
136	RESET4	O	4 ma
137	8042CS-	O	4 ma
138	VDD	I	
139	VSS	I	
140	CAS3-/CA25	I/O	12 ma

4.0 ET9000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
141	CAS2-	O	12 ma
142	CAS1-	O	12 ma
143	CAS0-	O	12 ma
144	RAS0-	O	12 ma
145	RAS1-	O	12 ma
146	VSS	I	
147	MP0	I/O	6 ma
148	MP1	I/O	6 ma
149	MP2	I/O	6 ma
150	MP3	I/O	6 ma
151	DWROMS-	O	6 ma
152	BUSCLK	O	6 ma
153	CHRDY	I/O	6 ma
154	IOR-	I/O	4 ma
155	IOW-	I/O	4 ma
156	MEMR-	I/O	4 ma
157	MEMW-	I/O	4 ma
158	0WS-	I	
159	REF-	I/O	12 ma
160	IOCS16-	I	
161	VDD	I	
162	VSS	I	
163	BALE	O	12 ma
164	XBHE-	I/O	4 ma
165	MCS16-	I	
166	L1MCS-	O	4 ma
167	SDEN-	O	4 ma
168	SDIR0-	O	4 ma

4.0 ET9000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
169	SDIR1-	O	4 ma
170	XA0	I/O	4 ma
171	XA1	I/O	4 ma
172	AEN8-	I	
173	AEN16-	I	
174	ADSTB16	I	
175	ADSTB8	I	
176	HLDAOUT	O	4 ma
177	DMAHRQ	I	
178	INTA-	O	4 ma
179	TMOUT2	I	
180	RTCAS	O	4 ma
181	XA20M	I/O	4 ma
182	ACK-	O	4 ma
183	OSC119	O	6 ma
184	VDD	I	

4.1 ET9000 Absolute Maximum Ragings

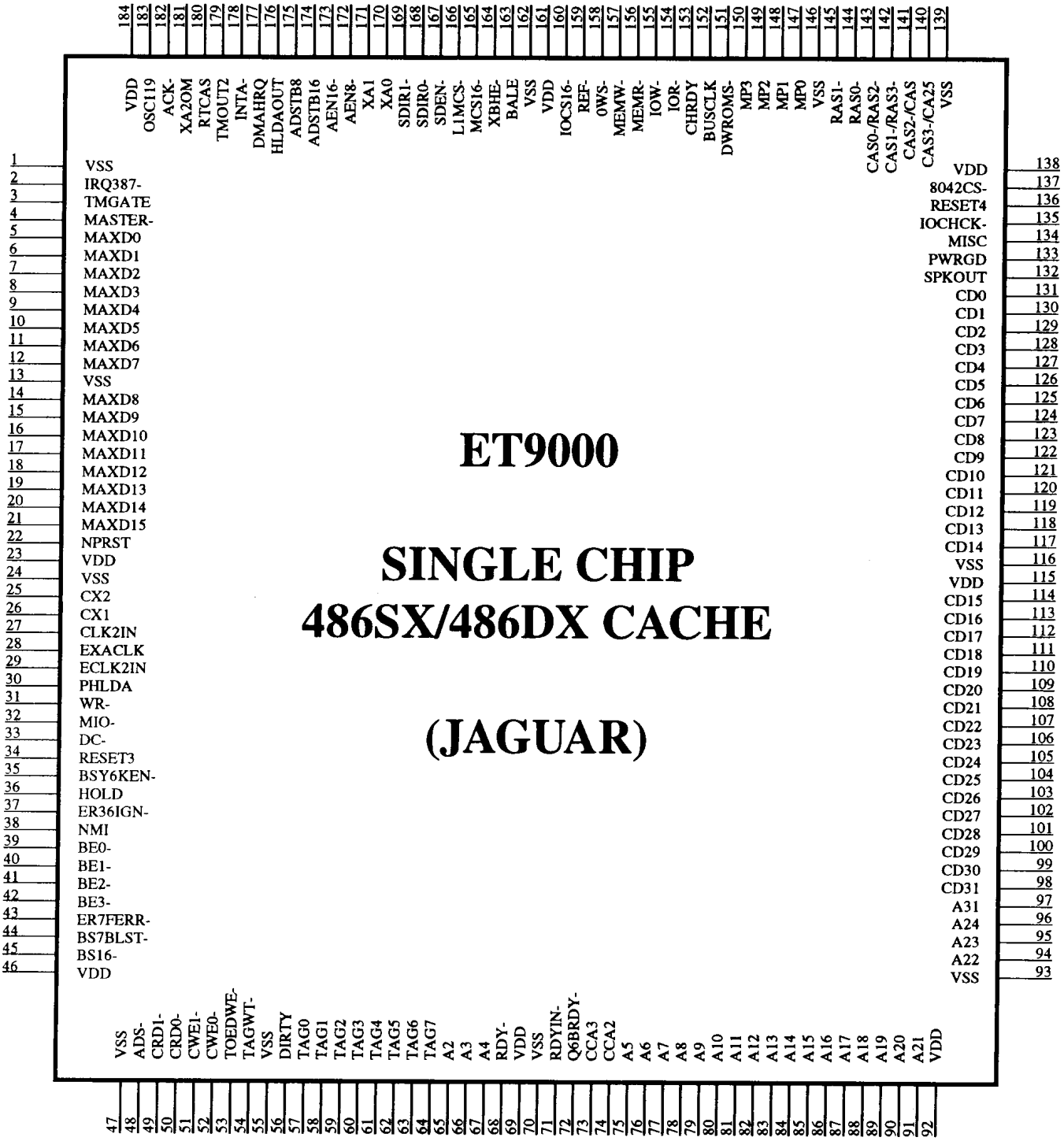
	Symbol	Min	Max	Units
Supply Voltage	VDD		7.0	V
Input Voltage	VIN	-0.5	5.5	V
Output Voltage	VOUT	-0.5	5.5	V
Operating Temperature	Top	-2.5	50	C
Storage Temperature	Tstg	-40	125	C

4.2 ET9000 Operating Condition

	Symbol	Min	Max	Units
Supply Voltage	VDD	4.75	5.25	V
Ambient Temperature	TA	0	50	C

4.3 ET9000 DC Characteristics

	Symbol	Min	Max	Units
Input Low Voltage	VIL			
TTL Level (All pins except PWRGD)			0.8	V
SHMT Level (PWRGD pin)			1.0	V
Input High Voltage	VIH			
TTL Level (All pins except PWRGD, TURBO- and CLK2IN)		2.0		V
CLK2IN Level		3.7		V
SHMT Level (PWRGD and TURBO- pins)		4.0		V
Output Low Voltage	VOL		0.45	V
Output High Voltage	VOH	2.4		V
Input Low Current AT VIN=VSS	IIL	-10	10	uA
Input High Current AT VIN=VDD	IIH	-10	10	uA
Tri-State Output OFF Current LOW	IOZL		-10	uA
Tri-State Output OFF Current HIGH	IOZH		10	uA
Output Leakage Current	IOH		TBD	
Output Short Circuit Current	IOS		TBD	
Power Supply Current	EDD			
@20MHz			150	mA
@25MHz			200	mA
@33MHz			230	mA
Input Capacitance	CIN		7	pF
Output or I/O Capacitance	COUT		10	pF


ET9000
SINGLE CHIP
486SX/486DX CACHE
(JAGUAR)
1 VSS
2 IRQ387-
3 TMGATE
4 MASTER-
5 MAXD0
6 MAXD1
7 MAXD2
8 MAXD3
9 MAXD4
10 MAXD5
11 MAXD6
12 MAXD7
13 VSS
14 MAXD8
15 MAXD9
16 MAXD10
17 MAXD11
18 MAXD12
19 MAXD13
20 MAXD14
21 MAXD15
22 NPRST
23 VDD
24 VSS
25 CX2
26 CX1
27 CLK2IN
28 EXACLK
29 ECLK2IN
30 PHLDA
31 WR-
32 MIO-
33 DC-
34 RESET3
35 BSY6KEN-
36 HOLD
37 ER36IGN-
38 NMI
39 BE0-
40 BE1-
41 BE2-
42 BE3-
43 ER7FERR-
44 BS7BLST-
45 BS16-
46 VDD
47 VSS
48 ADS-
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50 CRD0-
51 CWE1-
52 CWE0-
53 TOEDWE-
54 TAGWT-
55 VSS
56 DIRTY
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58 TAG1
59 TAG2
60 TAG3
61 TAG4
62 TAG5
63 TAG6
64 TAG7
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66 A3
67 A4
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69 VDD
70 VSS
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73 CCA3
74 CCA2
75 A5
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80 A10
81 A11
82 A12
83 A13
84 A14
85 A15
86 A16
87 A17
88 A18
89 A19
90 A20
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92 VDD
93 VSS
94 A22
95 A23
96 A24
97 A31
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105 CD24
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116 VSS
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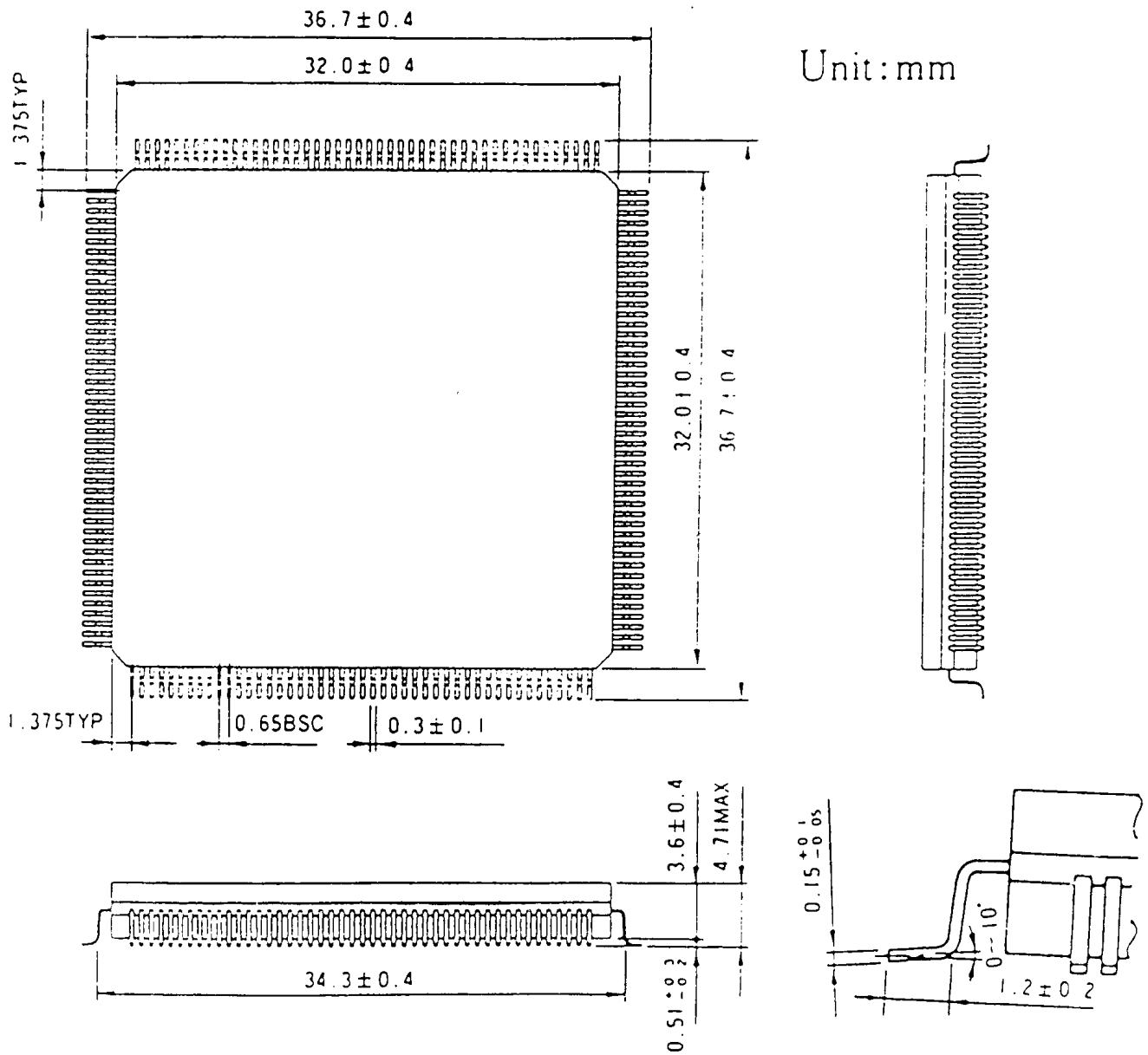
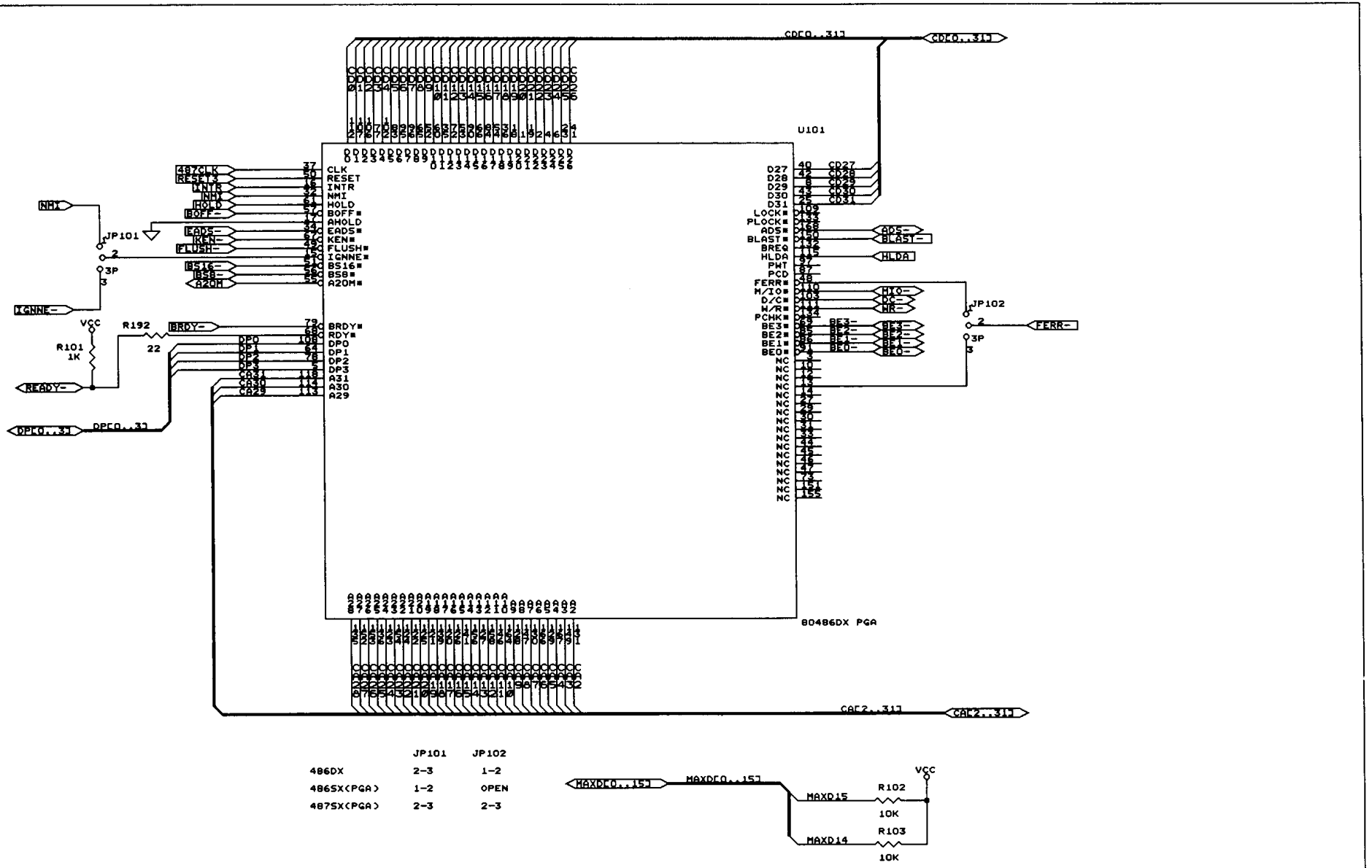
126 CD5
127 CD4
128 CD3
129 CD2
130 CD1
131 CD0
132 SPKOUT
133 PWRGD
134 MISC
135 IOCHCK-
136 RESET4
137 8042CS-
138 VDD
139 VSS
140 CAS3-/CA25
141 CAS2-/CAS
142 CAS1-/RAS3-
143 CAS0-/RAS2-
144 RAS0-
145 RAS1-
146 VSS
147 MP0
148 MP1
149 MP2
150 MP3
151 DWROMS-
152 BUSCLK
153 CHRDY
154 IOR-
155 IOW-
156 MEMR-
157 MEMW-
158 0WS-
159 REF-
160 IOCS16-
161 VDD
162 VSS
163 BALE
164 XBHE-
165 MCS16-
166 L1MCS-
167 SDEN-
168 SDIR0-
169 SDIR1-
170 XA0
171 XA1
172 AEN8-
173 AEN16-
174 ADSTB16
175 ADSTB8
176 HLDAOUT
177 DMAHRQ
178 INTA-
179 TMOUT2
180 RTCAS
181 XA20M
182 ACK-
183 OSC119
184 VDD

QFP184-G-3232(184-Pin Ceramic Flat Package)

Unit: mm





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487SX(PGA)	2-3	2-3

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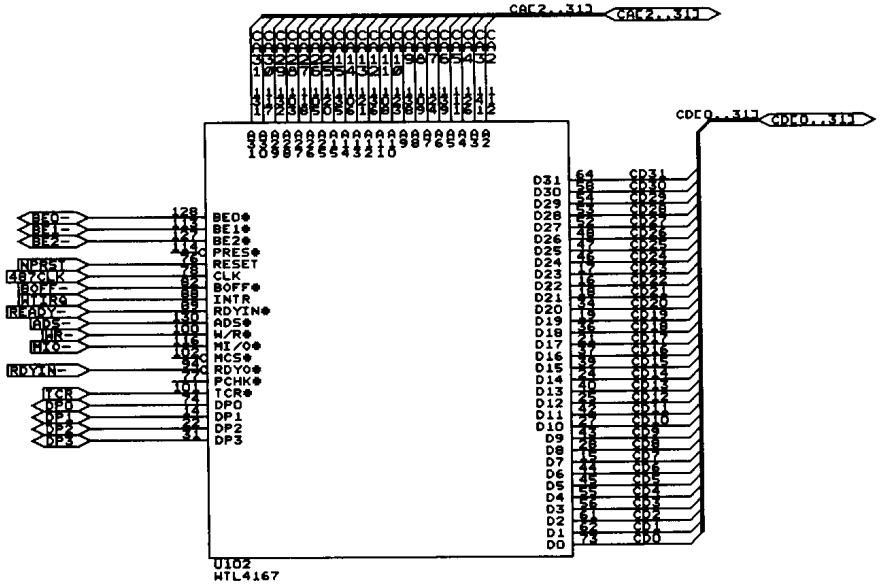
Size: B	Document Number: CPU	REV: 1.1
Date: June 29, 1992	Sheet 1 of 11	



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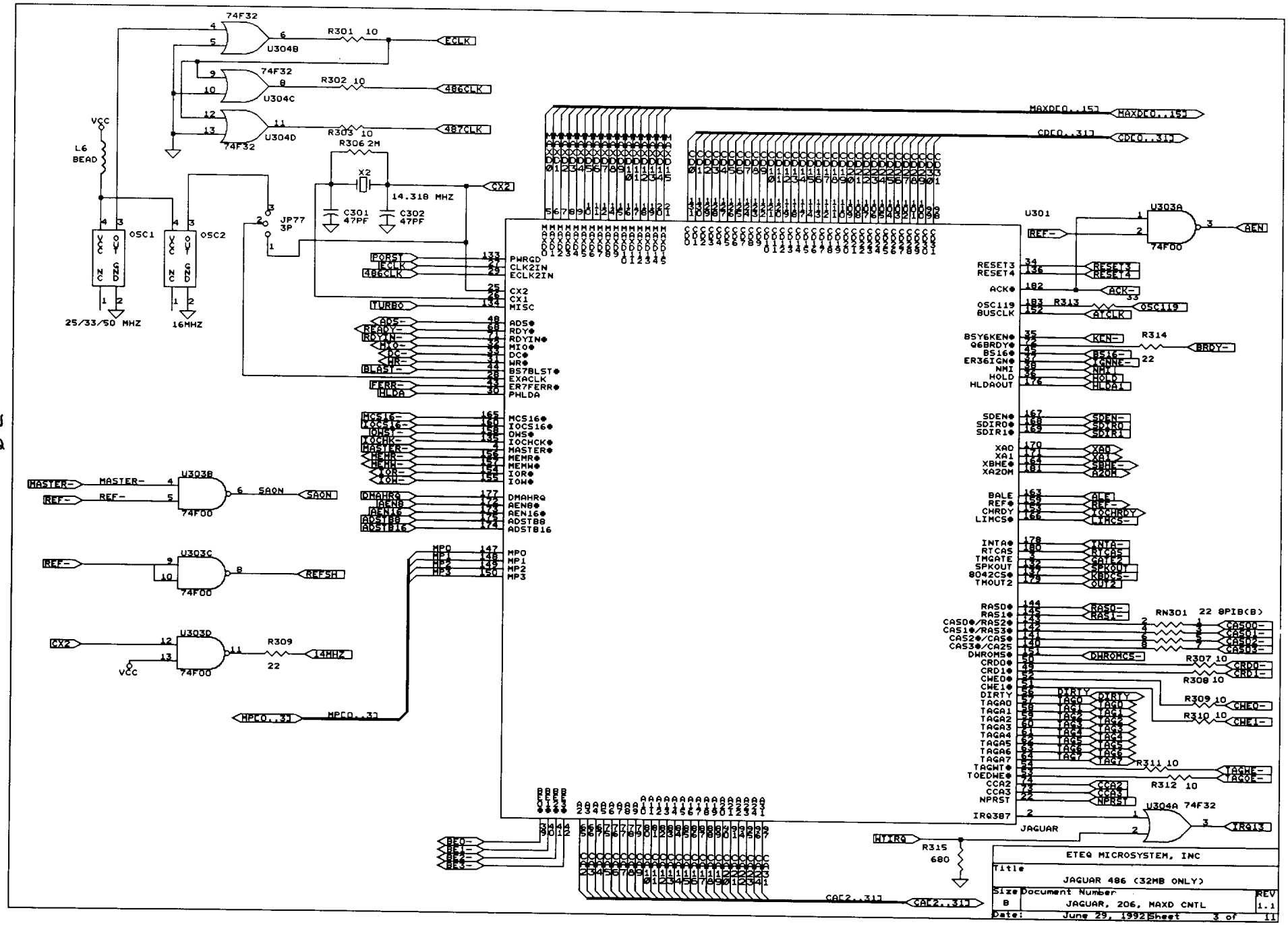
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R301 10
ECLK
U304C
R302 10
486CLK
U304D
R303 10
487CLK
VCC
L6
BEAD
R306 2M
X2
14.318 MHZ
CX2
C301
47PF
C302
47PF
OSC1
OSC2
JP77
3P
25/33/50 MHZ
16MHZ
PORST
ECLK
486CLK
TURBO
BLAST-
FERR-
HLDA
MCS16-
IOCS16-
IOWS-
IOCHK-
MASTER-
MEMR-
MEMW-
IOR-
IOW-
DMAHRQ
AEN8
AEN16
ADSTB8
ADSTB16
MP0
MP1
MP2
MP3
MPC0..3]
MAXDFC0..15]
CDFC0..31]
U301
U303A
74F00
AEN
RESET3
RESET4
ACK-
OSC119
BUSCLK
R313
ATCLK
KEN-
R314
BRDY-
BS16-
NMI
HOLD
HLDA1
SDEN-
SDIR0
SDIR1
XA0
XA1
SBHE-
A20M
ALE
REF-
IOCHRDY
LIMCS-
INTA-
RTCAS
GATE2
SPKOUT
KBDCS-
OUT2
RAS0-
RAS1-
RN301 22 8PIB(B)
CAS0-
CAS1-
CAS2-
CAS3-
DWROMCS-
R307 10
CRD0-
CRD1-
R308 10
R309 10
CWE0-
R310 10
CWE1-
DIRTY
TAG0
TAG1
TAG2
TAG3
TAG4
TAG5
TAG6
TAG7
R311 10
TAGWE-
TAGOE-
R312 10
TOEDWE-
CCA2
CCA3
NPRST
IRQ387
U304A 74F32
IRQ13
JAGUAR
HIXIRQ
R315
680
U303B
MASTER-
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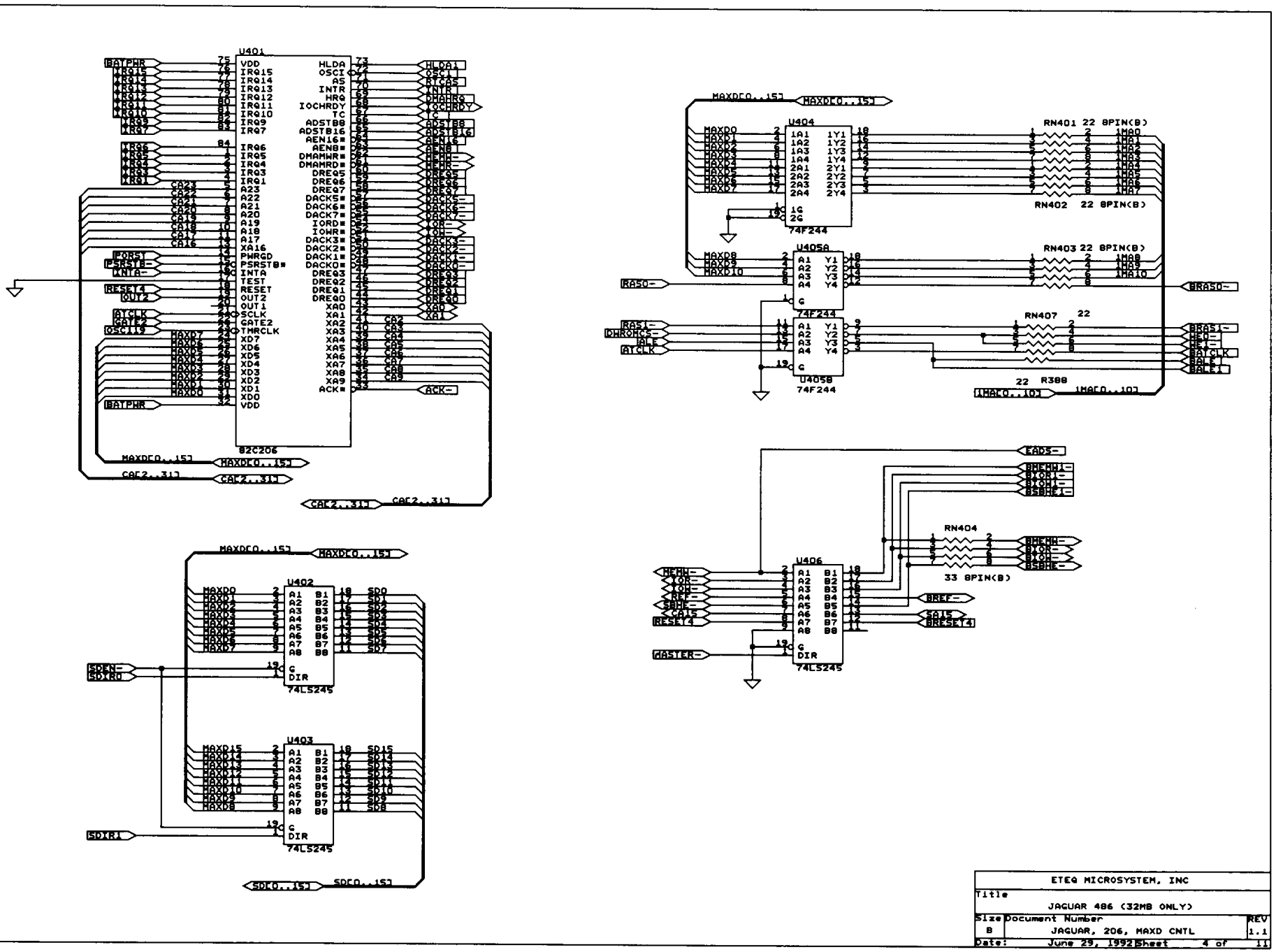
Size B
Document Number
JAGUAR, 206, MAXD CNTL
REV 1.1
Date: June 29, 1992
Sheet 3 of 11



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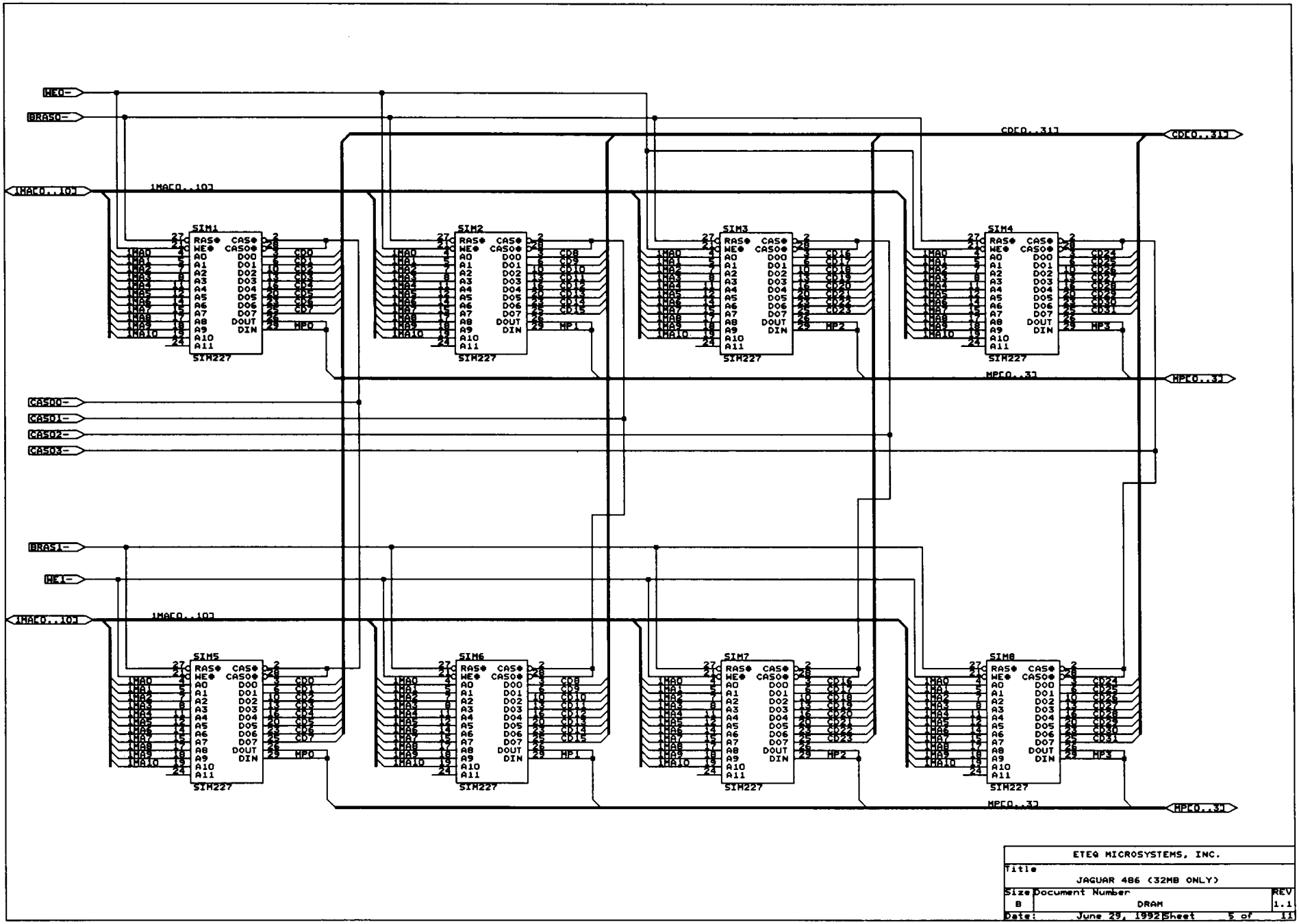
Date: June 29, 1992	Sheet 4 of 11	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ETEQ MICROSYSTEMS, INC.
Title
JAGUAR 486 (32MB ONLY)
Size B
Document Number
DRAM
REV 1.1
Date: June 29, 1992
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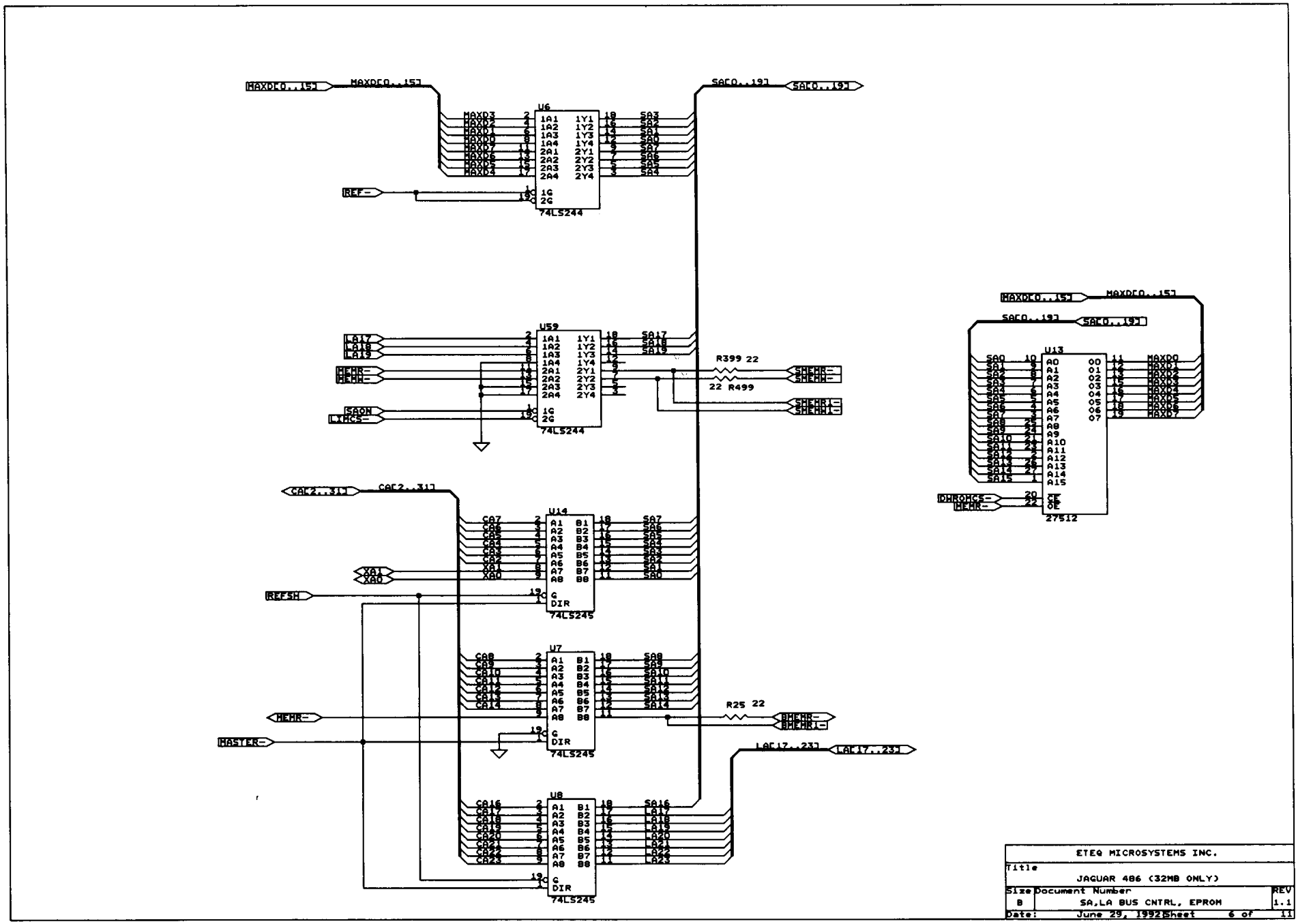
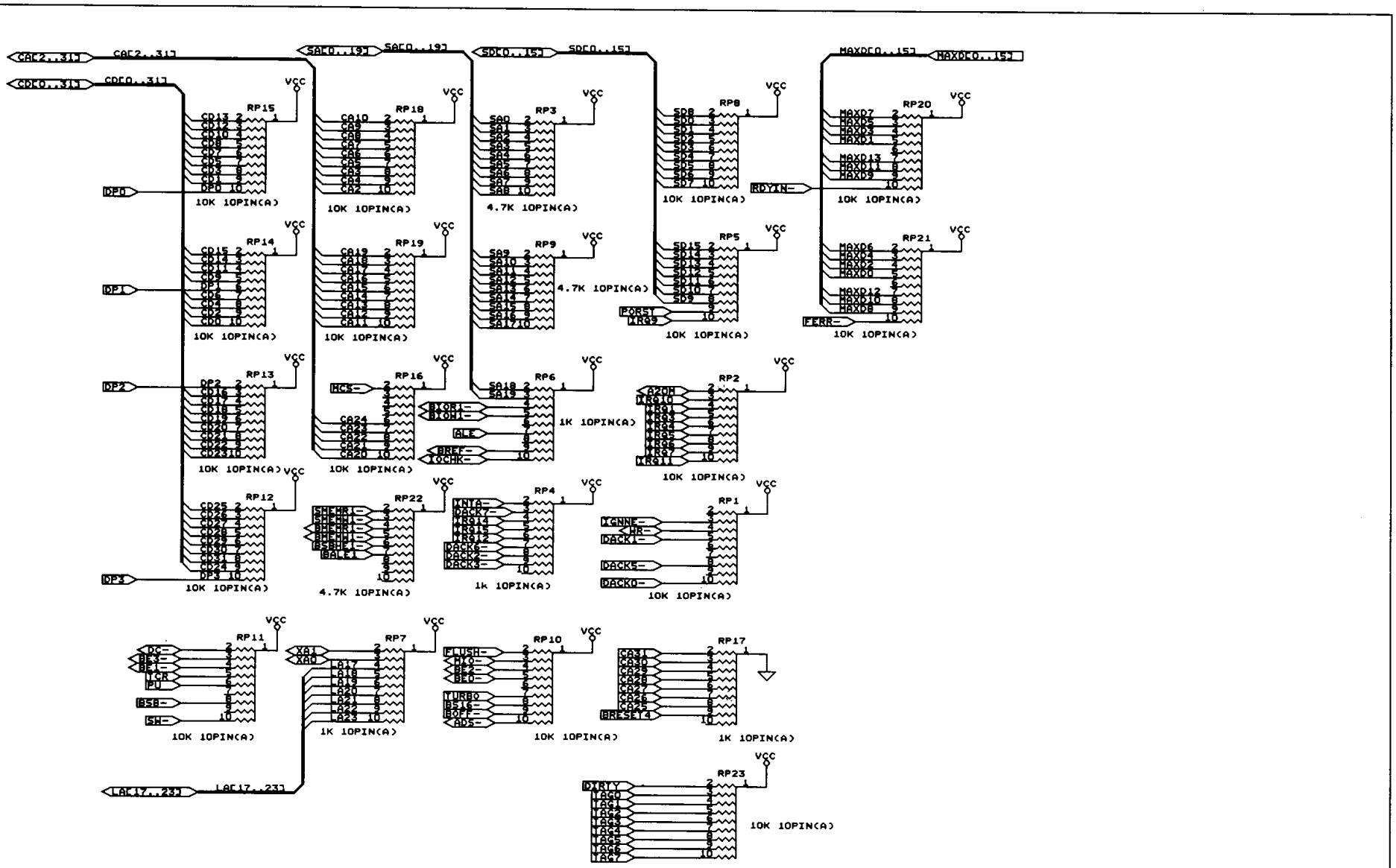


ETEQ MICROSYSTEMS INC.		
Title: JAGUAR 486 (32MB ONLY)		
Size: B	Document Number: SA,LA BUS CNTRL, EPROM	REV: 1.1
Date: June 29, 1992	Sheet 6 of 11	



ETEQ MICROSYSTEMS INC.		
Title: JAGUAR 486 (32MB ONLY)		
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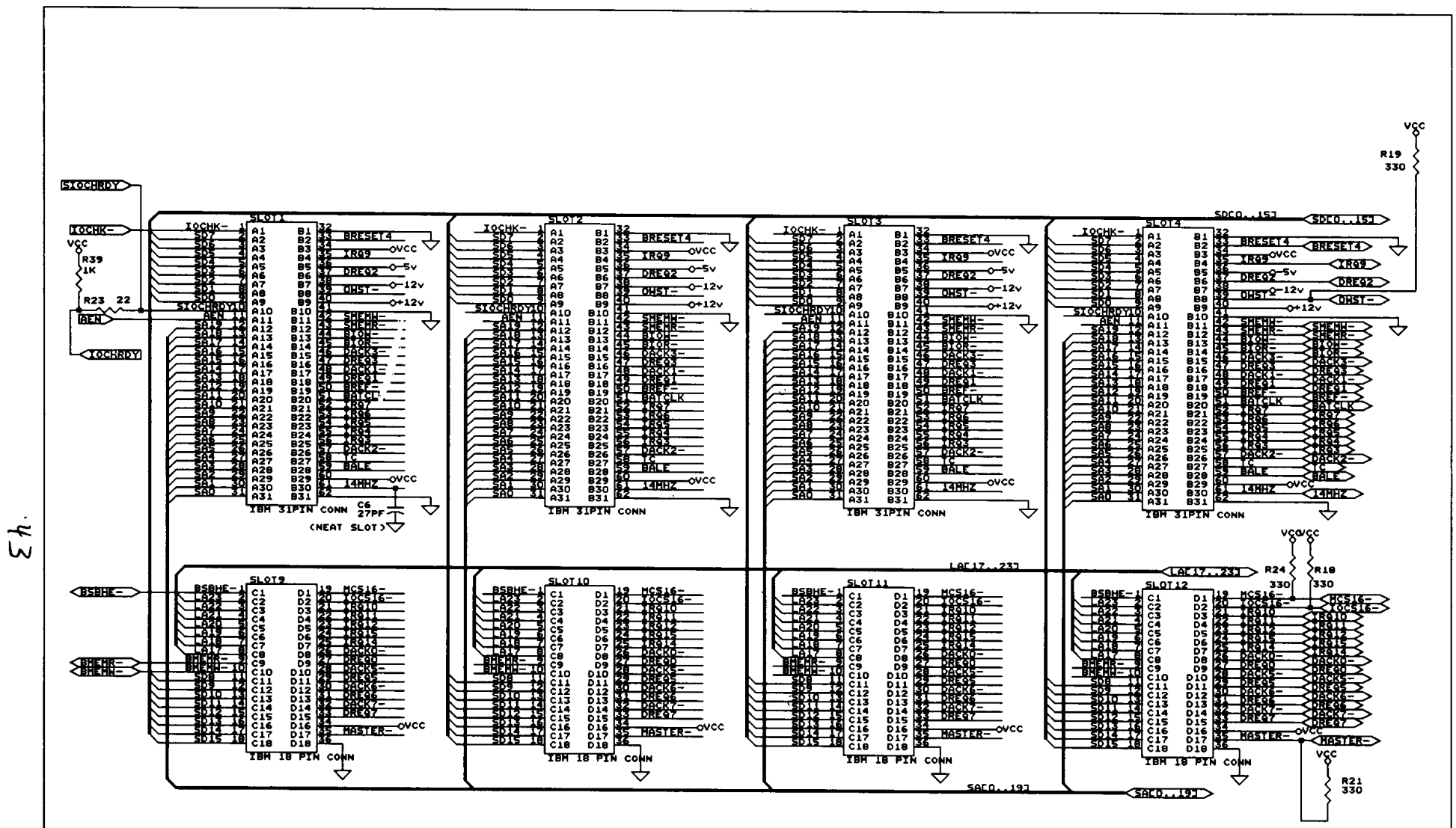
Date: June 29, 1992	Sheet 7 of 11	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1K
R23 22
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SLOT2
SLOT3
SLOT4
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C6
27PF
(NEAT SLOT)
SLOT9
SLOT10
SLOT11
SLOT12
IBM 18 PIN CONN
BSBHE-
BHEHR-
BHEHW-
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ETEQ MICROSYSTEMS, INC.
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Size
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Document Number
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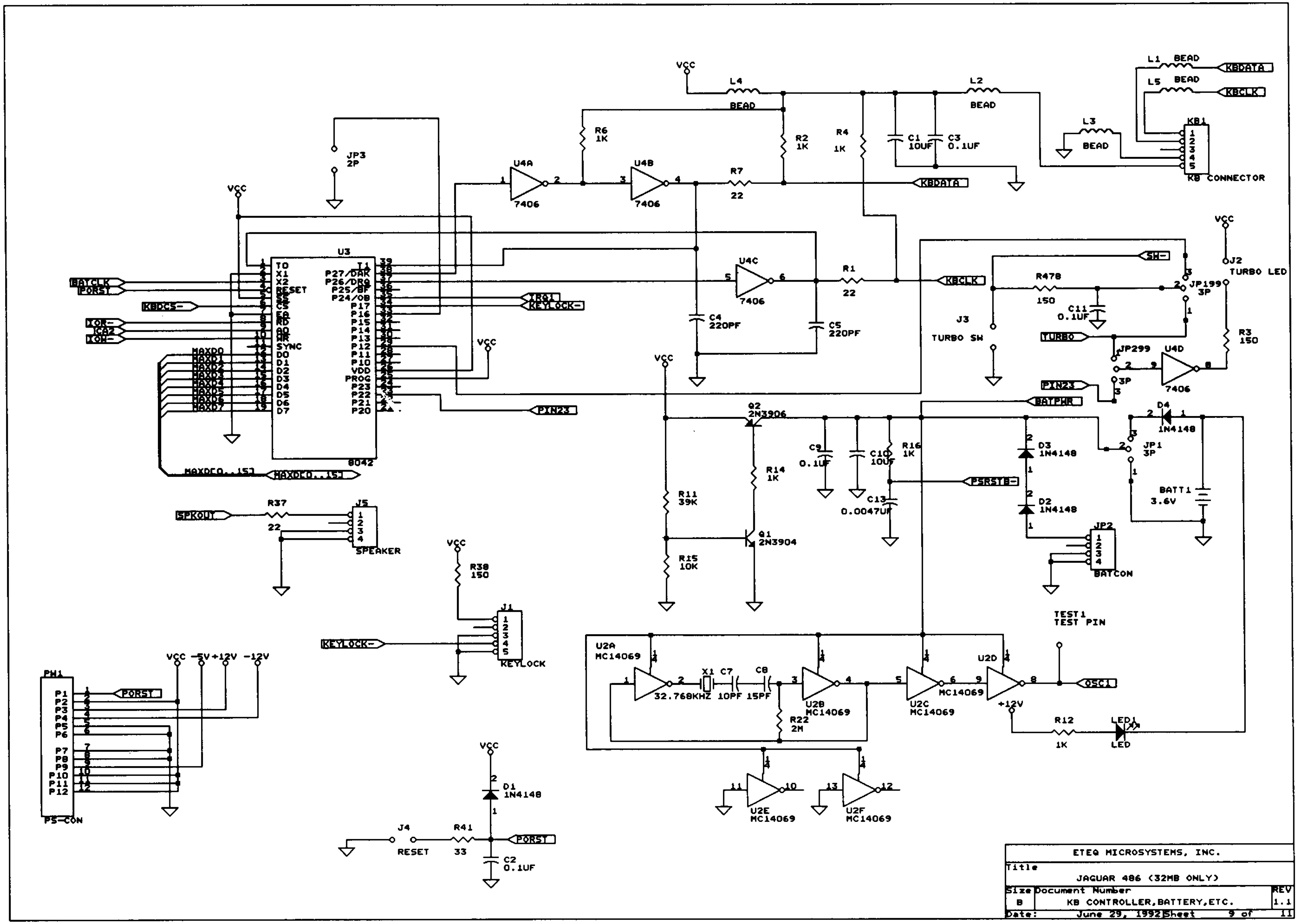
REV
1.1
Date:
June 29, 1992
Sheet
8 of
11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Title
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Document Number
KB CONTROLLER,BATTERY,ETC.
REV 1.1
Date: June 29, 1992
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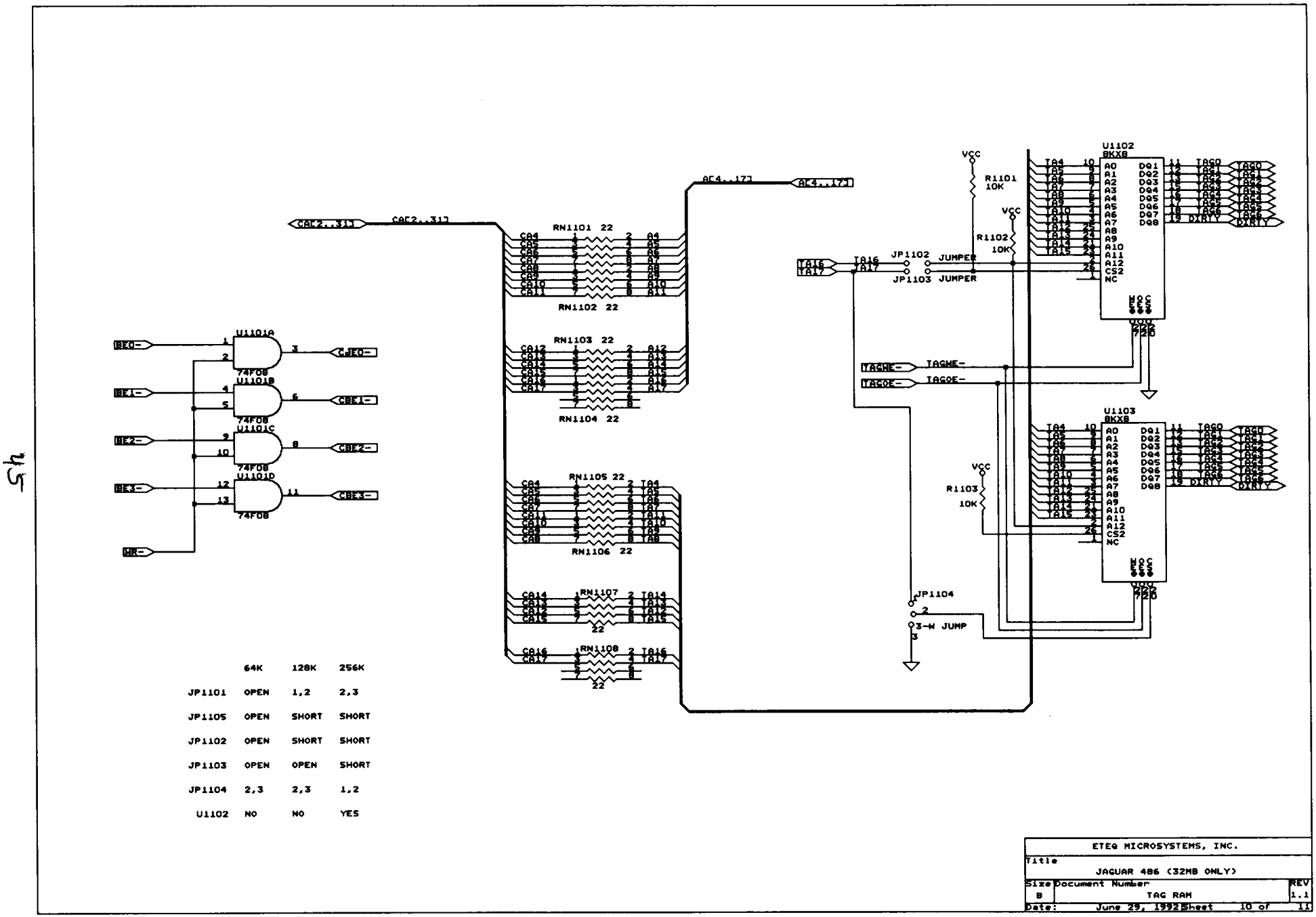

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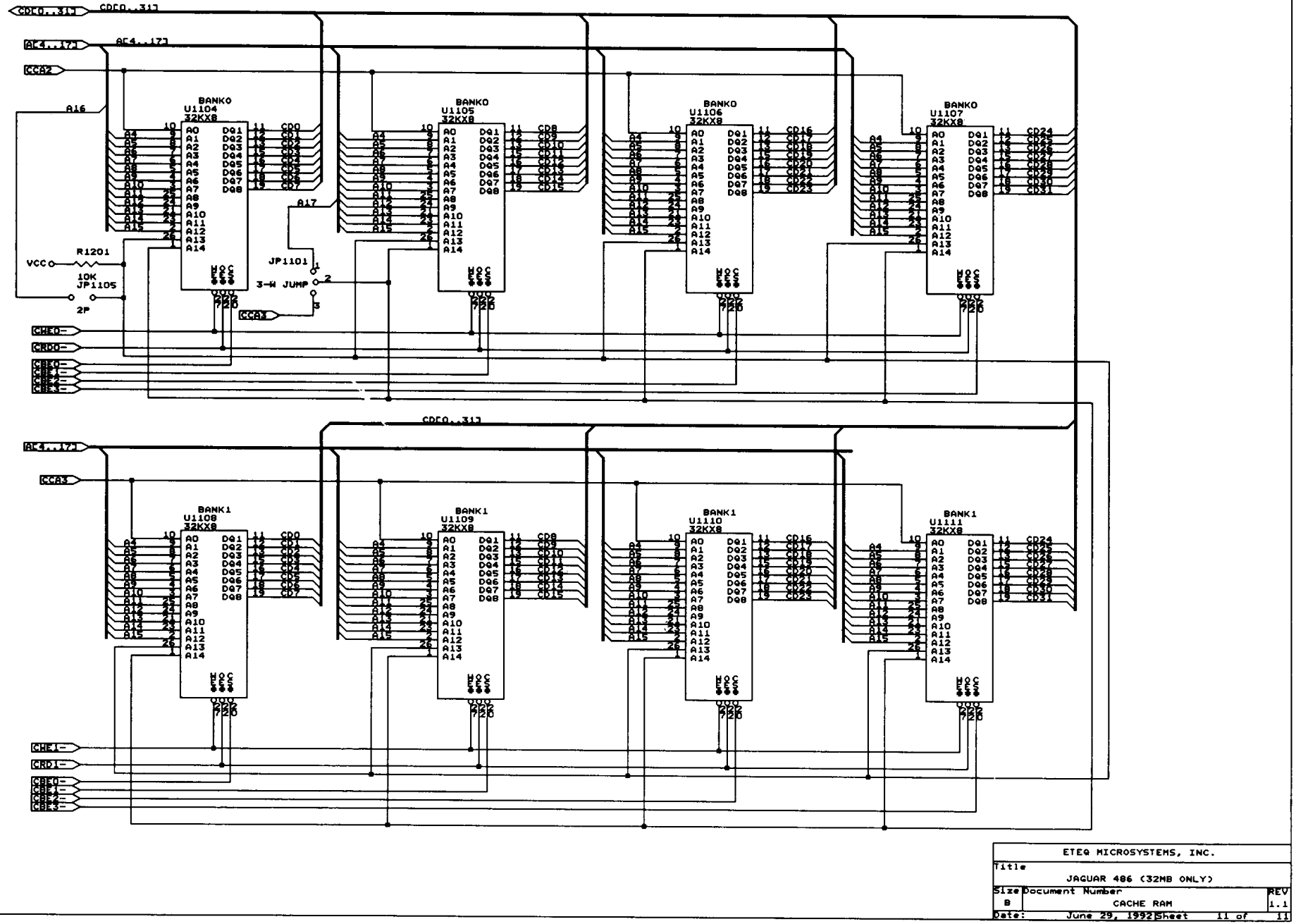
JP1101	OPEN	1,2	2,3
JP1105	OPEN	SHORT	SHORT
JP1102	OPEN	SHORT	SHORT
JP1103	OPEN	OPEN	SHORT
JP1104	2,3	2,3	1,2
U1102	NO	NO	YES

ETEQ MICROSYSTEMS, INC.		
Title: JAGUAR 486 (32MB ONLY)		
Size: B	Document Number: TAG RAM	REV: 1.1
Date: June 29, 1992	Sheet 10 of 11	



ETEQ MICROSYSTEMS, INC.		
Title: JAGUAR 486 (32MB ONLY)		
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Date: June 29, 1992	Sheet 11 of 11	