

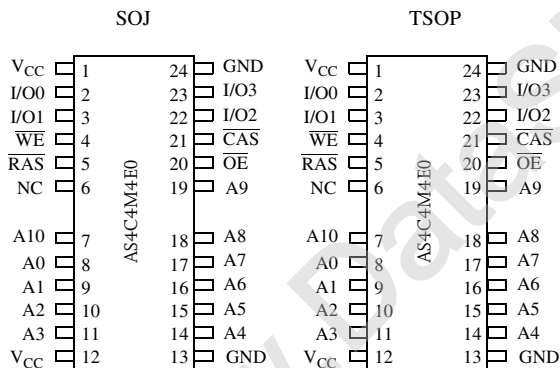


## 4M×4 CMOS DRAM (EDO) family

### Features

- Organization: 4,194,304 words × 4 bits
- High speed
  - 50/60 ns  $\overline{\text{RAS}}$  access time
  - 25/30 ns column address access time
  - 12/15 ns  $\overline{\text{CAS}}$  access time
- Low power consumption
  - Active: 908 mW max
  - Standby: 5.5 mW max, CMOS I/O
- Extended data out
- Refresh
  - 2048 refresh cycles, 32 ms refresh interval for AS4C4M4E1
  - $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
- TTL-compatible, three-state I/O
- JEDEC standard package
  - 300 mil, 24/26-pin SOJ
  - 300 mil, 24/26-pin TSOP
- 5V power supply
- Latch-up current  $\geq 200$  mA
- ESD protection  $\geq 2000$  volts
- Industrial and commercial temperature available

### Pin arrangement



### Pin designation

| Pin(s)                  | Description           |
|-------------------------|-----------------------|
| A0 to A10               | Address inputs        |
| $\overline{\text{RAS}}$ | Row address strobe    |
| $\overline{\text{CAS}}$ | Column address strobe |
| $\overline{\text{WE}}$  | Write enable          |
| I/O0 to I/O3            | Input/output          |
| $\overline{\text{OE}}$  | Output enable         |
| $V_{\text{CC}}$         | Power                 |
| GND                     | Ground                |

### Selection guide

|  | Symbol           | AS4C4M4E1-50 | AS4C4M4E1-60 | Unit |
|--|------------------|--------------|--------------|------|
| Maximum $\overline{\text{RAS}}$ access time                  | $t_{\text{RAC}}$ | 50           | 60           | ns   |
| Maximum column address access time                           | $t_{\text{CAA}}$ | 25           | 30           | ns   |
| Maximum $\overline{\text{CAS}}$ access time                  | $t_{\text{CAC}}$ | 12           | 15           | ns   |
| Maximum output enable ( $\overline{\text{OE}}$ ) access time | $t_{\text{OEA}}$ | 13           | 15           | ns   |
| Minimum read or write cycle time                             | $t_{\text{RC}}$  | 85           | 100          | ns   |
| Minimum fast page mode cycle time                            | $t_{\text{PC}}$  | 25           | 30           | ns   |
| Maximum operating current                                    | $I_{\text{CC1}}$ | 135          | 120          | mA   |
| Maximum CMOS standby current                                 | $I_{\text{CC5}}$ | 2.0          | 2.0          | mA   |



## Functional description

The AS4C4M4E1 is a high performance 16-megabit CMOS Dynamic Random Access Memories (DRAM) organized as 4,194,304 words  $\times$  4 bits. The devices are fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in PC, workstation, router and switch applications.

This product features a high speed page mode operation where read and write operations within a single row (or page) can be executed at very high speed by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  inputs respectively. Also,  $\overline{\text{RAS}}$  is used to make the column address latch transparent, enabling application of column addresses prior to  $\overline{\text{CAS}}$  assertion.

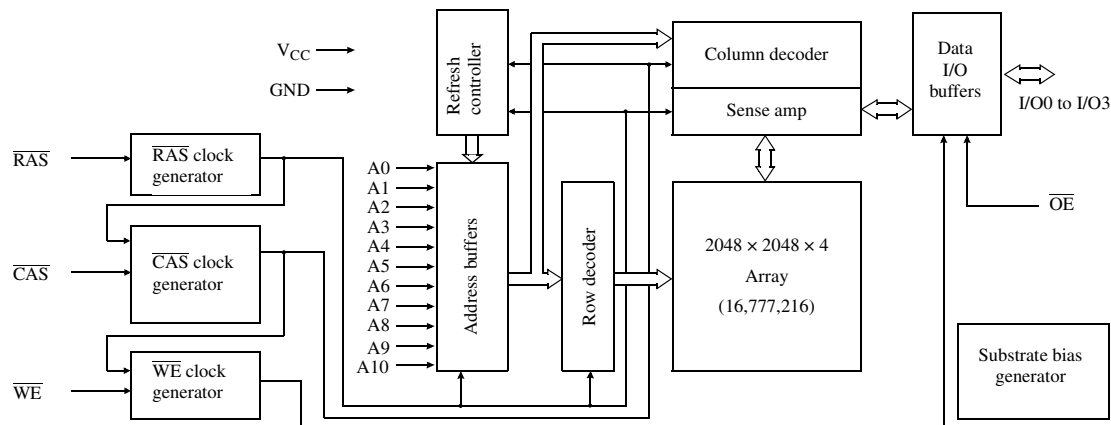
Extended data out (EDO) read mode enables 60MHz operation using 60ns devices. In contrast to 'fast page mode' devices, data remains active on outputs after  $\overline{\text{CAS}}$  is de-asserted high, giving system logic more time to latch the data. Use  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrence of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  going high.

Refresh on the 2048 address combinations of A0 to A10 must be performed every 32 ms using:

- $\overline{\text{RAS}}$ -only refresh:  $\overline{\text{RAS}}$  is asserted while  $\overline{\text{CAS}}$  is held high. Each of the 2048 rows must be strobed. Outputs remain high impedance.
- Hidden refresh:  $\overline{\text{CAS}}$  is held low while  $\overline{\text{RAS}}$  is toggled. Refresh address is generated internally. Outputs remain low impedance with previous valid data.
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh (CBR): At least one  $\overline{\text{CAS}}$  is asserted prior to  $\overline{\text{RAS}}$ . Refresh address is generated internally. Outputs are high-impedance ( $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  are don't care).
- Normal read or write cycles refresh the row being accessed.

The AS4C4M4E1 is available in the standard 24/26-pin plastic SOJ and 24/26-pin plastic TSOP packages. The AS4C4M4E1 operates with a single power supply of  $5\text{V} \pm 0.5\text{V}$ . It provides TTL compatible inputs and outputs.

## Logic block diagram for 2K refresh



## Recommended operating conditions

| Parameter                     | Symbol     | Min               | Nominal | Max      | Unit |
|-------------------------------|------------|-------------------|---------|----------|------|
| Supply voltage                | $V_{CC}$   | 4.5               | 5.0     | 5.5      | V    |
|                               | GND        | 0.0               | 0.0     | 0.0      | V    |
| Input voltage                 | $V_{IH}$   | 2.4               | —       | $V_{CC}$ | V    |
|                               | $V_{IL}$   | -0.5 <sup>†</sup> | —       | 0.8      | V    |
| Ambient operating temperature | Commercial | 0                 | —       | 70       | °C   |
|                               | Industrial | -40               | —       | 85       |      |

<sup>†</sup> $V_{IL}$  min -3.0V for pulse widths less than 5 ns. Recommended operating conditions apply throughout this document unless otherwise specified.



## Absolute maximum ratings

| Parameter                     | Symbol       | Min  | Max             | Unit     |
|-------------------------------|--------------|------|-----------------|----------|
| Input voltage                 | $V_{in}$     | -1.0 | +7.0            | V        |
| Input voltage (DQs)           | $V_{DQ}$     | -1.0 | $V_{CC} + 0.5$  | V        |
| Power supply voltage          | $V_{CC}$     | -1.0 | +7.0            | V        |
| Storage temperature (plastic) | $T_{STG}$    | -55  | +150            | °C       |
| Soldering temperature × time  | $T_{SOLDER}$ | –    | $260 \times 10$ | °C × sec |
| Power dissipation             | $P_D$        | –    | 1               | W        |
| Short circuit output current  | $I_{out}$    | –    | 50              | mA       |

## DC electrical characteristics

| Parameter  | Symbol    | Test conditions   | -50 |     | -60 |     | Unit | Notes |
|--|-----------|---|-----|-----|-----|-----|------|-------|
|  |           |   | Min | Max | Min | Max |      |       |
| Input leakage current  | $I_{IL}$  | $0V \leq V_{in} \leq +5.5V$ ,<br>Pins not under test = 0V   | -5  | +5  | -5  | +5  | μA   |       |
| Output leakage current   | $I_{OL}$  | $D_{OUT}$ disabled, $0V \leq V_{out} \leq +5.5V$  | -5  | +5  | -5  | +5  | μA   |       |
| Operating power supply current                                     | $I_{CC1}$ | $\overline{RAS}$ , $\overline{CAS}$ Address cycling; $t_{RC} = \text{min}$  | –   | 135 | –   | 120 | mA   | 1, 2  |
| TTL standby power supply current                                   | $I_{CC2}$ | $\overline{RAS} = \overline{CAS} \geq V_{IH}$   | –   | 2.0 | –   | 2.0 | mA   |       |
| Average power supply current, $\overline{RAS}$ refresh mode or CBR | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH}$ ,<br>$t_{RC} = \text{min}$ of $\overline{RAS}$ low after $\overline{CAS}$ low. | –   | 120 | –   | 110 | mA   | 1     |
| EDO page mode average power supply current                         | $I_{CC4}$ | $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ address cycling; $t_{HPC} = \text{min}$  | –   | 130 | –   | 120 | mA   | 1, 2  |
| CMOS standby power supply current                                  | $I_{CC5}$ | $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$   | –   | 2.0 | –   | 2.0 | mA   |       |
| Output voltage   | $V_{OH}$  | $I_{OUT} = -5.0 \text{ mA}$   | 2.4 | –   | 2.4 | –   | V    |       |
|  | $V_{OL}$  | $I_{OUT} = 4.2 \text{ mA}$  | –   | 0.4 | –   | 0.4 | V    |       |
| $\overline{CAS}$ before $\overline{RAS}$ refresh current           | $I_{CC6}$ | $\overline{RAS}$ or $\overline{CAS}$ cycling, $t_{RC} = \text{min}$   | –   | 120 | –   | 110 | mA   |       |



## AC parameters common to all waveforms

| Symbol    | Parameter   | -50 |     | -60 |     | Unit | Notes |
|-----------|---|-----|-----|-----|-----|------|-------|
|           |   | Min | Max | Min | Max |      |       |
| $t_{RC}$  | Random read or write cycle time                     | 80  | –   | 100 | –   | ns   |       |
| $t_{RP}$  | $\overline{RAS}$ precharge time                     | 30  | –   | 40  | –   | ns   |       |
| $t_{RAS}$ | $\overline{RAS}$ pulse width                        | 50  | 10K | 60  | 10K | ns   |       |
| $t_{CAS}$ | $\overline{CAS}$ pulse width                        | 8   | 10K | 10  | 10K | ns   |       |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ delay time     | 15  | 35  | 15  | 43  | ns   | 6     |
| $t_{RAD}$ | $\overline{RAS}$ to column address delay time       | 12  | 25  | 12  | 30  | ns   | 7     |
| $t_{RSH}$ | $\overline{CAS}$ to $\overline{RAS}$ hold time      | 10  | –   | 10  | –   | ns   |       |
| $t_{CSH}$ | $\overline{RAS}$ to $\overline{CAS}$ hold time      | 40  | –   | 50  | –   | ns   |       |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ precharge time | 5   | –   | 5   | –   | ns   |       |
| $t_{ASR}$ | Row address setup time                              | 0   | –   | 0   | –   | ns   |       |
| $t_{RAH}$ | Row address hold time                               | 8   | –   | 10  | –   | ns   |       |
| $t_T$     | Transition time (rise and fall)                     | 1   | 50  | 1   | 50  | ns   | 4,5   |
| $t_{REF}$ | Refresh period                                      | –   | 32  | –   | 32  | ms   | 16    |
| $t_{CP}$  | $\overline{CAS}$ precharge time                     | 8   | –   | 10  | –   | ns   |       |
| $t_{RAL}$ | Column address to $\overline{RAS}$ lead time        | 25  | –   | 30  | –   | ns   |       |
| $t_{ASC}$ | Column address setup time                           | 0   | –   | 0   | –   | ns   |       |
| $t_{CAH}$ | Column address hold time                            | 8   | –   | 10  | –   | ns   |       |

## Read cycle

| Symbol    | Parameter                                  | -50 |     | -60 |     | Unit | Notes |
|-----------|--|-----|-----|-----|-----|------|-------|
|           |  | Min | Max | Min | Max |      |       |
| $t_{RAC}$ | Access time from $\overline{RAS}$          | –   | 50  | –   | 60  | ns   | 6     |
| $t_{CAC}$ | Access time from $\overline{CAS}$          | –   | 12  | –   | 15  | ns   | 6,13  |
| $t_{AA}$  | Access time from address                   | –   | 25  | –   | 30  | ns   | 7,13  |
| $t_{RCS}$ | Read command setup time                    | 0   | –   | 0   | –   | ns   |       |
| $t_{RCH}$ | Read command hold time to $\overline{CAS}$ | 0   | –   | 0   | –   | ns   | 9     |
| $t_{RRH}$ | Read command hold time to $\overline{RAS}$ | 0   | –   | 0   | –   | ns   | 9     |



## Write cycle

| Symbol    | Parameter                                   | -50 |     | -60 |     | Unit | Notes |
|-----------|---|-----|-----|-----|-----|------|-------|
|           |   | Min | Max | Min | Max |      |       |
| $t_{WCS}$ | Write command setup time                    | 0   | –   | 0   | –   | ns   | 11    |
| $t_{WCH}$ | Write command hold time                     | 10  | –   | 10  | –   | ns   | 11    |
| $t_{WP}$  | Write command pulse width                   | 10  | –   | 10  | –   | ns   |       |
| $t_{RWL}$ | Write command to $\overline{RAS}$ lead time | 10  | –   | 10  | –   | ns   |       |
| $t_{CWL}$ | Write command to $\overline{CAS}$ lead time | 8   | –   | 10  | –   | ns   |       |
| $t_{DS}$  | Data-in setup time                          | 0   | –   | 0   | –   | ns   | 12    |
| $t_{DH}$  | Data-in hold time                           | 8   | –   | 10  | –   | ns   | 12    |

## Read-modify-write cycle

| Symbol    | Parameter                                      | -50 |     | -60 |     | Unit | Notes |
|-----------|--|-----|-----|-----|-----|------|-------|
|           |  | Min | Max | Min | Max |      |       |
| $t_{RWC}$ | Read-write cycle time                          | 113 | –   | 135 | –   | ns   |       |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ delay time | 67  | –   | 77  | –   | ns   | 11    |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ delay time | 32  | –   | 35  | –   | ns   | 11    |
| $t_{AWD}$ | Column address to $\overline{WE}$ delay time   | 42  | –   | 47  | –   | ns   | 11    |

## Refresh cycle

| Symbol    | Parameter  | -50 |     | -60 |     | Unit | Notes |
|-----------|--|-----|-----|-----|-----|------|-------|
|           |  | Min | Max | Min | Max |      |       |
| $t_{CSR}$ | $\overline{CAS}$ setup time ( $\overline{CAS}$ -before- $\overline{RAS}$ ) | 5   | –   | 5   | –   | ns   | 3     |
| $t_{CHR}$ | $\overline{CAS}$ hold time ( $\overline{CAS}$ -before- $\overline{RAS}$ )  | 8   | –   | 10  | –   | ns   | 3     |
| $t_{RPC}$ | $\overline{RAS}$ precharge to $\overline{CAS}$ hold time                   | 0   | –   | 0   | –   | ns   |       |
| $t_{CPT}$ | $\overline{CAS}$ precharge time (CBR counter test)                         | 10  |     | 10  | –   | ns   |       |



## Hyper page mode cycle

| Symbol      | Parameter  | -50 |      | -60 |      | Unit | Notes |
|-------------|--|-----|------|-----|------|------|-------|
|             |  | Min | Max  | Min | Max  |      |       |
| $t_{CPWD}$  | $\overline{CAS}$ precharge to $\overline{WE}$ delay time | 45  | –    | 52  | –    | ns   |       |
| $t_{CPA}$   | Access time from $\overline{CAS}$ precharge              | –   | 28   | –   | 35   | ns   | 13    |
| $t_{RASP}$  | $\overline{RAS}$ pulse width                             | 50  | 100K | 60  | 100K | ns   |       |
| $t_{DOH}$   | Previous data hold time from $\overline{CAS}$            | 5   | –    | 5   | –    | ns   |       |
| $t_{REZ}$   | Output buffer turn off delay from $\overline{RAS}$       | 0   | 13   | 0   | 15   | ns   |       |
| $t_{WEZ}$   | Output buffer turn off delay from $\overline{WE}$        | 0   | 13   | 0   | 15   | ns   |       |
| $t_{OEZ}$   | Output buffer turn off delay from $\overline{OE}$        | 0   | 13   | 0   | 15   | ns   |       |
| $t_{HPC}$   | Hyper page mode cycle time                               | 20  | –    | 25  | –    | ns   |       |
| $t_{HPRWC}$ | Hyper page mode RMW cycle                                | 47  | –    | 56  | –    | ns   |       |
| $t_{RHCP}$  | $\overline{RAS}$ hold time from $\overline{CAS}$         | 30  | –    | 35  | –    | ns   |       |

## Output enable

| Symbol    | Parameter  | -50 |     | -60 |     | Unit | Notes |
|-----------|--|-----|-----|-----|-----|------|-------|
|           |  | Min | Max | Min | Max |      |       |
| $t_{CLZ}$ | $\overline{CAS}$ to output in Low Z                      | 0   | –   | 0   | –   | ns   | 8     |
| $t_{ROH}$ | $\overline{RAS}$ hold time referenced to $\overline{OE}$ | 8   | –   | 10  | –   | ns   |       |
| $t_{OEA}$ | $\overline{OE}$ access time                              | –   | 13  | –   | 15  | ns   |       |
| $t_{OED}$ | $\overline{OE}$ to data delay                            | 13  | –   | 15  | –   | ns   |       |
| $t_{OEZ}$ | Output buffer turnoff delay from $\overline{OE}$         | 0   | 13  | 0   | 15  | ns   | 8     |
| $t_{OEH}$ | $\overline{OE}$ command hold time                        | 10  | –   | 10  | –   | ns   |       |
| $t_{OLZ}$ | $\overline{OE}$ to output in Low Z                       | 0   | –   | 0   | –   | ns   |       |
| $t_{OFF}$ | Output buffer turn-off time                              | 0   | 13  | 0   | 15  | ns   | 8,10  |



## Notes

- $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$ , and  $I_{CC6}$  are dependent on frequency.
- $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
- An initial pause of 200  $\mu$ s is required after power-up followed by any 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
- AC Characteristics assume  $t_T = 2$  ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF,  $V_{IL}(\text{min}) \geq \text{GND}$  and  $V_{IH}(\text{max}) \leq V_{CC}$ .
- $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- Operation within the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
- Operation within the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only. If  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
- Assumes three state test load (5 pF and a 380  $\Omega$  Thevenin equivalent).
- Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycle.
- $t_{\text{OFF}}(\text{max})$  defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.  $t_{\text{OFF}}$  is referenced from rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.
- $t_{\text{WCS}}$ ,  $t_{\text{WCH}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$  and  $t_{\text{AWD}}$  are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If  $t_{\text{WS}} \geq t_{\text{WS}}(\text{min})$  and  $t_{\text{WH}} \geq t_{\text{WH}}(\text{min})$ , the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$  and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
- These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in read-write cycles.
- Access time is determined by the longest of  $t_{\text{CAA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{CPA}}$
- $t_{\text{ASC}} \geq t_{\text{CP}}$  to achieve  $t_{\text{PC}}(\text{min})$  and  $t_{\text{CPA}}(\text{max})$  values.
- These parameters are sampled and not 100% tested.
- These characteristics apply to AS4C4M4E1 5V devices.

## AC test conditions

- Access times are measured with output reference levels of  $V_{\text{OH}} = 2.4\text{V}$  and  $V_{\text{OL}} = 0.4\text{V}$ ,  
 $V_{\text{IH}} = 2.4\text{V}$  and  $V_{\text{IL}} = 0.8\text{V}$
- Input rise and fall times: 2 ns

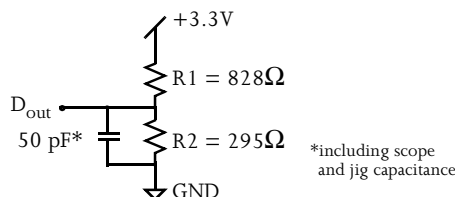


Figure A: Equivalent output load  
(AS4C4M4E1)

## Key to switching waveforms



Rising input



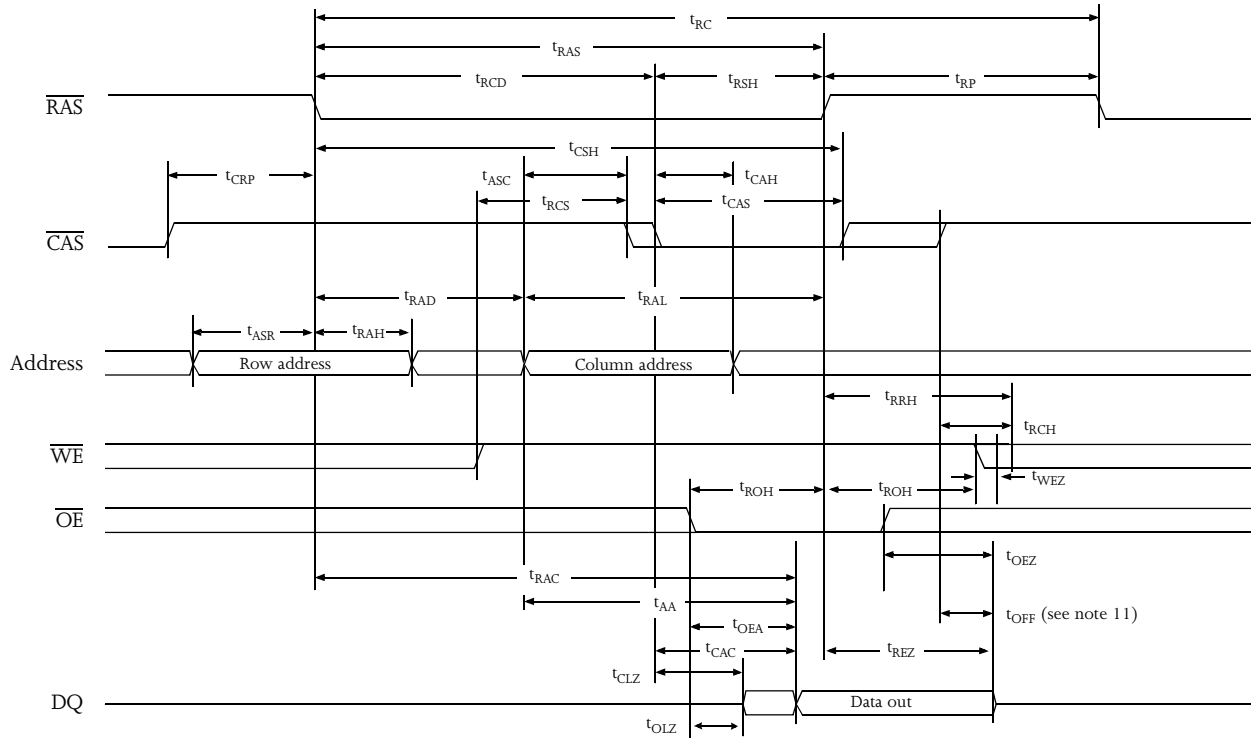
Falling input



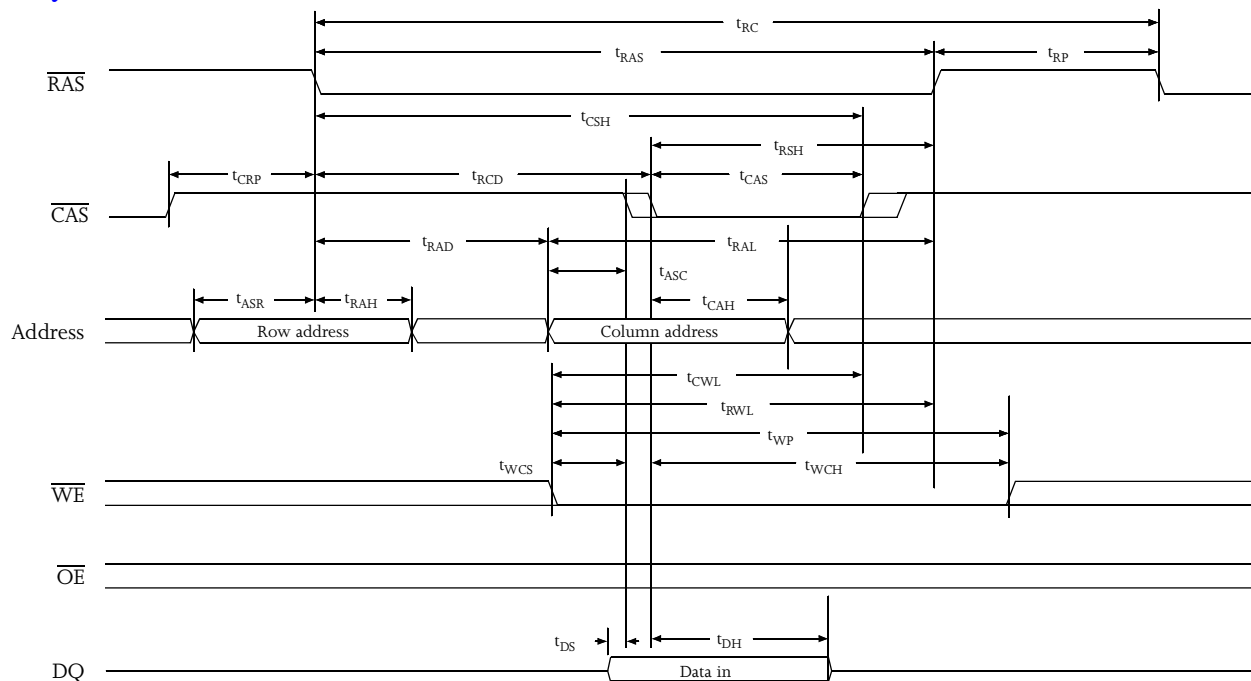
Undefined output/don't care



Read waveform



Early write waveform

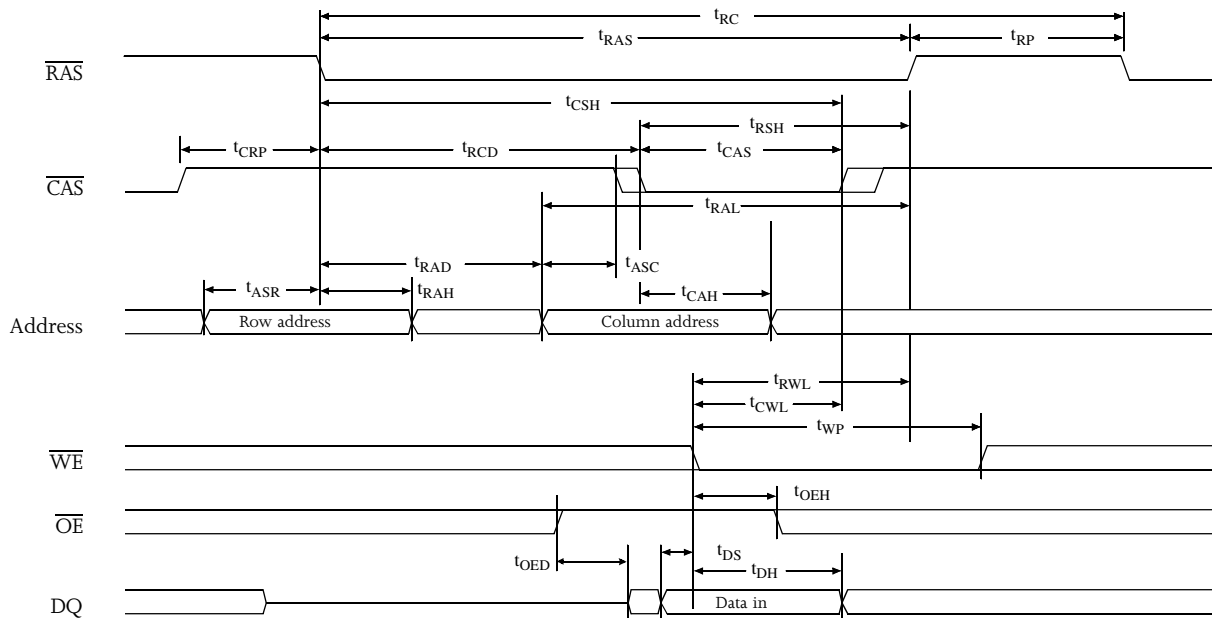




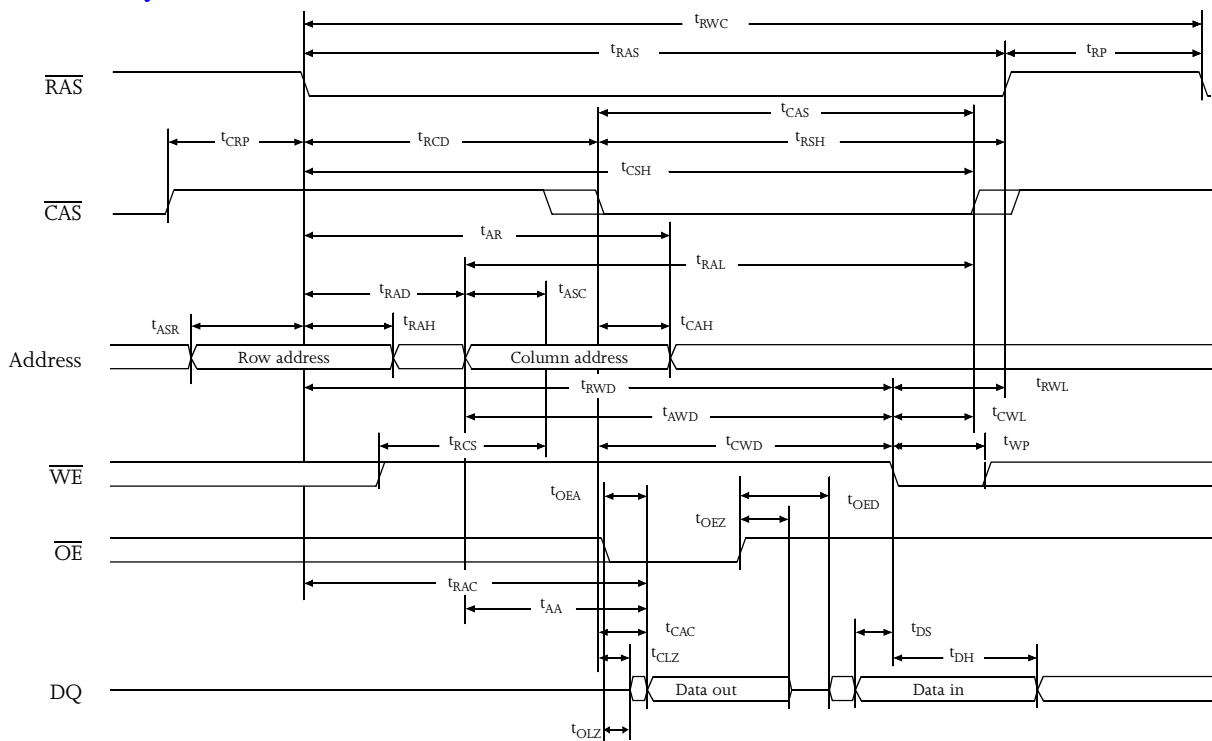


Write waveform

$\overline{OE}$  controlled

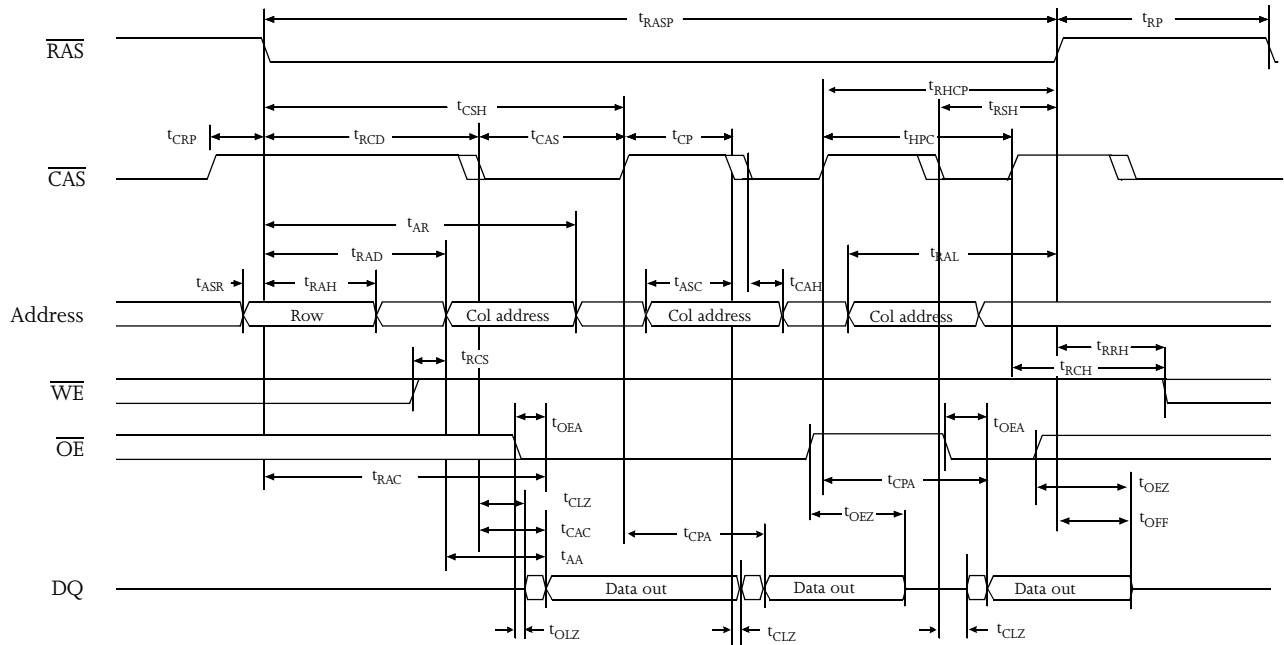


Read-modify-write waveform

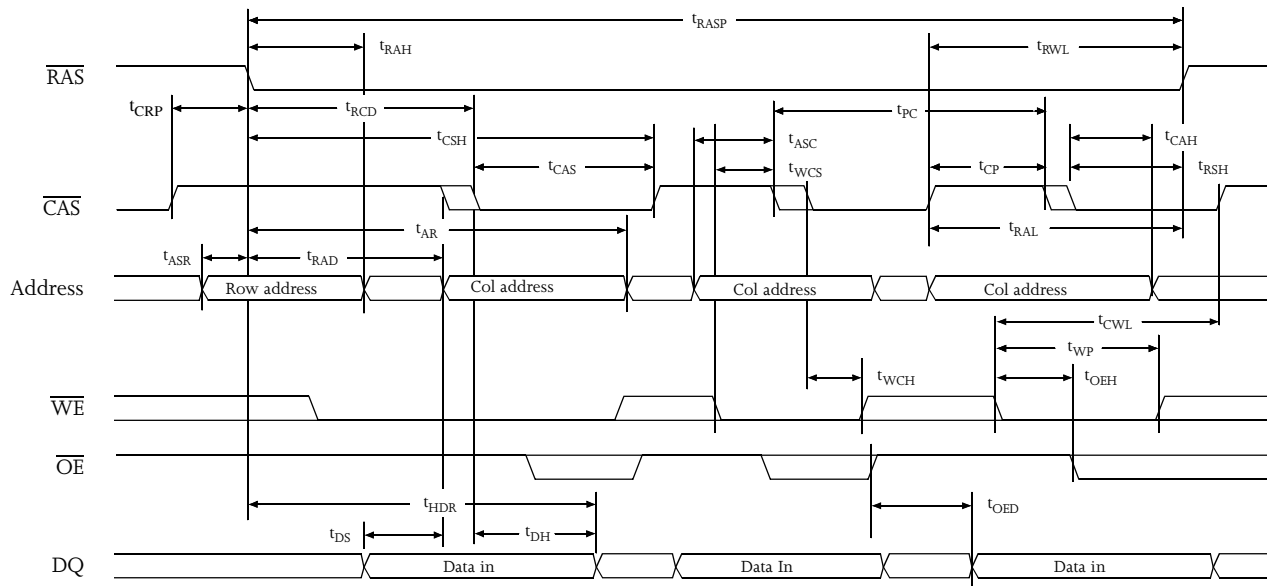




## EDO page mode read waveform

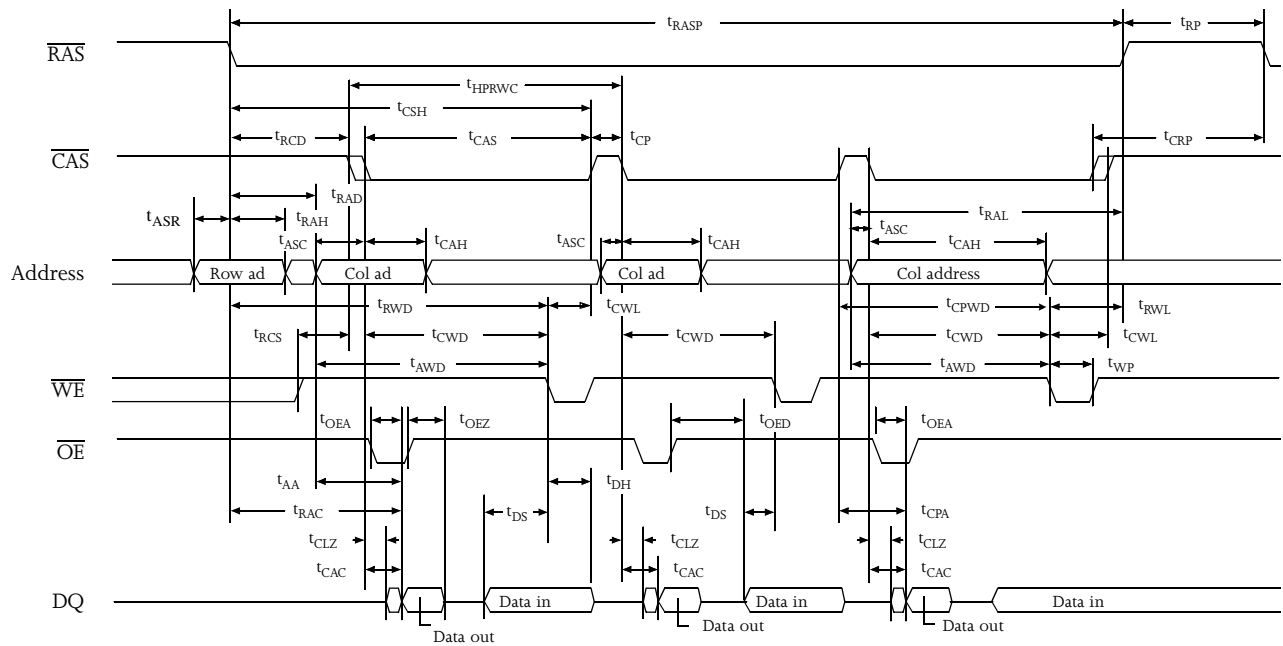


## EDO page mode early write waveform



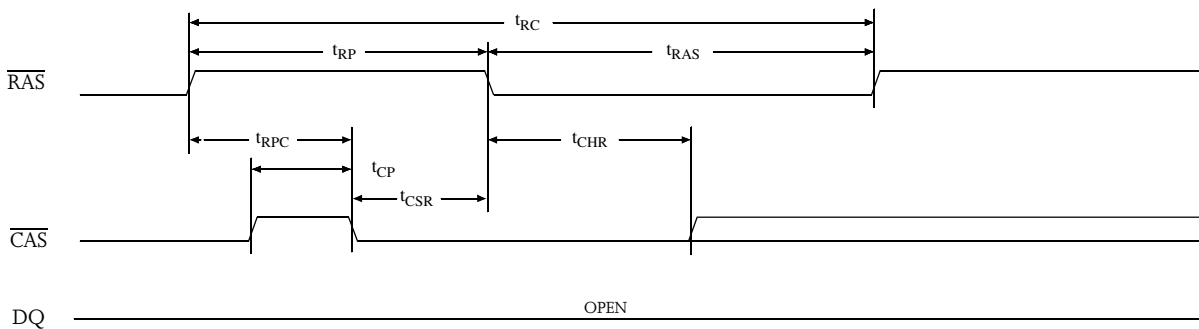


EDO page mode read-modify-write waveform



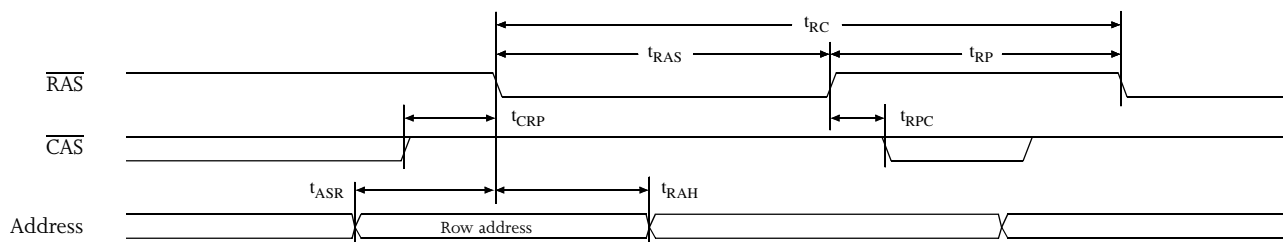
CAS before RAS refresh waveform

$\overline{WE} = A = V_{IH} \text{ or } V_{IL}$



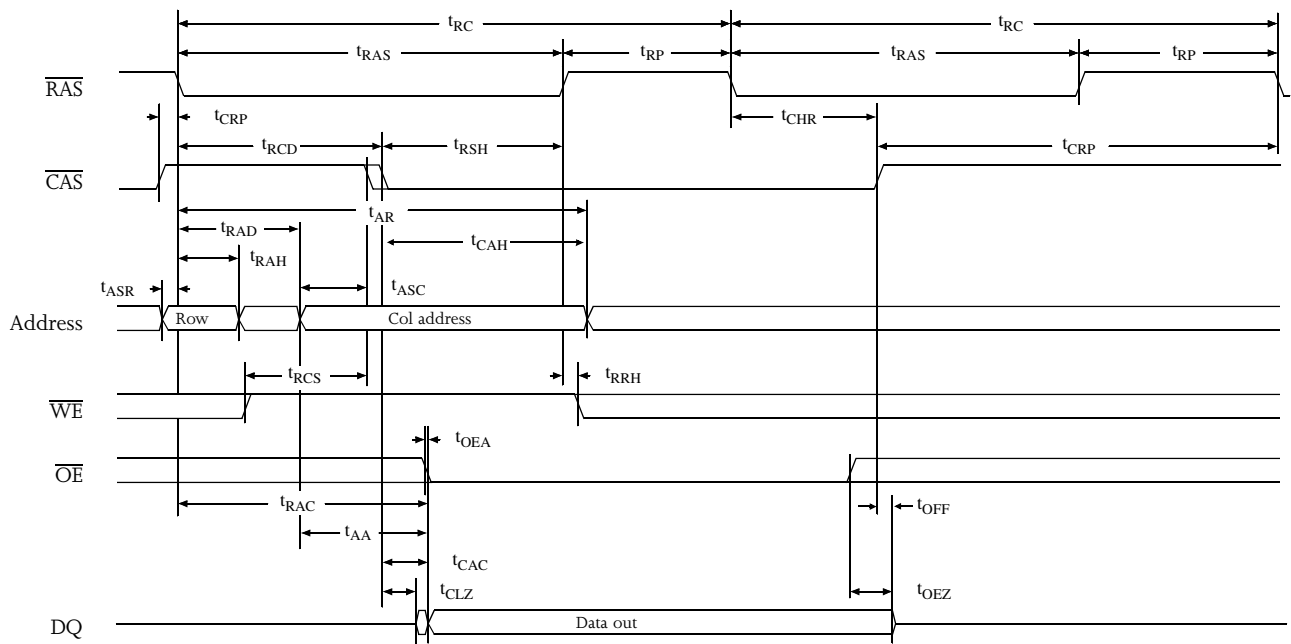
RAS only refresh waveform

$\overline{WE} = \overline{OE} = V_{IH} \text{ or } V_{IL}$

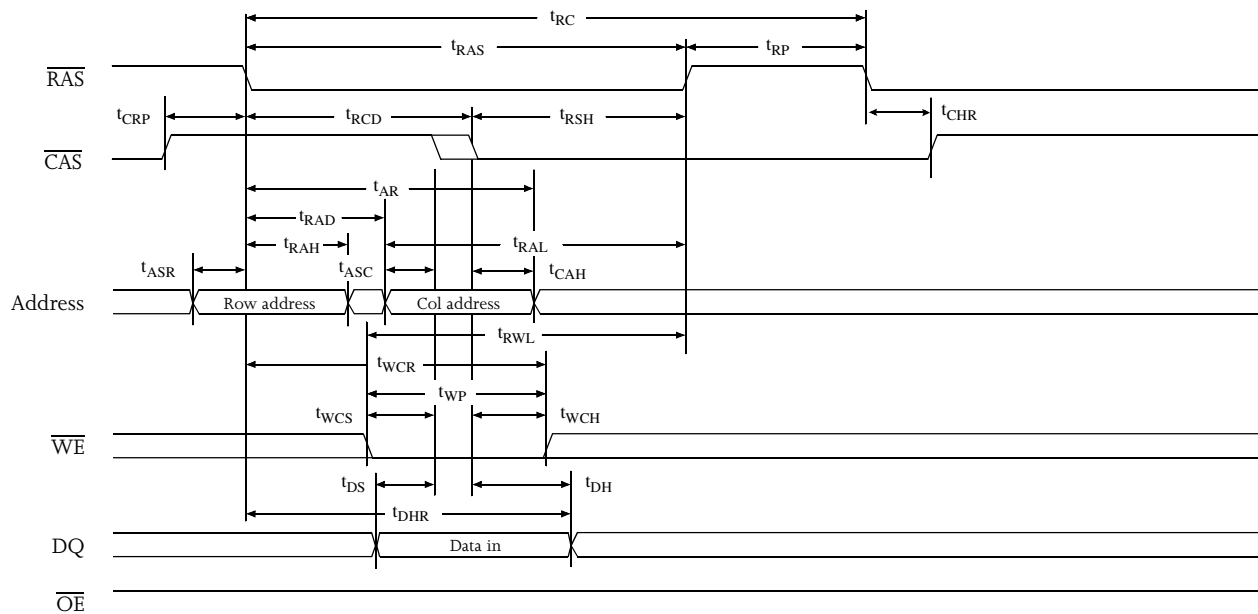




### Hidden refresh waveform (read)

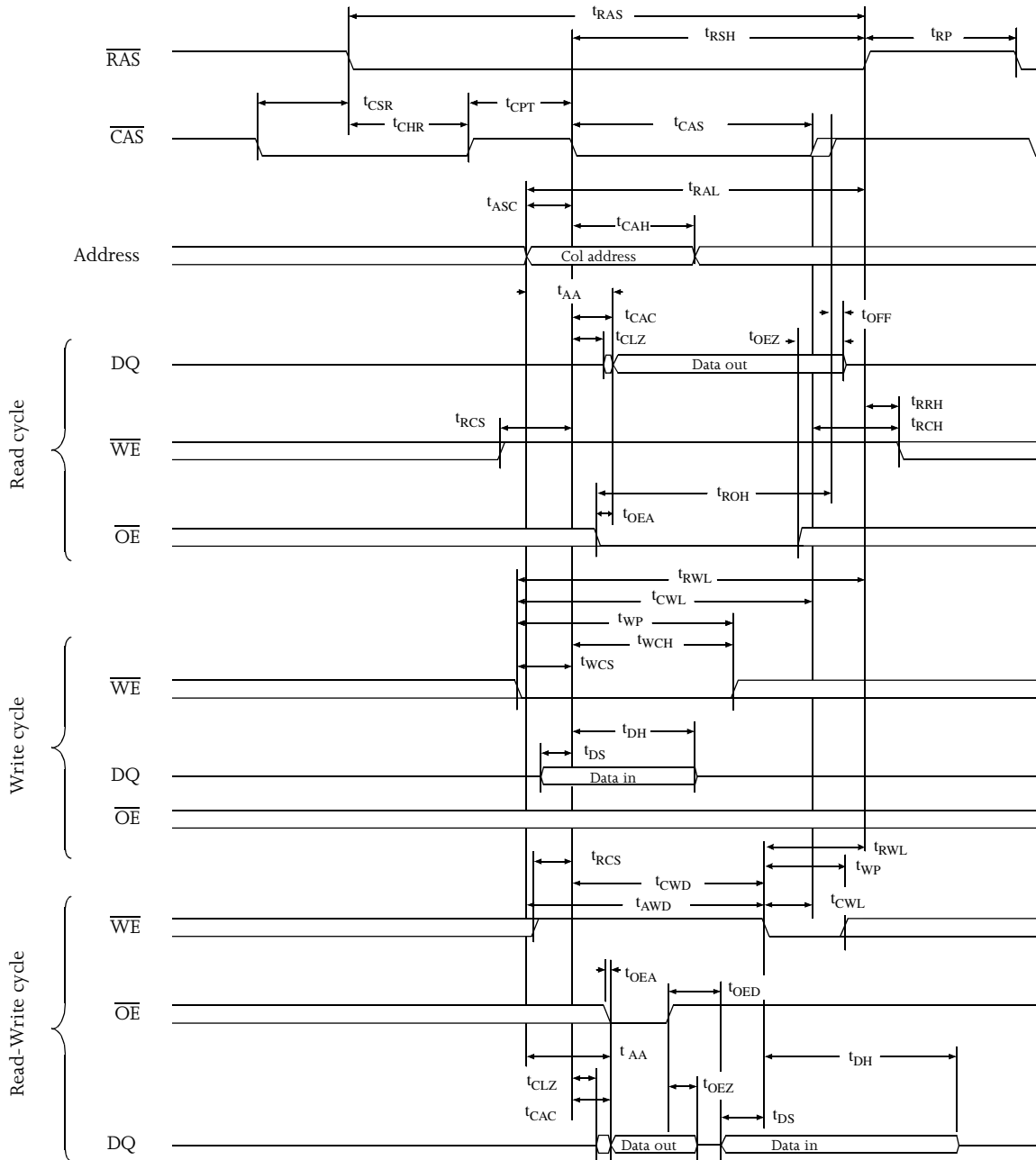


### Hidden refresh waveform (write)





CAS before RAS refresh counter test waveform





## Capacitance <sup>15</sup>

 $f = 1 \text{ MHz}, T_a = \text{Room temperature}$ 

| Parameter         | Symbol    | Signals  | Test conditions         | Max | Unit |
|-------------------|-----------|--|-------------------------|-----|------|
| Input capacitance | $C_{IN1}$ | A0 to A10  | $V_{in} = 0V$           | 5   | pF   |
|                   | $C_{IN2}$ | $\overline{RAS}, \overline{CAS}, \overline{WE}, \overline{OE}$ | $V_{in} = 0V$           | 7   | pF   |
| DQ capacitance    | $C_{DQ}$  | DQ0 to DQ3   | $V_{in} = V_{out} = 0V$ | 7   | pF   |

## AS4C4M4E1 ordering information

| Package \ $\overline{RAS}$ access time |    | 50 ns          | 60 ns          |
|--|----|----------------|----------------|
| Plastic SOJ, 300 mil, 24/26-pin        | 5V | AS4C4M4E1-50JC | AS4C4M4E1-60JC |
|  |    | AS4C4M4E1-50JI | AS4C4M4E1-60JI |
| Plastic TSOP, 300 mil, 24/26-pin       | 5V | AS4C4M4E1-50TC | AS4C4M4E1-60TC |
|  |    | AS4C4M4E1-50TI | AS4C4M4E1-60TI |

## AS4C4M4E1 family part numbering system

| AS4         | C           | 4M4  | E1            | -XX                          | X   | X   |
|-------------|-------------|------|---------------|------------------------------|---|---|
| DRAM prefix | C = 5V CMOS | 4M×4 | E1=2K refresh | $\overline{RAS}$ access time | Package:<br>J = SOJ 300 mil, 24/26<br>T = TSOP 300 mil, 24/26 | Temperature range<br>C=Commercial, 0°C to 70°C<br>I=Industrial, -40°C to 85°C |