# 11 Electrical Data

The following sections describe recommended electrical connections for the $Am5_X86$ microprocessors and electrical specifications.

## 11.1 Power and Grounding

### 11.1.1 Power Connections

$Am5_X86$ microprocessors with 16 Kbytes of cache have modest power requirements. However, the high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean, on-chip power distribution at high frequency, 23 $V_{CC}$ pins and 28 $V_{SS}$ pins feed the microprocessor in the 168-pin PGA package. The 208-pin SQFP package includes 53 $V_{CC}$ pins and 38 $V_{SS}$ pins.

Power and ground connections must be made to all external $V_{CC}$ and $V_{SS}$ pins of the microprocessors. On a circuit board, all $V_{CC}$ pins must connect to a $V_{CC}$ plane. Likewise, all $V_{SS}$ pins must connect to a common GND plane.

The $Am5_X86$ microprocessor family requires only 3.3 V as input power. Unlike other 3-V processors, the $Am5_X86$ microprocessor family does not require a $V_{CC5}$ input of 5 V to indicate the presence of 5-V I/O devices on the system motherboard. For socket compatibility, this pin is INC, allowing the $Am5_X86$ CPU to operate in 3-V sockets in systems that use 5-V I/O.

### 11.1.2 Power Decoupling Recommendations

Liberal decoupling capacitance should be placed near the microprocessor. The microprocessor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the microprocessor and the decoupling capacitors. Capacitors designed specifically for use with PGA packages are commercially available.

### 11.1.3 Other Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. Active Low inputs should be connected to $V_{CC}$ through a pull-up resistor. Pull-ups in the range of 20 KΩ are recommended. Active High inputs should be connected to GND.

## ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias . . . – 65°C to +110°C
Storage Temperature . . . . . – 65°C to +150°C
Voltage on any pin
with respect to ground . . . . . – 0.5 V to $V_{CC}$ +2.6 V
Supply voltage with
respect to $V_{SS}$ . . . . . – 0.5 V to +4.6 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices

$T_{CASE}$ . . . . . 0°C to 85°C
$V_{CC}$ . . . . . 3.3 V ±0.3 V

*Operating Ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges

$V_{CC}$ = 3.3 V ± 0.3 V; $T_{CASE}$ = 0°C to + 85°C

| Symbol | Parameter | Preliminary Info | | Notes |
|---|---|---|---|---|
| | | Min | Max | |
| $V_{IL}$ | Input Low Voltage | – 0.3 V | +0.8 V | |
| $V_{IH}$ | Input High Voltage | 2.0 V | $V_{CC}$ + 2.4 V | |
| $V_{OL}$ | Output Low Voltage | | 0.45 V | Note 1 |
| $V_{OH}$ | Output High Voltage | 2.4 V | | Note 2 |
| $I_{CC}$ | Power Supply Current: 133 MHz | | 931 mA | Typical supply current: 825 mA @ 133 MHz. Inputs at rails, outputs unloaded. |
| $I_{CCSTOPGRANT}$ or $I_{CCAUTOHALT}$ | Input Current in Stop Grant or Auto Halt mode 133 MHz | | 93 mA | Typical supply current for Stop Grant or Auto Halt mode: 50 mA @ 133 MHz . |
| $I_{CCSTPCLK}$ | Input Current in Stop Clock mode | | 5 mA | Typical supply current in Stop Clock mode is 600 µA. |
| $I_{LI}$ | Input Leakage Current | | ±15 µA | Note 3 |
| $I_{IH}$ | Input Leakage Current | | 200 µA | Note 4 |
| $I_{IL}$ | Input Leakage Current | | – 400 µA | Note 5 |
| $I_{LO}$ | Output Leakage Current | | ±15 µA | |
| $C_{IN}$ | Input Capacitance | | 10 pF | $F_C$ = 1 MHz (Note 6) |
| $C_O$ | I/O or Output Capacitance | | 14 pF | $F_C$ = 1 MHz (Note 6) |
| $C_{CLK}$ | CLK Capacitance | | 12 pF | $F_C$ = 1 MHz (Note 6) |

***Notes:***

1. *This parameter is measured at: Address, Data, $\overline{BE3}$–$\overline{BE0}$ = 4.0 mA; Definition, Control = 5.0 mA*
2. *This parameter is measured at: Address, Data, $\overline{BE3}$–$\overline{BE0}$ = –1.0 mA; Definition, Control = –0.9 mA*
3. *This parameter is for inputs without internal pull-ups or pull-downs and $0 \leq V_{IN} \leq V_{CC}$.*
4. *This parameter is for inputs with internal pull-downs and $V_{IH}$ = 2.4 V.*
5. *This parameter is for inputs with internal pull-ups and $V_{IL}$ = 0.45 V.*
6. *Not 100% tested.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

The AC specifications, provided in the AC characteristics table, consist of output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the rising edge of the CLK signal. AC specifications measurement is defined by Figure 39. All timings are referenced to 1.5 V unless otherwise specified. Am5$_X$86 microprocessor output delays are specified with minimum and maximum limits, measured as shown. The minimum microprocessor delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct microprocessor operation.

### 33-MHz bus (133-MHz operating frequency)

$V_{CC}$ = 3.3 V ±0.3 V; $T_{CASE}$ = 0°C to + 85°C; $C_L$ = 50 pF unless otherwise specified

| Symbol | Parameter | Preliminary Info Min | Preliminary Info Max | Unit | Figure | Notes |
|---|---|---|---|---|---|---|
| | Frequency | 8 | 33 | MHz | | Note 2 |
| $t_1$ | CLK Period | 30 | 125 | ns | 39 | |
| $t_{1a}$ | CLK Period Stability | | 0.1% | Δ | | Adjacent Clocks Notes 3 and 4 |
| $t_2$ | CLK High Time at 2 V | 11 | | ns | 39 | Note 3 |
| $t_3$ | CLK Low Time at 0.8 V | 11 | | ns | 39 | Note 3 |
| $t_4$ | CLK Fall Time (2 V–0.8 V) | | 3 | ns | 39 | Note 3 |
| $t_5$ | CLK Rise Time (0.8 V–2 V) | | 3 | ns | 39 | Note 3 |
| $t_6$ | A31–A2, PWT, PCD, $\overline{BE3}$–$\overline{BE0}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{CACHE}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA, $\overline{SMIACT}$, $\overline{HITM}$ Valid Delay | 3 | 14 | ns | 40 | Note 5 |
| $t_7$ | A31–A2, PWT, PCD, $\overline{BE3}$–$\overline{BE0}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{CACHE}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$ Float Delay | 3 | 20 | ns | 41 | Note 3 |
| $t_8$ | $\overline{PCHK}$ Valid Delay | 3 | 14 | ns | 42 | |
| $t_{8a}$ | $\overline{BLAST}$, $\overline{PLOCK}$, Valid Delay | 3 | 14 | ns | 40 | |
| $t_9$ | $\overline{BLAST}$, $\overline{PLOCK}$, Float Delay | 3 | 20 | ns | 41 | Note 3 |
| $t_{10}$ | D31–D0, DP3–DP0 Write Data Valid Delay | 3 | 14 | ns | 40 | |
| $t_{11}$ | D31–D0, DP3–DP0 Write Data Float Delay | 3 | 20 | ns | 41 | Note 3 |
| $t_{12}$ | $\overline{EADS}$, INV, WB/$\overline{WT}$ Setup Time | 5 | | ns | 43 | |
| $t_{13}$ | $\overline{EADS}$, INV, WB/$\overline{WT}$ Hold Time | 3 | | ns | 43 | |
| $t_{14}$ | $\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time | 5 | | ns | 43 | |
| $t_{15}$ | $\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time | 3 | | ns | 43 | |
| $t_{16}$ | $\overline{RDY}$, $\overline{BRDY}$ Setup Time | 5 | | ns | 44 | |
| $t_{17}$ | $\overline{RDY}$, $\overline{BRDY}$ Hold Time | 3 | | ns | 44 | |
| $t_{18}$ | HOLD, AHOLD Setup Time | 6 | | ns | 43 | |
| $t_{18a}$ | $\overline{BOFF}$ Setup Time | 7 | | ns | 43 | |
| $t_{19}$ | HOLD, AHOLD, $\overline{BOFF}$ Hold Time | 3 | | ns | 43 | |
| $t_{20}$ | RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$, $\overline{STPCLK}$, SRESET, $\overline{SMI}$ Setup Time | 5 | | ns | 43 | Note 5 |
| $t_{21}$ | RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$, $\overline{STPCLK}$, SRESET, $\overline{SMI}$ Hold Time | 3 | | ns | 43 | Note 5 |
| $t_{22}$ | D31–D0, DP3–DP0, A31–A4 Read Setup Time | 5 | | ns | 43, 44 | |
| $t_{23}$ | D32–D0, DP3–DP0, A31–A4 Read Hold Time | 3 | | ns | 43, 44 | |

***Notes:***

1. *Specifications assume $C_L$ = 50 pF. I/O Buffer model must be used to determine delays due to loading (trace and component). First Order I/O buffer models for the processor are available.*
2. *0-MHz operation guaranteed during stop clock operation.*
3. *Not 100% tested. Guaranteed by design characterization.*
4. *For faster transitions (>0.1% between adjacent clocks), use the Stop Clock protocol to switch operating frequency.*
5. *All timings are referenced at 1.5 V (as illustrated in the listed figures) unless otherwise noted.*

## Am5$_X$86 Microprocessor AC Characteristics for Boundary Scan Test Signals at 25 MHz

$V_{CC}$ = 3.3 V ±0.3 V; $T_{CASE}$ = 0°C to +85°C; $C_L$ = 50 pF unless otherwise specified

| Symbol | Parameter | Preliminary Info | | Unit | Figure | Notes |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| $t_{24}$ | TCK Frequency | | 25 | MHz | | 1x Clock |
| $t_{25}$ | TCK Period | 40 | | ns | 45, 46 | Note 1 |
| $t_{26}$ | TCK High Time at 2 V | 10 | | ns | 45 | |
| $t_{27}$ | TCK Low Time at 0.8 V | 10 | | ns | 45 | |
| $t_{28}$ | TCK Rise Time (0.8 V–2 V) | | 4 | ns | 45 | Note 2 |
| $t_{29}$ | TCK Fall Time (2 V–0.8 V) | | 4 | ns | 45 | Note 2 |
| $t_{30}$ | TDI, TMS Setup Time | 8 | | ns | 46 | Note 3 |
| $t_{31}$ | TDI, TMS Hold Time | 7 | | ns | 46 | Note 3 |
| $t_{32}$ | TDO Valid Delay | 3 | 25 | ns | 46 | Note 3 |
| $t_{33}$ | TDO Float Delay | | 36 | ns | 46 | Note 3 |
| $t_{34}$ | All Outputs (Non-Test) Valid Delay | 3 | 25 | ns | 46 | Note 3 |
| $t_{35}$ | All Outputs (Non-Test) Float Delay | | 30 | ns | 46 | Note 3 |
| $t_{36}$ | All Inputs (Non-Test) Setup Delay | 8 | | ns | 46 | Note 3 |
| $t_{37}$ | All Inputs (Non-Test) Hold Time | 7 | | ns | 46 | Note 3 |

***Notes:***

1. *TCK period ≥ CLK period.*
2. *Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.*
3. *Parameter measured from TCK.*

**Key to Switching Waveforms**

| Waveform | Inputs | Outputs |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from H to L | Will change from H to L |
| | May change from L to H | Will change from L to H |
| | Don't care; any change permitted | Changing; state unknown |
| | Does not apply | Center line is High-impedance "Off" state |

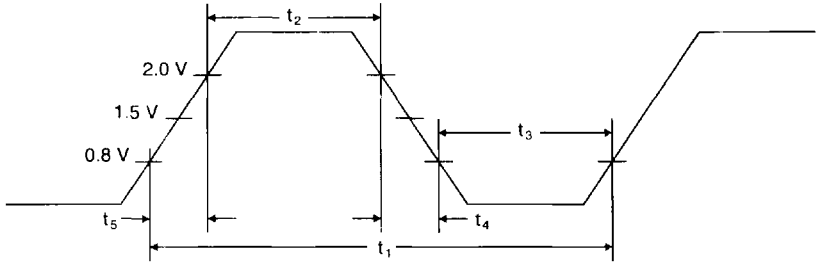


**Figure 39. CLK Waveforms**

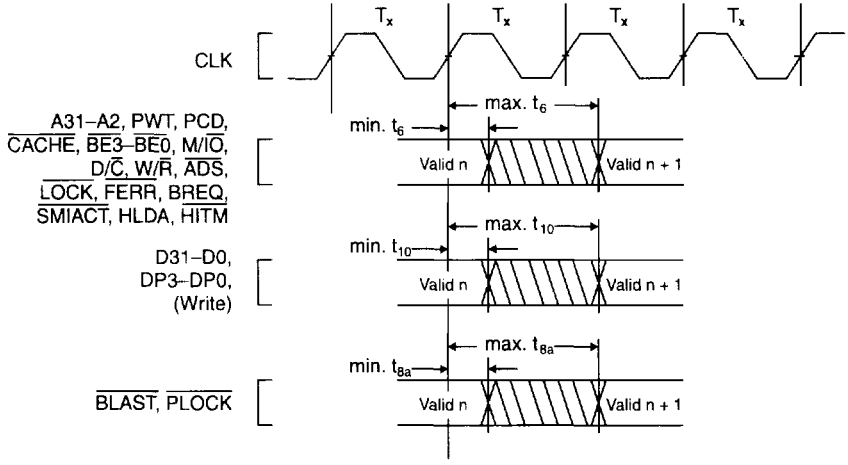


**Figure 40. Output Valid Delay Timing**

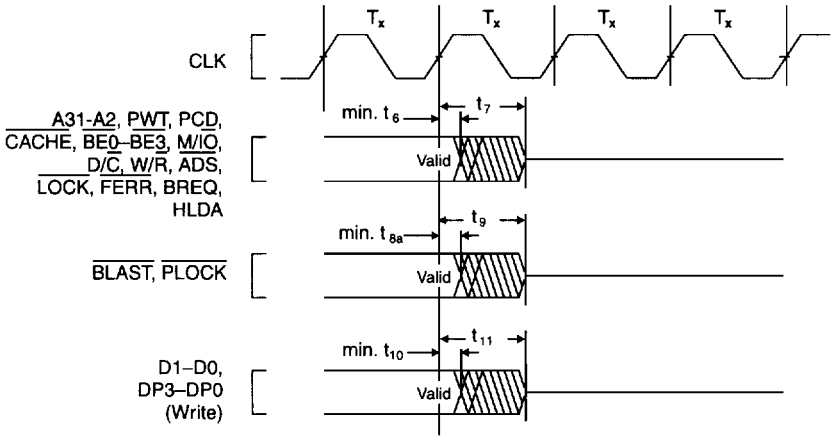


**Figure 41. Maximum Float Delay Timing**

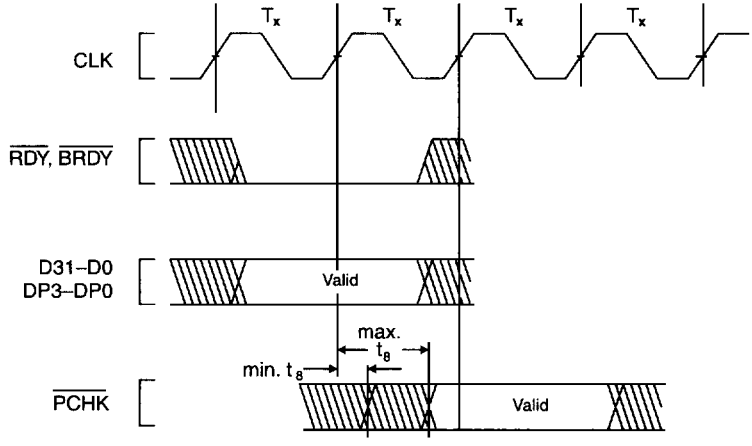


**Figure 42. PCHK Valid Delay Timing**

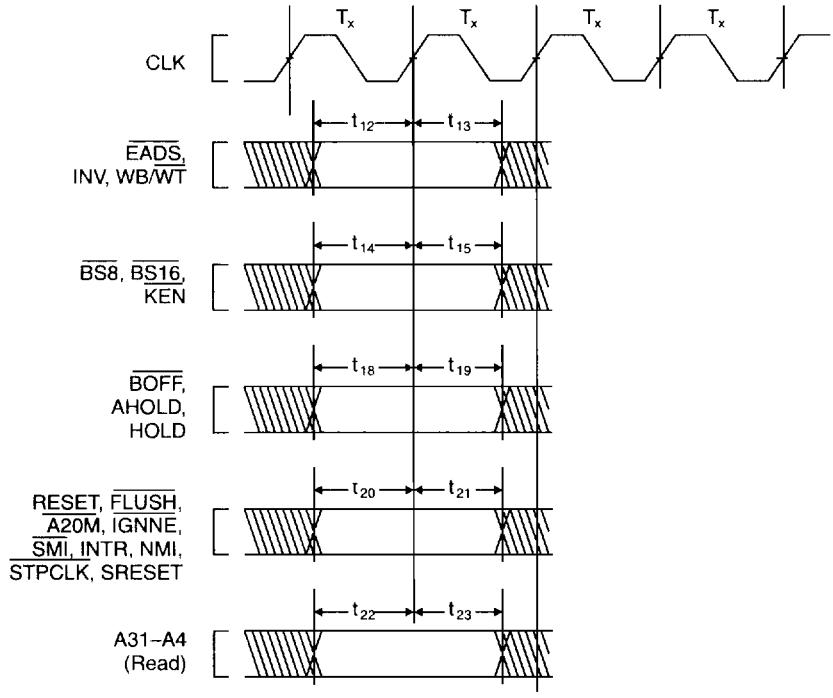


**Figure 43. Input Setup and Hold Timing**

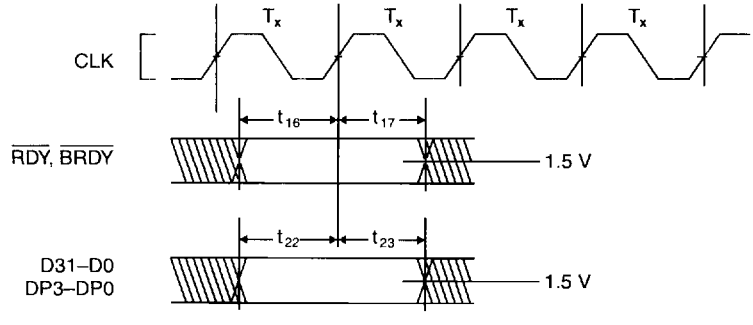


**Figure 44. RDY and BRDY Input Setup and Hold Timing**

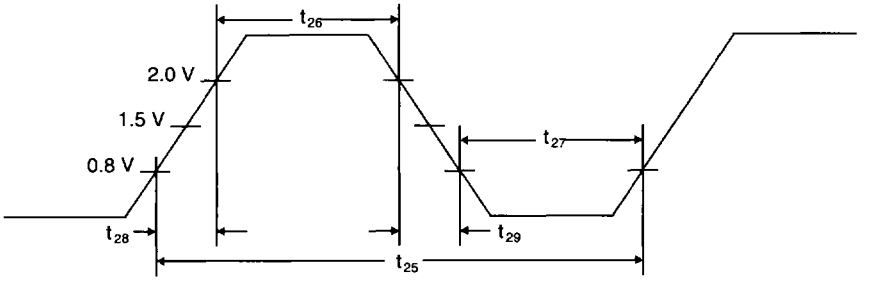


Figure 45. TCK Waveforms

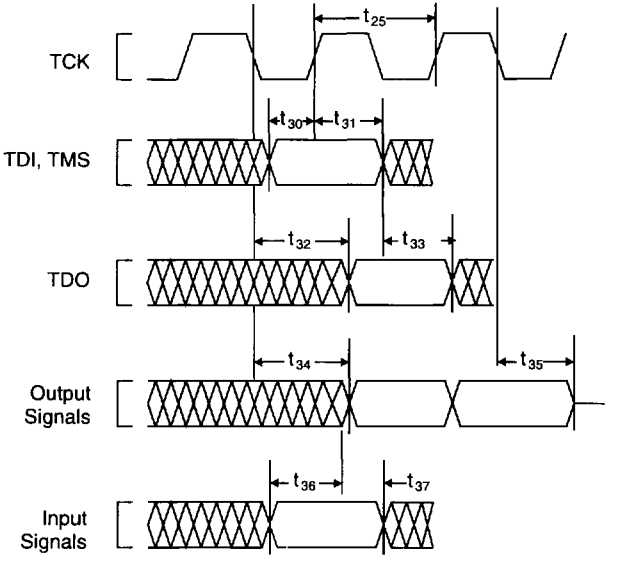


Figure 46. Test Signal Timing Diagram