74AUP2G80

Low-power dual D-type flip-flop; positive-edge trigger

Rev. 04 — 2 June 2008　　　　　　　　　　　　　　　　**Product data sheet**

1. General description

The 74AUP2G80 provides the dual positive-edge triggered D-type flip-flop. Information on the data input is transferred to the $\overline{Q}$ output on the LOW-to-HIGH transition of the clock pulse. The input pin D must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}.
The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features

■ Wide supply voltage range from 0.8 V to 3.6 V
■ High noise immunity
■ Complies with JEDEC standards:
　◆ JESD8-12 (0.8 V to 1.3 V)
　◆ JESD8-11 (0.9 V to 1.65 V)
　◆ JESD8-7 (1.2 V to 1.95 V)
　◆ JESD8-5 (1.8 V to 2.7 V)
　◆ JESD8-B (2.7 V to 3.6 V)
■ ESD protection:
　◆ HBM JESD22-A114E Class 3A exceeds 5 000 V
　◆ MM JESD22-A115-A exceeds 200 V
　◆ CDM JESD22-C101C exceeds 1 000 V
■ Low static power consumption; I_{CC} = 0.9 μA (maximum)
■ Latch-up performance exceeds 100 mA per JESD78 Class II
■ Inputs accept voltages up to 3.6 V
■ Low noise overshoot and undershoot < 10 % of V_{CC}
■ I_{OFF} circuitry provides partial Power-down mode operation
■ Multiple package options
■ Specified from −40 °C to +85 °C and −40 °C to +125 °C

NXP founded by Philips

3. Ordering information

Table 1.   Ordering information

Type number	Package				
	Temperature range	**Name**	**Description**		**Version**
74AUP2G80DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
74AUP2G80GT	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $1 \times 1.95 \times 0.5$ mm		SOT833-1
74AUP2G80GD	−40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body $3 \times 2 \times 0.5$ mm		SOT996-2
74AUP2G80GM	−40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body $1.6 \times 1.6 \times 0.5$ mm		SOT902-1

4. Marking

Table 2.   Marking codes

Type number	Marking code
74AUP2G80DC	p80
74AUP2G80GT	p80
74AUP2G80GD	p80
74AUP2G80GM	p80

5. Functional diagram
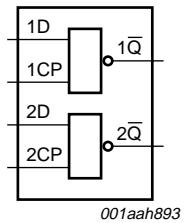
Fig 1.   Logic symbol
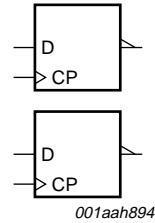
Fig 2.   IEC logic symbol
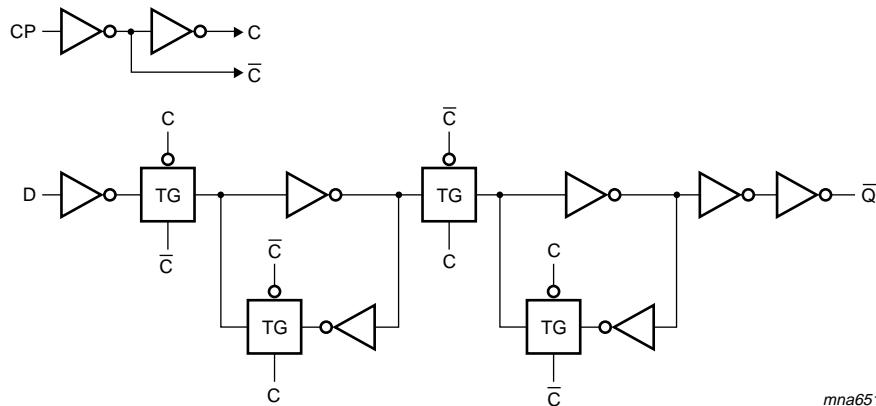
Fig 3.   Logic diagram (one flip-flop)

6. Pinning information

6.1 Pinning
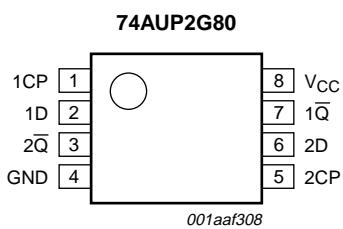
Fig 4.   Pin configuration SOT765-1 (VSSOP8)

Transparent top view

Fig 5.   Pin configuration SOT833-1 (XSON8)

Fig 6. Pin configuration SOT996-2 (XSON8U)

Fig 7. Pin configuration SOT902-1 (XQFN8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1 and SOT996-2	**SOT902-1**	
1CP, 2CP	1, 5	7, 3	clock input
1D, 2D	2, 6	6, 2	data input
GND	4	4	ground (0 V)
$1\overline{Q}$, $2\overline{Q}$	7, 3	1, 5	data output
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input		Output
nCP	**nD**	**n$\overline{Q}$**
↑	L	H
↑	H	L
L	X	$\overline{q}$

[1] H = HIGH voltage level;

L = LOW voltage level;

↑ = LOW-to-HIGH CP transition;

X = don't care;

$\overline{q}$ = lower case letter indicates the state of referenced input, one setup time prior to the LOW-to-HIGH CP transition.

8. Limiting values

Table 5.   Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		−50	-	mA
V_I	input voltage		[1] −0.5		+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode and Power-down mode	[1] −0.5		+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}		-	±20	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			−50	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = −40$ °C to +125 °C	[2]	-	250	mW

[1]   The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]   For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8, XSON8U and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6.   Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	-	200	ns/V

74AUP2G80_4

Product data sheet

Rev. 04 — 2 June 2008

5 of 20

10. Static characteristics

Table 7.   Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	$0.75 \times V_{CC}$	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V	[1] -	-	40	μA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	0.6	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.3	-	pF

74AUP2G80_4

Product data sheet **Rev. 04 — 2 June 2008** 6 of 20

Table 7. **Static characteristics** *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 0.9 V 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	$0.7 \times V_{CC}$	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	[1] -	-	50	µA

Table 7.   Static characteristics *…continued*
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	$0.75 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V	$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	$0.25 \times V_{CC}$	V
		V_{CC} = 0.9 V 1.95 V	-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 0.8 V to 3.6 V	$V_{CC} - 0.11$	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	$0.6 \times V_{CC}$	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	0.93	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.17	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.77	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.67	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.40	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	$0.33 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V	[1] -	-	75	μA

[1]   One input at V_{CC} − 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = −40 °C to +125 °C				Unit
				Min	Typ[1]	Max	Min (85 °C)	Max (85 °C)	Min (125 °C)	Max (125 °C)	
C_L = 5 pF											
t_{pd}	propagation delay	nCP to n$\overline{Q}$; see Figure 8	[2]								
		V_{CC} = 0.8 V		-	20.9	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		2.9	6.0	12.9	2.6	14.3	2.6	15.7	ns
		V_{CC} = 1.4 V to 1.6 V		1.9	4.2	7.6	2.0	8.9	2.0	9.8	ns
		V_{CC} = 1.65 V to 1.95 V		1.7	3.4	5.9	1.6	7.0	1.6	7.7	ns
		V_{CC} = 2.3 V to 2.7 V		1.4	2.6	4.3	1.2	5.6	1.2	6.2	ns
		V_{CC} = 3.0 V to 3.6 V		1.2	2.2	3.6	1.0	4.4	1.0	4.8	ns
f_{max}	maximum frequency	nCP; see Figure 9									
		V_{CC} = 0.8 V		-	53	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V		-	203	-	170	-	170	-	MHz
		V_{CC} = 1.4 V to 1.6 V		-	347	-	310	-	300	-	MHz
		V_{CC} = 1.65 V to 1.95 V		-	435	-	400	-	390	-	MHz
		V_{CC} = 2.3 V to 2.7 V		-	550	-	490	-	480	-	MHz
		V_{CC} = 3.0 V to 3.6 V		-	619	-	550	-	510	-	MHz
C_L = 10 pF											
t_{pd}	propagation delay	nCP to n$\overline{Q}$; see Figure 8	[2]								
		V_{CC} = 0.8 V		-	24.6	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V		3.3	6.9	14.9	3.0	16.5	3.0	18.2	ns
		V_{CC} = 1.4 V to 1.6 V		2.6	4.8	8.8	2.3	10.3	2.3	11.3	ns
		V_{CC} = 1.65 V to 1.95 V		2.3	3.9	6.8	2.0	8.1	2.0	8.9	ns
		V_{CC} = 2.3 V to 2.7 V		1.9	3.1	5.1	1.7	6.3	1.7	6.9	ns
		V_{CC} = 3.0 V to 3.6 V		1.8	2.7	4.4	1.4	4.9	1.4	5.4	ns
f_{max}	maximum frequency	nCP; see Figure 9									
		V_{CC} = 0.8 V		-	52	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V		-	192	-	150	-	150	-	MHz
		V_{CC} = 1.4 V to 1.6 V		-	324	-	280	-	230	-	MHz
		V_{CC} = 1.65 V to 1.95 V		-	421	-	310	-	250	-	MHz
		V_{CC} = 2.3 V to 2.7 V		-	486	-	370	-	360	-	MHz
		V_{CC} = 3.0 V to 3.6 V		-	550	-	410	-	360	-	MHz

Table 8. **Dynamic characteristics** …continued

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +125 °C				Unit
			Min	Typ[1]	Max	Min (85 °C)	Max (85 °C)	Min (125 °C)	Max (125 °C)	
C_L = 15 pF										
t_{pd}	propagation delay	nCP to n$\overline{Q}$; see Figure 8 [2]								
		V_{CC} = 0.8 V	-	28.2	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.0	7.6	16.7	3.4	18.6	3.4	20.5	ns
		V_{CC} = 1.4 V to 1.6 V	3.0	5.3	9.8	2.6	11.5	2.6	12.7	ns
		V_{CC} = 1.65 V to 1.95 V	2.6	4.4	7.6	2.3	9.1	2.3	10.0	ns
		V_{CC} = 2.3 V to 2.7 V	2.2	3.5	5.7	2.0	6.9	2.0	7.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.9	3.1	5.0	1.8	5.5	1.8	6.1	ns
f_{max}	maximum frequency	nCP; see Figure 9								
		V_{CC} = 0.8 V	-	50	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C_L = 30 pF										
t_{pd}	propagation delay	nCP to n$\overline{Q}$; see Figure 8 [2]								
		V_{CC} = 0.8 V	-	38.8	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.9	9.8	20.7	4.4	24.7	4.4	27.2	ns
		V_{CC} = 1.4 V to 1.6 V	4.0	6.8	12.7	3.5	15.0	3.5	16.5	ns
		V_{CC} = 1.65 V to 1.95 V	3.5	5.6	9.9	2.2	11.9	2.2	13.1	ns
		V_{CC} = 2.3 V to 2.7 V	3.1	4.5	7.5	2.8	9.3	2.8	10.2	ns
		V_{CC} = 3.0 V to 3.6 V	2.9	4.1	6.4	2.7	7.5	2.7	8.3	ns
f_{max}	maximum frequency	nCP; see Figure 9								
		V_{CC} = 0.8 V	-	28	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
$t_{su(H)}$	set-up time HIGH	nD to nCP; see Figure 9								
		V_{CC} = 0.8 V	-	2.5	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	0.5	-	2.3	-	2.3	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.3	-	1.2	-	1.2	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.3	-	0.8	-	0.8	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.2	-	0.6	-	0.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.2	-	0.4	-	0.4	-	ns

74AUP2G80_4

Product data sheet Rev. 04 — 2 June 2008 10 of 20

Table 8.   **Dynamic characteristics** *…continued*

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +125 °C				Unit
			Min	Typ[1]	Max	Min (85 °C)	Max (85 °C)	Min (125 °C)	Max (125 °C)	
$t_{su(L)}$	set-up time LOW	nD to nCP; see Figure 9								
		V_{CC} = 0.8 V	-	1.7	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	0.3	-	1.9	-	1.9	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.2	-	1.3	-	1.3	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.2	-	1.1	-	1.1	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.3	-	0.8	-	0.8	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.3	-	0.7	-	0.7	-	ns
t_h	hold time	nD to nCP; see Figure 9								
		V_{CC} = 0.8 V	-	−2.1	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	−0.4	-	0.1	-	0.1	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	−0.3	-	0	-	0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	−0.2	-	0	-	0	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	−0.2	-	0	-	0	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	−0.3	-	0	-	0	-	ns
t_W	pulse width	nCP HIGH or LOW; see Figure 9								
		V_{CC} = 0.8 V	-	5.2	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	1.0	-	3.0	-	3.0	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.8	-	2.0	-	2.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.6	-	2.0	-	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.5	-	2.0	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.5	-	2.0	-	2.0	-	ns
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} [3]								
		V_{CC} = 0.8 V	-	1.8	-	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	1.8	-	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	1.9	-	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	2.0	-	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	2.4	-	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	2.9	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

    $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

    f_i = input frequency in MHz;

    f_o = output frequency in MHz;

    C_L = output load capacitance in pF;

    V_{CC} = supply voltage in V;

    N = number of inputs switching;

    $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms

Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. **The clock input (nCP) to output ($n\overline{Q}$) propagation delays**

Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
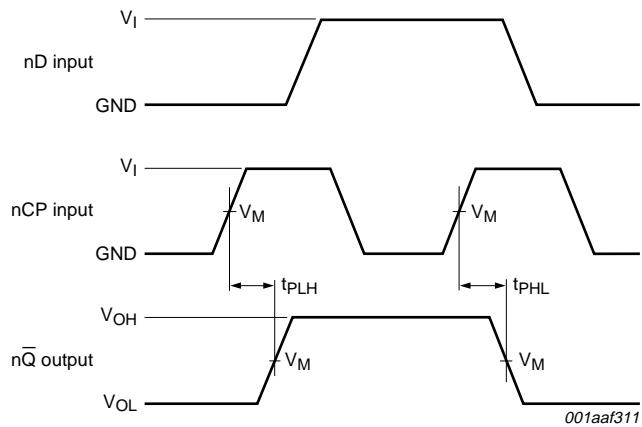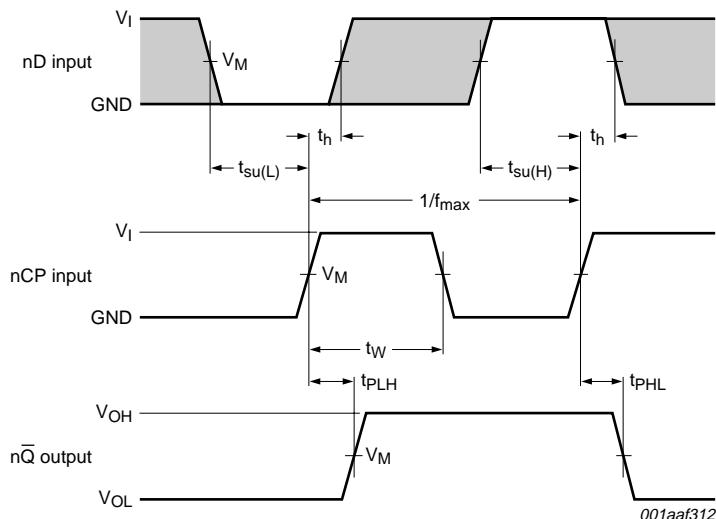
Fig 9. **The clock input (nCP) to output ($n\overline{Q}$) propagation delays, clock pulse width, nD to nCP setup and hold times and the nCP maximum frequency**

Table 9. **Measurement points**

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns
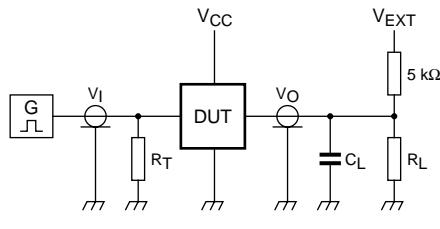
Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Load circuit for measuring switching times

Table 10. Test data

Supply voltage	Load			V_{EXT}		
V_{CC}	C_L	R_L [1]		t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ		open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times R_L = 5 kΩ.

For measuring propagation delays, setup and hold times and pulse width R_L = 1 MΩ.

74AUP2G80_4

Product data sheet

Rev. 04 — 2 June 2008

13 of 20

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm   **SOT765-1**
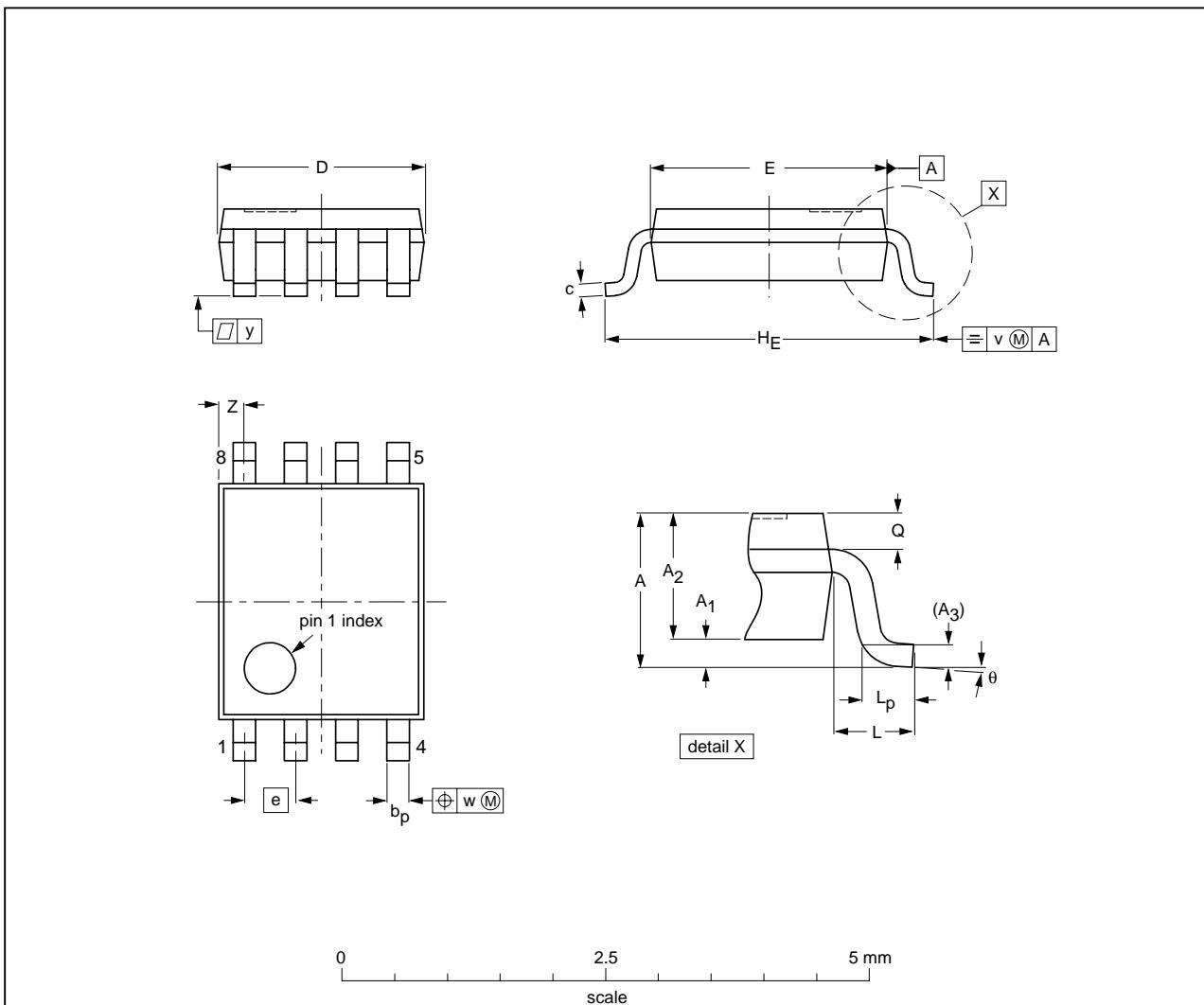
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 11. Package outline SOT765-1 (VSSOP8)

74AUP2G80_4

Product data sheet   Rev. 04 — 2 June 2008   **14 of 20**

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm   SOT833-1

DIMENSIONS (mm are the original dimensions)

UNIT	A[1] max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07
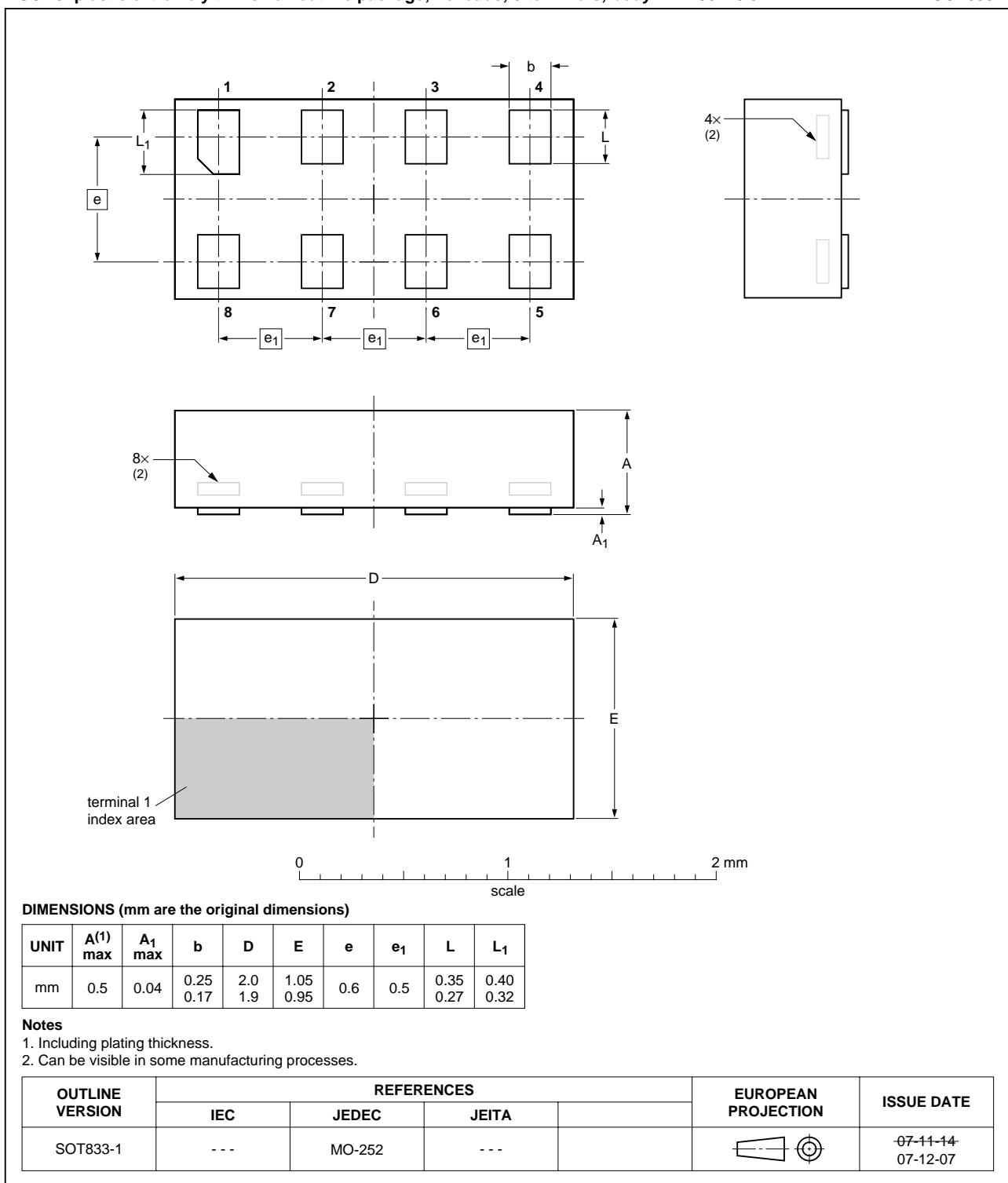
Fig 12. Package outline SOT833-1 (XSON8)

**XSON8U: plastic extremely thin small outline package; no leads;
8 terminals; UTLP based; body 3 x 2 x 0.5 mm**

SOT996-2

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A$_1$	b	D	E	e	e$_1$	L	L$_1$	L$_2$	v	w	y	y$_1$
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT996-2	- - -		- - -		~~07-12-18~~ 07-12-21
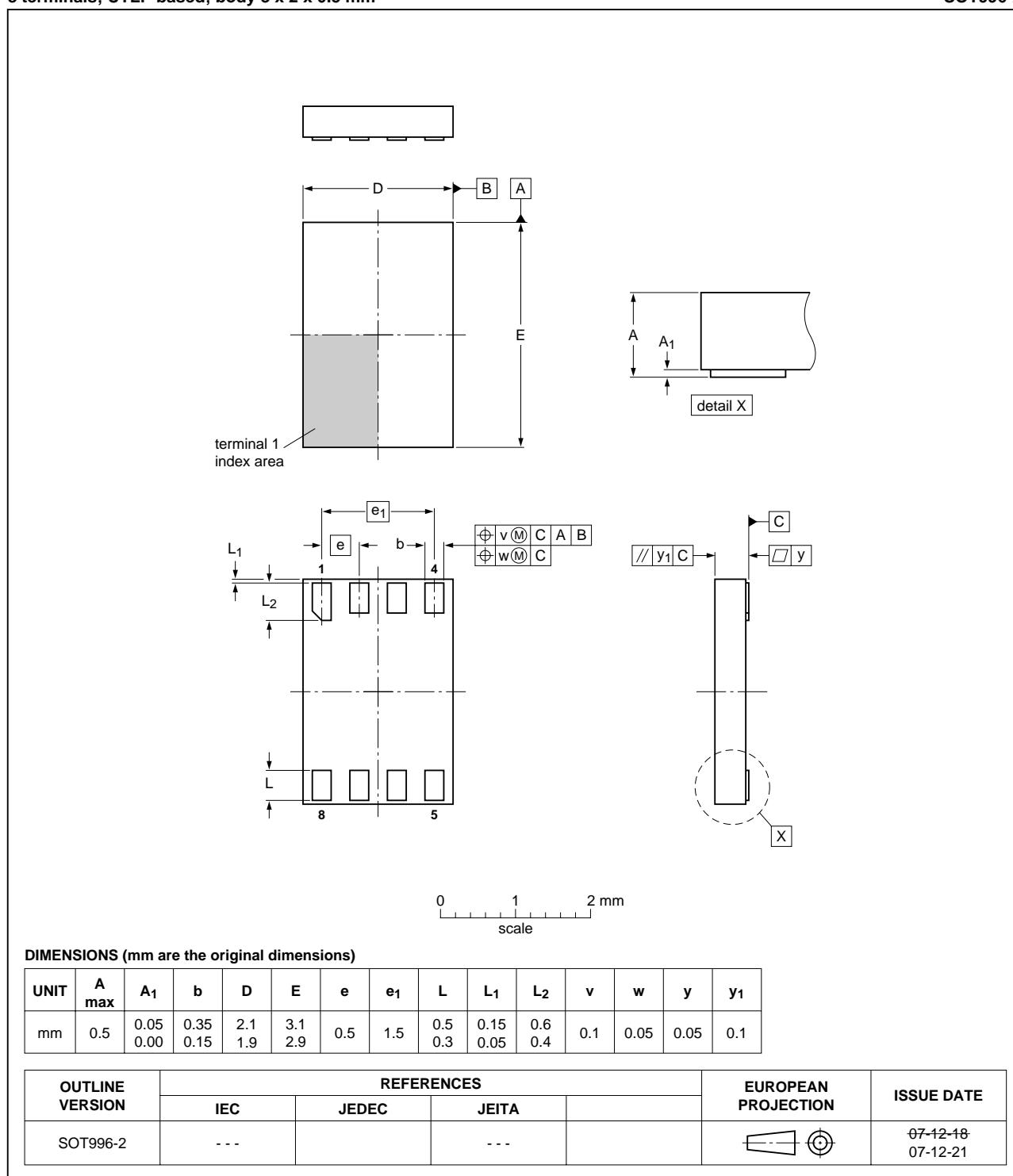
Fig 13. Package outline SOT996-2 (XSON8U)

**XQFN8U: plastic extremely thin quad flat package; no leads;
8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm**   SOT902-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT902-1	- - -	MO-255	- - -		05-11-25 07-11-14
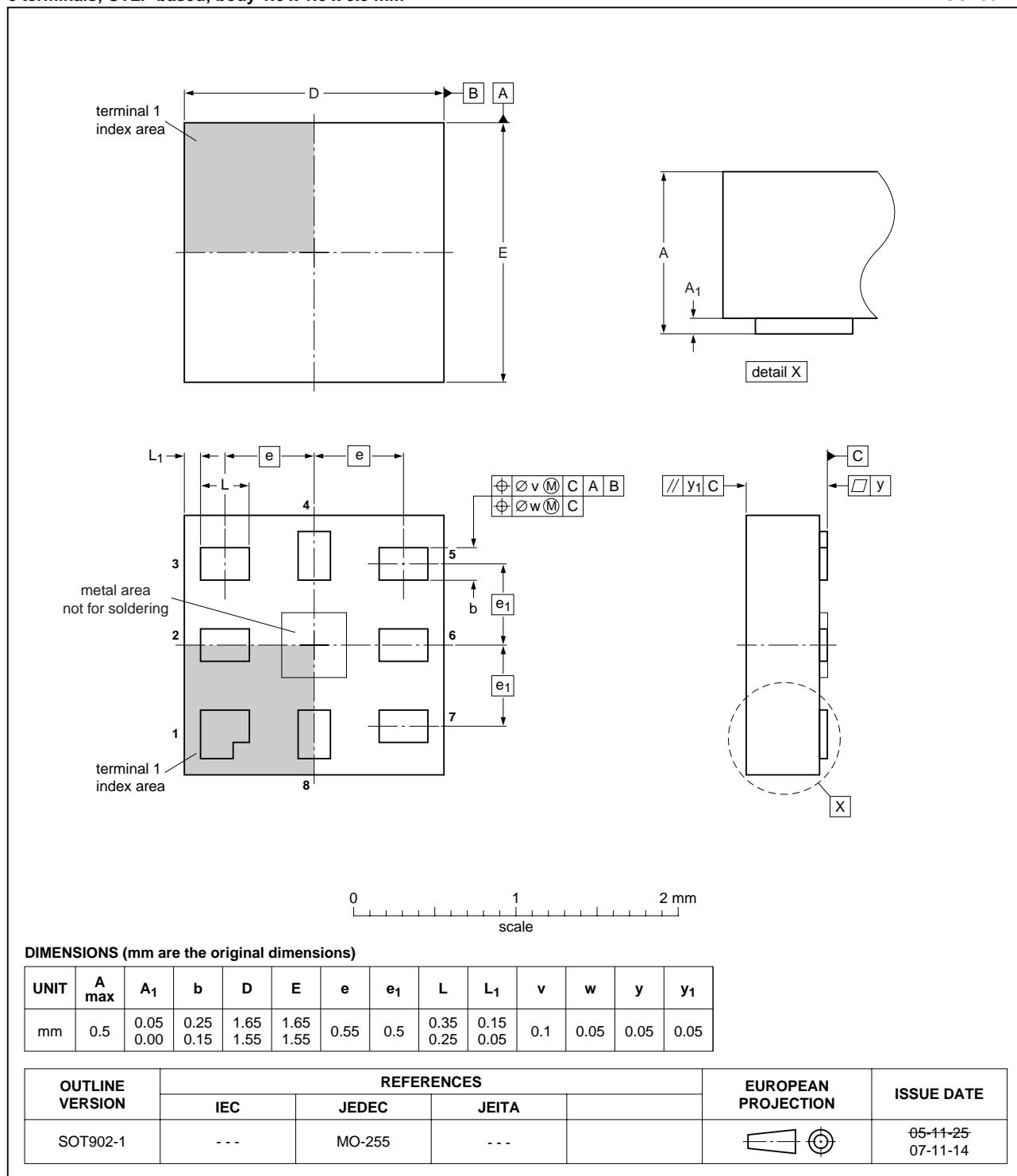
Fig 14. Package outline SOT902-1 (XQFN8U)

14. Abbreviations

Table 11.   Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G80_4	20080602	Product data sheet	-	74AUP2G80_3
Modifications:	• Added type number 74AUP2G80GD (XSON8U package)			
74AUP2G80_3	20080328	Product data sheet	-	74AUP2G80_2
74AUP2G80_2	20070801	Product data sheet	-	74AUP2G80_1
74AUP2G80_1	20060825	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

founded by

PHILIPS