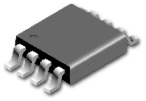
1.5A Very Low Input / Output Voltage Ultra Low Dropout Linear Regulator

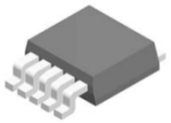
FEATURES

- Ultra Low Dropout Voltage
- Low Quiescent Current
- Excellent Line and Load Regulation
- Guaranteed Output Current of 1.5A
- Available in SOP-8, SOP-8-PP, TO-252-5L Packages
- Adjustable Output Voltage Down to 0.8V
- Logic Controlled Shutdown Option
- Over-Temperature/Over-Current Protection
- -40°C to 125°C Junction Temperature Range

SOP-8 / SOP-8-PP



TO252-5L



APPLICATIONS

- Motherboards and Graphic Cards
- Microprocessor Power Supplies
- Peripheral Cards
- Low Voltage Digital ICs
- High Efficiency Linear Regulators
- SMPS Post Regulators

DESCRIPSION

The TJ49150 is a series of 1.5A high performance ultra low dropout linear regulator ideal for powering core voltages of low-power microprocessors. The TJ49150 implements a dual supply configuration allowing for very low output impedance. The TJ49150 requires a bias input supply and a main input supply, allowing for very low input voltages on the main supply rail. The input supply operates from 1.4V to 5.5V and the bias supply requires between 3V and 5.5V for proper operation. The TJ49150 offers adjustable output voltages down to 0.8V. The TJ49150 is developed on a CMOS technology which allows low quiescent current operation independent of output current. This technology also allows the TJ49150 to operate under extremely low dropout conditions.

ORDERING INFORMATION

Device	Package
TJ49150GD	SOP-8
TJ49150GDP	SOP-8-PP
TJ49150GRS	TO-252-5L

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Input Supply Voltage (Survival)	V_{IN}	-0.3	6	V
Bias Supply Voltage (Survival)	V_{BIAS}	-0.3	6	V
Enable Input Voltage (Survival)	V_{EN}	-0.3	6	V
Output Voltage (Survival)	V_{OUT}	-0.3	V_{IN} +0.3	V
Lead Temperature (Soldering, 5 sec)	T_{SOL}		260	°C
Storage Temperature Range	T_{STG}	-65	150	°C

RECOMMENDED OPERATING RATINGS

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Input Supply Voltage	V_{IN}	1.3	5.5	V
Bias Supply Voltage	V_{BIAS}	3	5.5	V
Enable Input Voltage	V_{EN}	0	V_{BIAS}	V
Ambient Temperature Range	T_{AOPR}	-40	105	°C
Operating Junction Temperature Range	T_{JOPR}	-40	125	°C

THERMAL INFORMATION

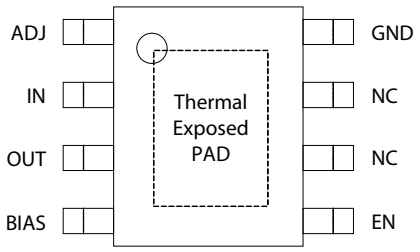
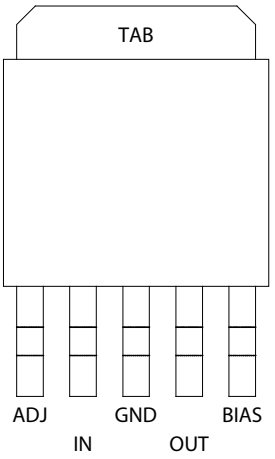
THERMAL METRIC	θ_{JC}	θ_{JA}	UNIT
Thermal Resistance (SOP-8) *			°C/W
Thermal Resistance (SOP-8-PP) *	15	75	°C/W
Thermal Resistance (TO-252-5L) *		68	°C/W

* Calculated from package in still air, mounted to minimum foot print(2.5mm x 3.0mm) PCB.

ORDERING INFORMATION

V_{OUT}	Package	Order No.	Description	Marking	Compliance	Status
ADJ	SOP-8	TJ49150GD	1.5A, Adjustable, Enable	TJ49150G	RoHS, Green	Contact Us
	SOP-8-PP	TJ49150GDP	1.5A, Adjustable, Enable	TJ49150G	RoHS, Green	Active
	TO-252 5L	TJ49150GRS	1.5A, Adjustable	TJ49150G	RoHS, Green	Contact Us

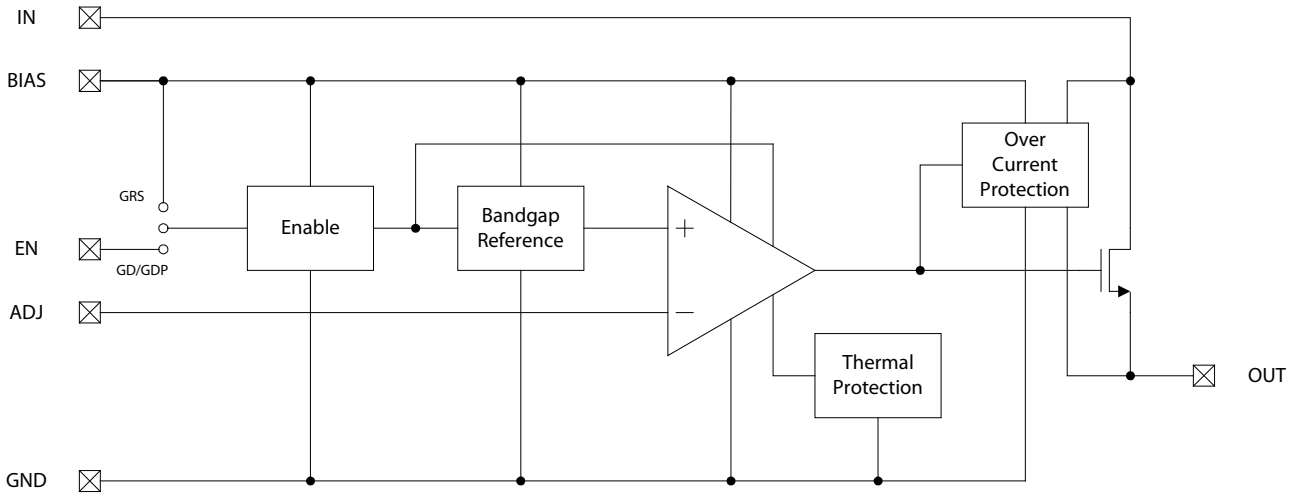
PIN CONFIGURATION

SOP-8 / SOP-8-PP	TO-252-5L
	

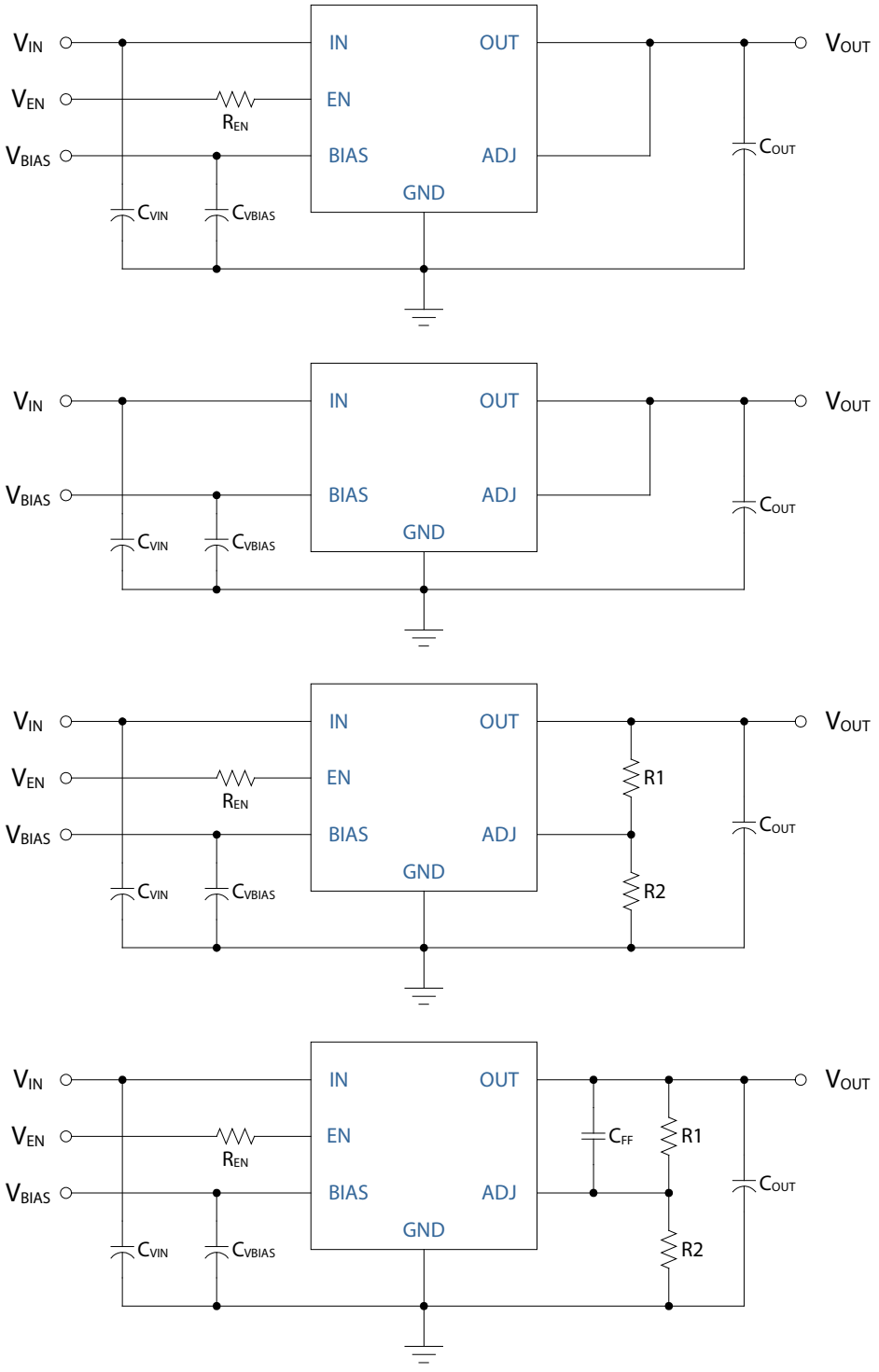
PIN DESCRIPTION

Pin No.			Pin Name	Pin Function
SOP-8	SOP-8-PP	TO252-5L		
1	1	1	ADJ	Output Adjust for Adjustable Output.
2	2	2	IN	Power Input.
8	8	3	GND	Reference Ground.
3	3	4	OUT	Power Output.
4	4	5	BIAS	Input Bias Voltage for powering all circuitry on the regulator except the output power TR.
5	5	-	EN	Chip Enable (SOP-8/SOP-8-PP Only).
6, 7	6, 7	-	NC	No Connection.
-	Exposed PAD	TAB	Thermal Exposed PAD / TAB	Connect to ground.

BLOCK DIAGRAM



TYPICAL APPLICATION



* See application information for the details over external capacitor.

** TJ49150 can deliver a continuous current of 1.5A over the full operating temperature. However, the output current is limited by the restriction of power dissipation which differs from packages. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of application. With respect to the applied package, the maximum output current of 1.5A may be still undeliverable.

*** For the details, see Application Information.

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for TJ=25℃, and limits in **boldface** type apply over the **full operating temperature range**.
Unless otherwise specified: $V_{BIAS} = V_{O(NOM.)} + 2.1V$, $V_{IN} = V_{O(NOM.)} + 1V$, $V_{EN}=V_{BIAS}$, I_L = 10 mA.

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Adjustable Pin Voltage		V_{ADJ}	V_{OUT}+1 V < V_{IN} < 5.5 V	0.784 **0.776**	0.8	0.816 **0.824**	V
Line Regulation(Note 1)		ΔV_{LINE}	V_{OUT}+1 V < V_{IN} < 5.5 V		0.02	**0.1**	%/V
Load Regulation(Note 1, 2)		ΔV_{LOAD}	10 mA < I_L < 1.5 A		0.25	**1.0**	%
Dropout Voltage(Note 2)		V_{DROP}	I_L = 0.75 A		120	160 **200**	mV
			I_L = 1.5 A		240	320 **400**	
Dropout Voltage(Note 2)		V_{DROP}	I_L = 1.5 A , V_{BIAS} = 5.0 V		200	270 **340**	mV
Dropout Voltage(Note 3)		V_{DROP}	I_L = 1.5 A		1.5	**2.1**	V
Bias Pin Current		I_{BIAS}	I_L = 1.5 A		300	450 **600**	µA
Ground Pin Current(Note 4)		I_{GND1}	I_L = 10 mA		300	450 **600**	µA
Ground Pin Current(Note 4)		I_{GND2}	V_{EN} < 0.2 V		0.1	0.5 **1.0**	µA
Current Limit		I_{CL}			2.5		A
Thermal Shutdown Temperature		T_{SD}			155		°C
Thermal Shutdown Hysteresis		ΔT_{SD}			30		°C
Enable threshold(Note 5)	Logic Low	V_{ENL}	Output = Low			0.4	V
	Logic High	V_{ENH}	Output = High	2.0			V
Enable Pin Input Current(Note 5)		I_{EN}	$V_{EN} = V_{BIAS}$		0.1	**1.0**	µA
Adjust Pin Current		I_{ADJ}	V_{ADJ} = 0.8 V		0.1	**1.0**	µA

Note 1. Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current.

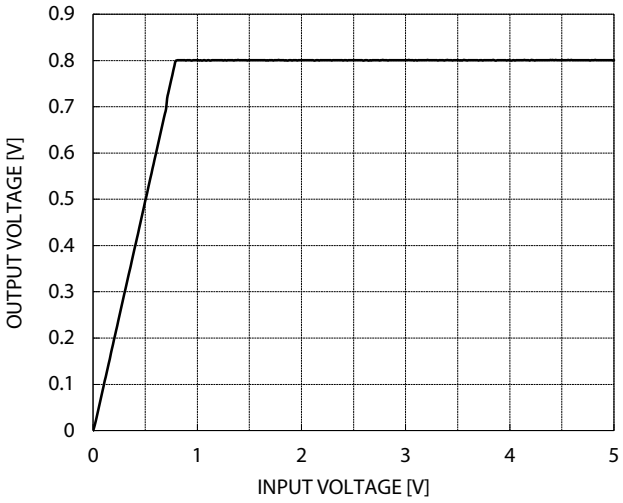
Note 2. Regulation is measured at constant junction temperature by using a 10ms current pulse. Devices are tested for load regulation in the load range from 10mA to 1.5A.

Note 3. For $V_{OUT} \leq 1.0V$, the V_{BIAS} Dropout specification does not apply due that the minimum V_{BIAS} input is 3.0V.

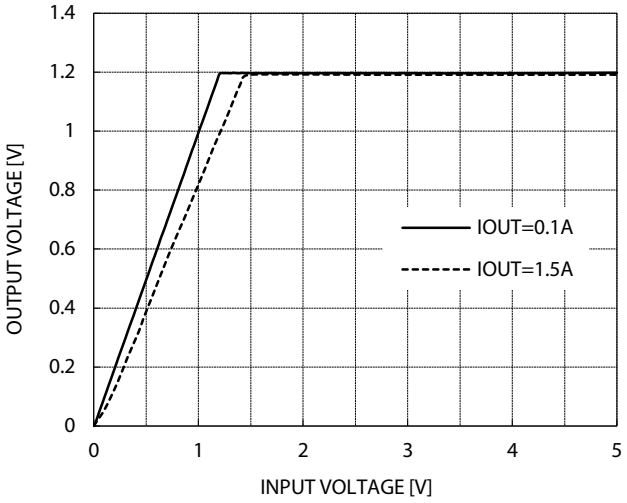
Note 4. $I_{GND} = I_{BIAS} + (I_{IN} - I_{OUT})$. The total current drawn from the supply is the sum of the load current plus the ground current.

Note 5. SOP-8/SOP-8-PP packages only.

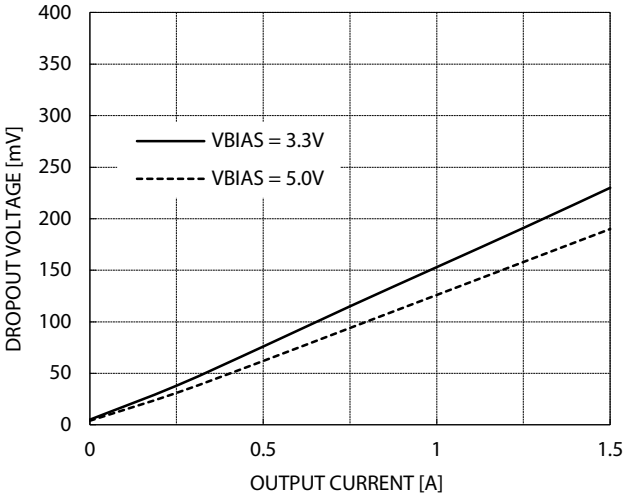
TYPICAL OPERATING CHARACTERISTICS



Reference Voltage vs. V_{IN}



Output Voltage vs. V_{IN}



Dropout Voltage (V_{IN}-V_{OUT}) vs. Output Current

T.B.D.

APPLICATION INFORMATION

The TJ49150 is a high performance, low dropout linear regulator, designed for high current application that requires fast transient response. The TJ49150 operates from two input supply voltages, significantly reducing dropout voltage. The TJ49150 is designed so that a minimum of external component are necessary.

Bias Supply Voltage

The TJ49150 control circuitry is supplied by the BIAS pin which requires a very low bias current even at the maximum output current level. A bypass capacitor on the bias pin is recommended to improve the performance of the TJ49150 during line and load transient. A small ceramic capacitor from BIAS pin to ground reduces high frequency noise that could be injected into the control circuitry from the bias rail. In practical applications, a 1μF capacitor and smaller valued capacitors such as 0.01μF or 0.001μF in parallel with that larger capacitor may be used to decouple the bias supply. The BIAS input voltage must be 2.1V above the output voltage, with a minimum BIAS input voltage of 3.0V.

Adjustable Regulator Design

The TJ49150 adjustable version allows fixing output voltage anywhere between 0.8V and 2.0V using two external resistors as presented in the typical application circuit. The resistor values are given by;

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

It is suggested to use R1 values lower than 10kΩ to obtain better load transient performances. Even, higher values up to 100kΩ are suitable.

Enable

The SOP-8 and SOP8-PP types of TJ49150 feature an active high Enable input(EN) that allows on/off control of the regulator. The enable function of TJ49150 has hysteresis characteristics. The enable input allows on control of the regulator with the enable pin voltage of 2.0V or above. When the enable input voltage lowers under 0.4V, the enable input allows off control of the regulator. If not in used for logic control, EN pin must be tied to BIAS voltage for proper operation. When a pull-up resistor is connected between EN pin and V_{EN} signal(or V_{BIAS} line), the resistance should be kept under 10kΩ. The EN pin must not be left at high impedance.

Supply Power Sequencing

In common applications where the power on transient of IN and BIAS voltages are not particularly fast(Tr>100μs), no power sequencing is required. Where voltage transient input is very fast(Tr<100μs), it is recommended to have the IN voltage present before or, at least, at the same time as the BIAS voltage in order to avoid over voltage spikes during the power on transient.

Output Capacitors

The TJ49150 requires a minimum output capacitance to maintain stability. The TJ49150 is specifically designed to be stable with a ceramic chip, tantalum, and aluminum electrolytic capacitor. A 10μF of ceramic chip capacitor or a 33μF tantalum or aluminum electrolytic capacitor would satisfy most applications. Its minimum value of ceramic chip capacitor is 1μF and of tantalum or aluminum electrolytic capacitor is 22μF. They might be increased if output current is high.

Input Capacitor

An input capacitor of minimum 1μF of chip ceramic capacitor or 10μF of tantalum or aluminum electrolytic

capacitor is recommended. Larger values will help to improve ripple rejection by bypassing the input to the regulator, further improving the integrity of the output voltage.

Feed Forward Capacitor

The TJ49150 requires a feed forward capacitor to stabilize output in case of complicated transient load condition. It also performs a soft-start(SS) function on the output voltage. A 10nF is recommended to support its stability support function and its higher value will increase the time of SS function.

Maximum Output Current Capability

The TJ49150 can deliver a continuous current of 1.5A over the full operating junction temperature range. However, the output current is limited by the restriction of power dissipation which differs from packages. A heat sink may be required depending on the maximum power dissipation and maximum ambient temperature of application. With respect to the applied package, the maximum output current of 1.5A may be still undeliverable due to the restriction of the power dissipation of TJ49150. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.
The temperatures over the device are given by :

$$T_C = T_A + P_D \text{ X } \theta_{CA} \quad / \quad T_J = T_C + P_D \text{ X } \theta_{JC} \quad / \quad T_J = T_A + P_D \text{ X } \theta_{JA}$$

Where T_J is the junction temperature, T_C is the case temperature, T_A is the ambient temperature, P_D is the total power dissipation of the device, θ_{CA} is the thermal resistance of case-to-ambient, θ_{JC} is the thermal resistance of junction-to-case, and θ_{JA} is the thermal resistance of junction to ambient.
The total power dissipation of the device is given by:

$$P_D = P_{IN} - P_{OUT} = \{(V_{IN} \text{ X } I_{IN}) + (V_{BIAS} \text{ X } I_{BIAS})\} - (V_{OUT} \text{ X } I_{OUT})$$

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D = (T_{Jmax} - T_{Amax}) / P_D$$

TJ49150 is available in SOP-8, SOP-8-PP, and TO-252-5L packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow.

If proper cooling solution such as heat sink, copper plane area, air flow is applied, the maximum allowable power dissipation could be increased. However, if the ambient temperature is increased, the allowable power dissipation would be decreased.

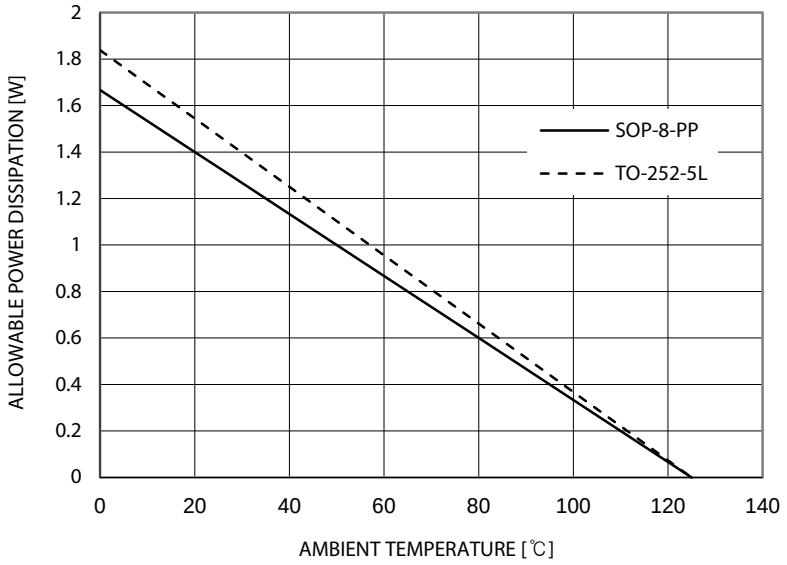
The θ_{JA} could be decreased with respect to the copper plane area. So, the specification of maximum power dissipation for an application is fixed, the proper copper plane area could be estimated by following graphs. Wider copper plane area leads lower θ_{JA}.

The maximum allowable power dissipation is also influenced by the ambient temperature. With the θ_{JA}-Copper

plane area relationship, the maximum allowable power dissipation could be evaluated with respect to the ambient temperature. As shown in graph, the higher copper plane area leads θ_{JA}. And the higher ambient temperature leads lower maximum allowable power dissipation.

All this relationship is based on the aforesaid equation ; $\theta_{JA} = T_{Rmax} / P_D = (T_{Jmax} - T_{Amax}) / P_D$

The graph below is valid for the thermal impedance specified in the Thermal Information section on page 2.



REVISION NOTICE

The information in this datasheet can be revised without any notice to describe proper electrical characteristics.