



SPXXHC00
SPXXHC08
SPXXHC10
SPXXHC11
SPXXHC20
SPXXHC30
SPXXHC132
SPXXHC133

Features

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- Speed, function and pin-out compatible to 74LS series Logic.
- High Noise Immunity.
- Low quiescent power consumption.
- Wide power supply range.
- Operates over V_{CC} range of 2.0 to 6.0 Volts.
- Symmetric current drive.
- All Inputs are fully buffered.
- All devices have Input Protection diodes to V_{CC} and ground.
- All devices have Logic Input voltage levels consistent with CMOS.

54/74 Series
AND/NAND Gates

Ordering Information

| Plastic DIP, Industrial Temp Range | Ceramic DIP, Industrial Temp Range | Ceramic DIP, Military Temp Range |
|---------------------------------------|---------------------------------------|-------------------------------------|
| SP74HCXXXN | SP74HCXXXJ | SP54HCXXXJ |

Absolute Maximum Ratings

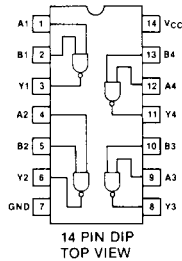
| Parameter | Min | Max | Units |
|---|------|--------------|-------|
| V_{CC} DC Supply Voltage | -0.5 | +7.0 | V |
| V_I, V_O Input or Output Voltage | -0.5 | $V_{CC}+0.5$ | V |
| I_L DC Current Per Pin Any Input or Output | — | 25 | mA |
| I_{CC} DC Current Drain, V_{CC} or GND | — | 50 | mA |
| T_S Storage Temperature | -65 | +150 | °C |
| P_D Power Dissipation (Note 1) | — | 500 | mW |
| T_L Lead Temperature (1/16" from mounting surface for 10 sec) | — | +300 | °C |

Note 1: Derate at 12mW/°C over +45 to +85°C for Plastic "N" Package.

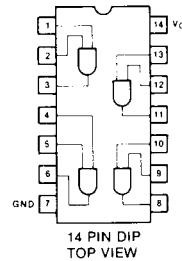
Recommended Operating Conditions

| Parameter | SP74HCXXX | | SP54HCXXX | | Units |
|--|-----------|----------|-----------|----------|-------|
| | Min | Max | Min | Max | |
| V_{CC} DC Supply Voltage Range | 2.0 | 6.0 | 2.0 | 6.0 | V |
| V_I, V_O Input Voltage, Output Voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| T_A Operating Temperature Range | -40 | +85 | -55 | +125 | °C |

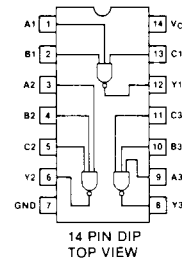
SPXXHC00
Quad 2-Input NAND Gate



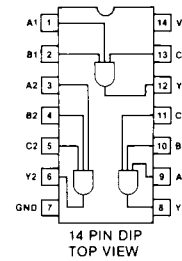
SPXXHC08
Quad 2-Input AND Gate



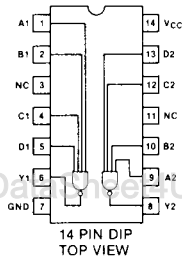
SPXXHC10
Triple 3-Input NAND Gate



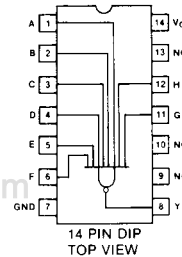
SPXXHC11
Triple 3-Input AND Gate



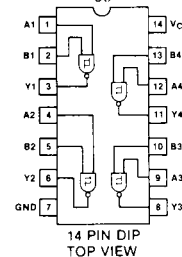
SPXXHC20
Dual 4-Input NAND Gate



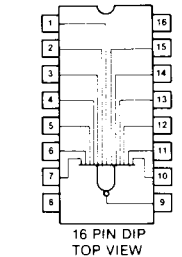
SPXXHC30
8-Input NAND Gate



SPXXHC132
Quad 2-Input NAND Gate Schmitt Trigger



SPXXHC133
13-Input NAND Gate



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DC Electrical Characteristics

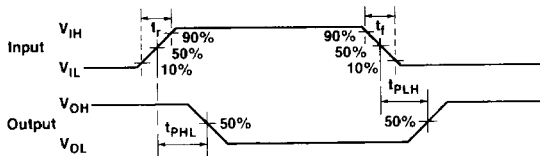
| Symbol | Parameter | Conditions | V _{CC} | Typ T = 25 °C | Guaranteed Limits | | Units | |
|-----------------|-----------------------------------|---|-------------------------|------------------|-------------------------|--------------------------|-------|------|
| | | | | | SP74HC -40 to +85 °C | SP54HC -55 to +125 °C | | |
| V _{IH} | Minimum High Level Input Voltage | V _O = 0.1V or V _{CC} - 0.1V I _O ≤ 20 μA | 2.0V | | 1.5 | 1.5 | V | |
| | | | 4.5V | | 3.15 | 3.15 | | |
| | | | 6.0V | | 4.2 | 4.2 | | |
| V _{IL} | Maximum Low Level Input Voltage | V _O = 0.1V or V _{CC} - 0.1V I _O ≤ 20 μA | 2.0V | | 0.3 | 0.3 | V | |
| | | | 4.5V | | 0.9 | 0.9 | | |
| | | | 6.0V | | 1.2 | 1.2 | | |
| V _{OH} | Minimum High Level Output Voltage | I _{OH} = 20 μA V _I = V _{CC} or GND | 2.0V | 2.0 | 1.9 | 1.9 | V | |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | | |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | V | |
| | | | 4.5V | * | 3.7 | 3.7 | | |
| | | | 6.0V | * | 5.2 | 5.2 | | |
| V _{OL} | Maximum Low Level Output Voltage | I _{OL} = 20 μA V _I = V _{CC} or GND | 2.0V | 0 | 0.1 | 0.1 | V | |
| | | | 4.5V | 0 | 0.1 | 0.1 | | |
| | | | 6.0V | 0 | 0.1 | 0.1 | V | |
| | | | 4.5V | * | 0.3 | 0.4 | | |
| | | | 6.0V | * | 0.3 | 0.4 | | |
| I _{IN} | Input Leakage Current | V _I = V _{CC} or GND V _{CC} = 2.0 to 6.0V | | | ± 1.0 | ± 1.0 | μA | |
| I _{CC} | Maximum Quiescent Supply Current | V _I = V _{CC} or GND I _O = 0 μA | T _A = 25 °C | 0.1 | 2.0 | 2.0 | μA | |
| | | | T _A = 85 °C | | 5.0V | 20.0 | | 20.0 |
| | | | T _A = 125 °C | | 5.0V | | | 40.0 |

* 4mA STD outputs 6mA Bus-Drivers Note: For Schmitt Trigger V_{T+} = 3.7, V_{T-} = 1.2 @ V_{CC} = 5.0V

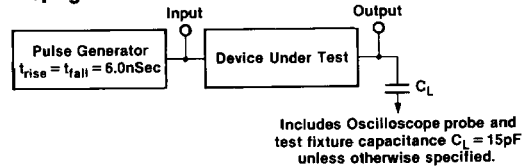
AC Electrical Characteristics (V_{CC} = 5.0V, t_r = t_f = 6ns, T_A = 25 °C, unless otherwise specified)

| Device Types | Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|--------------|-------------------------------------|--|-----------------------|-----|------------------|-------|
| 00 | t _{PHL} , t _{PLH} | Maximum Propagation Delay Any Input to Output | C _L = 15pF | 11 | | ns |
| | | | C _L = 50pF | 13 | | |
| 08 | t _{PHL} , t _{PLH} | Maximum Propagation Delay Any Input to Output | C _L = 15pF | 16 | | ns |
| | | | C _L = 50pF | 18 | | |
| 10, 133 | t _{PHL} , t _{PLH} | Maximum Propagation Delay Any Input to Output | C _L = 15pF | 13 | | ns |
| | | | C _L = 50pF | 16 | | |
| 11 | t _{PHL} , t _{PLH} | Maximum Propagation Delay Any Input to Output | C _L = 15pF | 14 | | ns |
| | | | C _L = 50pF | 16 | | |
| 20, 30, 132 | t _{PHL} , t _{PLH} | Maximum Propagation Delay Any Input to Output | C _L = 15pF | 17 | | ns |
| | | | C _L = 50pF | 20 | | |
| | C _{IN} | Maximum Input Capacitance | | 2 | | pF |

AC Waveforms



Propagation Time Test Circuit



All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (either V_{CC} or GND).