FAIRCHILD SEMICONDUCTOR®

October 2011

FAN3850T
Microphone Pre-Amplifier with Temperature Compensation and Digital Output

Features

- Optimized for Mobile Handset and Notebook PC Microphone Applications
- Accepts Input from Electret Condenser Microphones
- Pulse Density Modulation (PDM) Output
- Standard 5-Wire Digital Interface
- Amplifier Gain: 15.7dB
- Negative Temperature Coefficient to Compensate for ECM Positive Temperature Coefficient
- Low Input Capacitance, High PSR, 20kHz Pre-Amplifier
- Low-Power, 1.5µA Sleep Mode
- Typical 420µA Supply Current
- Signal to Noise Ratio of 62.4dB(A)
- Total Harmonic Distortion: 0.01%
- Input Clock Frequency Range of 1-4MHz
- Integrated Low Drop-Out Regulator (LDO)
- Small 1.26mm x 0.86mm 6-Ball WLCSP

Applications

- Electret Condenser Microphones with Digital Output
- Mobile Handsets
- Headset Accessories
- Personal Computers (PC)

Description

The FAN3850T integrates a pre-amplifier, LDO, and Analog-to-Digital Converter (ADC) to convert Electret Condenser Microphone (ECM) outputs to digital Pulse Density Modulation (PDM) data streams. The pre-amplifier accepts analog signals from the ECM and drives an over-sampled sigma delta ADC and outputs PDM data. The PDM digital audio has the advantage of noise rejection and interface-to-mobile handset processors.

The FAN3850T is powered from the system supply rails up to 3.63V, with a low power consumption of only 0.85mW, and less than 20µW in Power-Down Mode. The device compensates for the temperature variation of the microphone element to achieve a flat sensitivity response over-temperature.

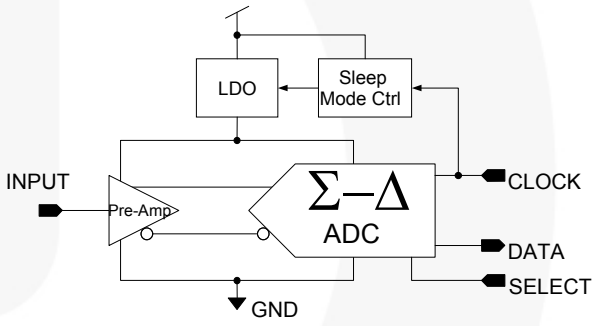


Figure 1. Block Diagram

Ordering Information

Part Number	Gain Option	Operating Temperature Range	Package	Packing Method
FAN3850TUC15X35	15.7dB	-30°C to +85°C	6-Ball, Wafer-Level Chip-Scale Package (WLCSP)	3000 Unit Tape & Reel

Note:
1. Alternate gain options and temperature coefficient slopes are possible. Please contact a Fairchild representative.

Pin Configuration

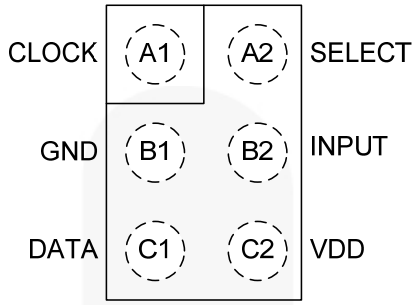


Figure 2. Pin Configuration (Top View)

Pin Definitions

Pin#	Name	Type	Description
A1	CLOCK	Input	Clock Input
B1	GND	Input	Ground Pin
C1	DATA	Output	PDM Output – 1-Bit ADC
A2	SELECT	Input	Rising or Falling Clock-Edge Select
B2	INPUT	Input	Microphone Input
C2	VDD	Input	Device Power Pin

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	-0.3	4.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
ESD	Human Body Model, JESD22-A114[(2)], All Pins Except Microphone Input	±7		kV
	Human Body Model, JESD22-A114[(2)], Microphone Input	±300		V

Note:

2. This device is fabricated using CMOS technology and is therefore susceptible to damage from electrostatic discharges. Appropriate precautions must be taken during handling and storage of this device to prevent exposure to ESD.

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+125	°C
T_{REFLOW}	Peak Reflow Temperature			+260	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		90		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-30		+85	°C
V_{DD}	Supply Voltage Range	1.64	1.80	3.63	V
t_{RF-CLK}	Clock Rise and Fall Time			10	ns

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8V, V_{IN}=94dB (SPL), f_{CLK}=2.4MHz, duty cycle = 50%, and C_{MIC}=15pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Range		1.64	1.80	3.63	V
I_{DD}	Supply Current	INPUT=AC Coupled to GND, CLOCK=On, No Load		420		µA
I_{SLEEP}	Sleep Mode Current	f_{CLK}=GND		1.4	8.0	µA
PSR	Power Supply Rejection(7)	INPUT=AC Coupled to GND, Test Signal on V_{DD}=217Hz Square Wave and Broad Band Noise(3) both 100mV_{P-P}		-80		dBFS
IN_{NOM}	Nominal Sensitivity(4)	INPUT=94dBSPL		-26		dBFS
SNR	Signal-to-Noise Ratio	f_{IN}=1kHz 1Pa, A-Weighted		62.4		dB(A)
e_N	Input Referred Noise(7)	20Hz to 20kHz, A-Weighted 15.7dB Gain		5.3	8.6	µV_{RMS}
THD	Total Harmonic Distortion(5)	f_{IN}=1kHz, INPUT=-26dBFS		0.01	0.10	%
THD+N	THD and Noise(7)	50Hz ≤ f_{IN} ≤ 1kHz, INPUT=-20dBFS		0.2	1.0	%
		f_{IN}=1kHz, INPUT=-5dBFS		1.0	5.0	
		f_{IN}=1kHz, INPUT=0dBFS		5.0	10.0	
tc	Temperature Coefficient(7,11)	Gain Measured at 50˚C and -10˚C		-0.035		dB/˚C
C_{IN}	Input Capacitance(7,11)	INPUT		0.2		pF
R_{IN}	Input Resistance(7,11)	INPUT	>100			GΩ
V_{IL}	CLOCK & SELECT Input, Logic LOW Level				0.3	V
V_{IH}	CLOCK & SELECT Input, Logic HIGH Level		1.5		V_{DD}+0.3	V
V_{OL}	Data Output, Logic LOW Level				0.35×V_{DD}	V
V_{OH}	Data Output, Logic HIGH Level		0.65×V_{DD}			V
V_{IN15dB}	Maximum Input Signal for 15.7dB of Gain(5)	f_{IN}=1 kHz, THD+N < 10%; DC Level=0V			503	mV_{PP}
V_{OUT}	Acoustic Overload Point(11)	THD < 10%	120			dBSPL

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8V, V_{IN}=94dB (SPL), f_{CLK}=2.4MHz, duty cycle = 50%, and C_{MIC}=15pF.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_A	Time from CLOCK Transition to Data Becoming Valid	On Falling Edge of CLOCK, SELECT=GND, C_{LOAD}=15pF	18	43		ns
t_B	Time from CLOCK Transition to Data Becoming Hi-Z	On Rising Edge of CLOCK, SELECT=GND, C_{LOAD}=15pF	0	5	16	ns
t_A	Time from CLOCK Transition to Data Becoming Valid	On Rising Edge of CLOCK, SELECT=V_{DD}, C_{LOAD}=15pF	18	56		ns
t_B	Time from CLOCK Transition to Data Becoming Hi-Z	On Falling Edge of CLOCK, SELECT=V_{DD}, C_{LOAD}=15pF	0	5	16	ns
f_{CLK}	Input CLOCK Frequency(8)	Active Mode	1.0	2.4	4.0	MHz
CLK_{dc}	CLOCK Duty Cycle(7)		40	50	60	%
t_{WAKEUP}	Wake-Up Time(9)	f_{CLK}=2.4MHz		0.35	2.00	ms
$t_{FALLASLEEP}$	Fall-Asleep Time(10)	f_{CLK}=2.4MHz	0	0.01	1.00	ms
C_{LOAD}	Load Capacitance on Data				100	pF

Notes:

3. Pseudo-random noise with triangular probability density function. Bandwidth up to 10MHz.
4. Assumes 120dB(SPL) is mapped to 0Dbfs.
5. Assumes an input -41, or -38dBV, depending on the part-specific gain.
6. Verified by design simulation, showing idle tones and low noise level modulation to be typical 96dB.
7. Guaranteed by characterization.
8. All parameters are tested at 2.4MHz. Frequency range guaranteed by characterization.
9. Device wakes up when $f_{CLK} \geq$ 300kHz.
10. Device falls asleep when $f_{CLK} \leq$ 70kHz.
11. Guaranteed by design.
12. Temperature coefficient is calculated by measuring gain in db at 50˚C and -10°C and dividing by 60 (Gain(50°C) – Gain(-10°C)/60).

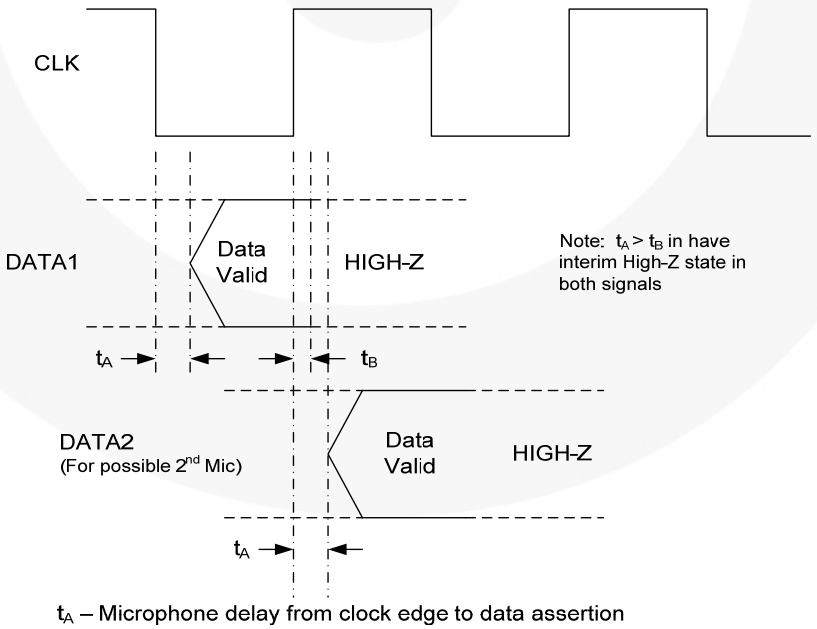


Figure 3. Interface Timing

Typical Performance Characteristics

Unless otherwise specified, all limits are guaranteed for T_A=25°C, V_{DD}=1.8V, V_{IN}=94dB(SPL), f_{CLK}=2.4MHz, and duty cycle=50%.

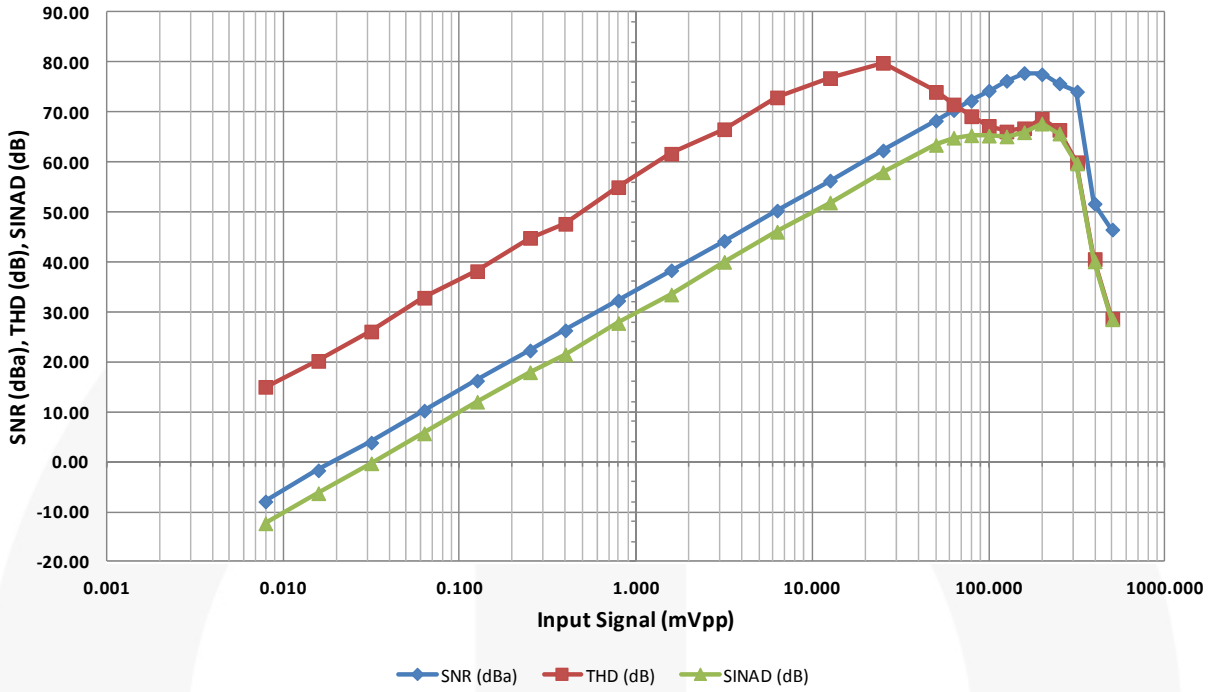


Figure 4. THD, SINAD, and SNR vs. Input Amplitude

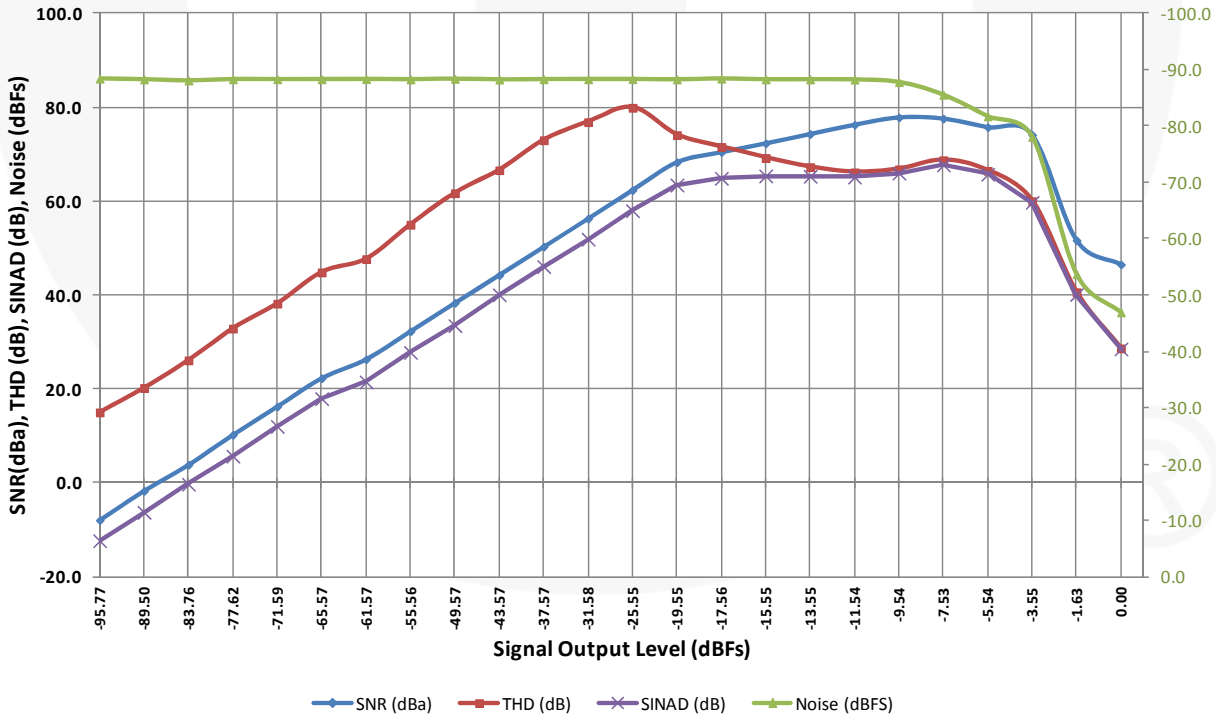


Figure 5. THD, SINAD, and SNR vs. Output Level

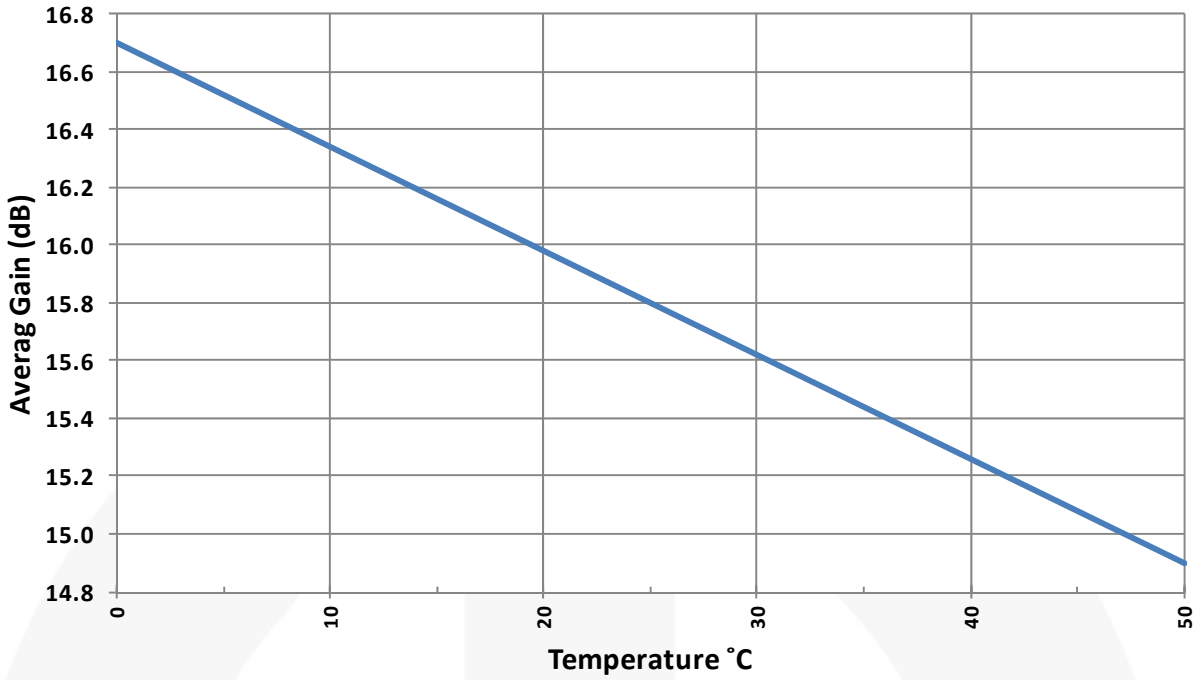


Figure 6. Gain vs. Temperature (~.035db/˚C)(1)

Note:

13. Alternate temperature coefficient slopes are possible. Please contact a Fairchild representative.

Applications Information

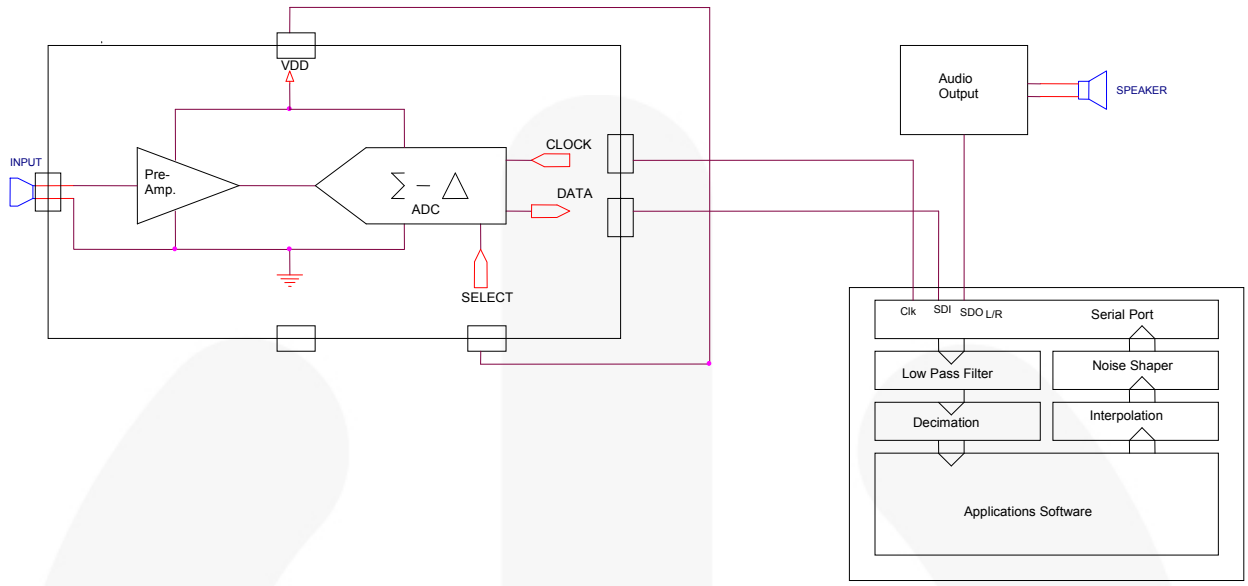


Figure 7. Mono Microphone Application Circuit

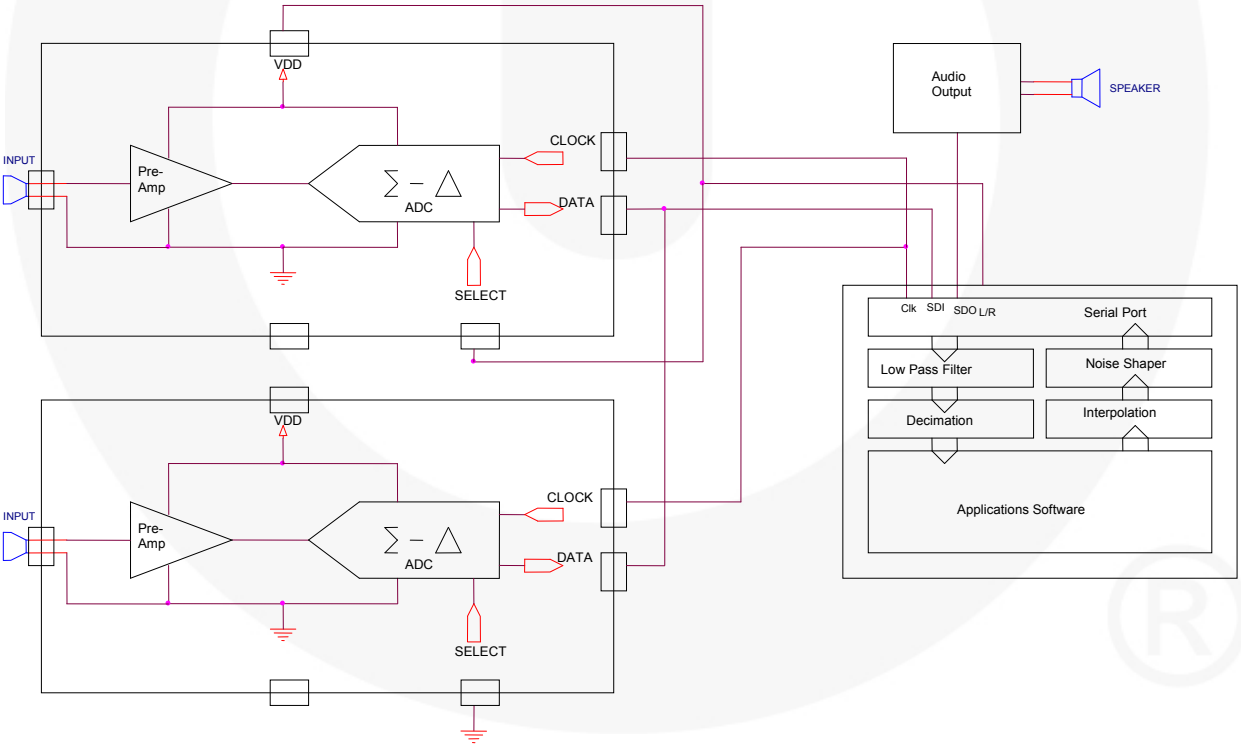


Figure 8. Stereo Microphone Application Circuit

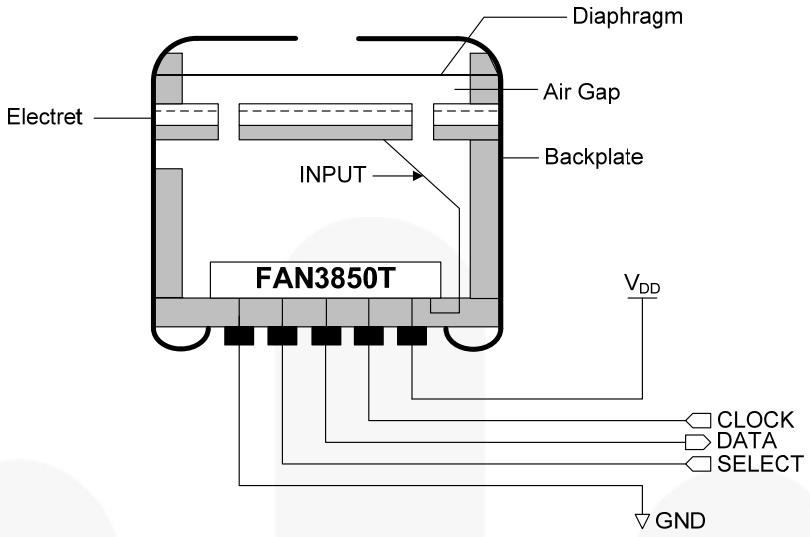


Figure 9. MIC Element Drawing

Applications Information

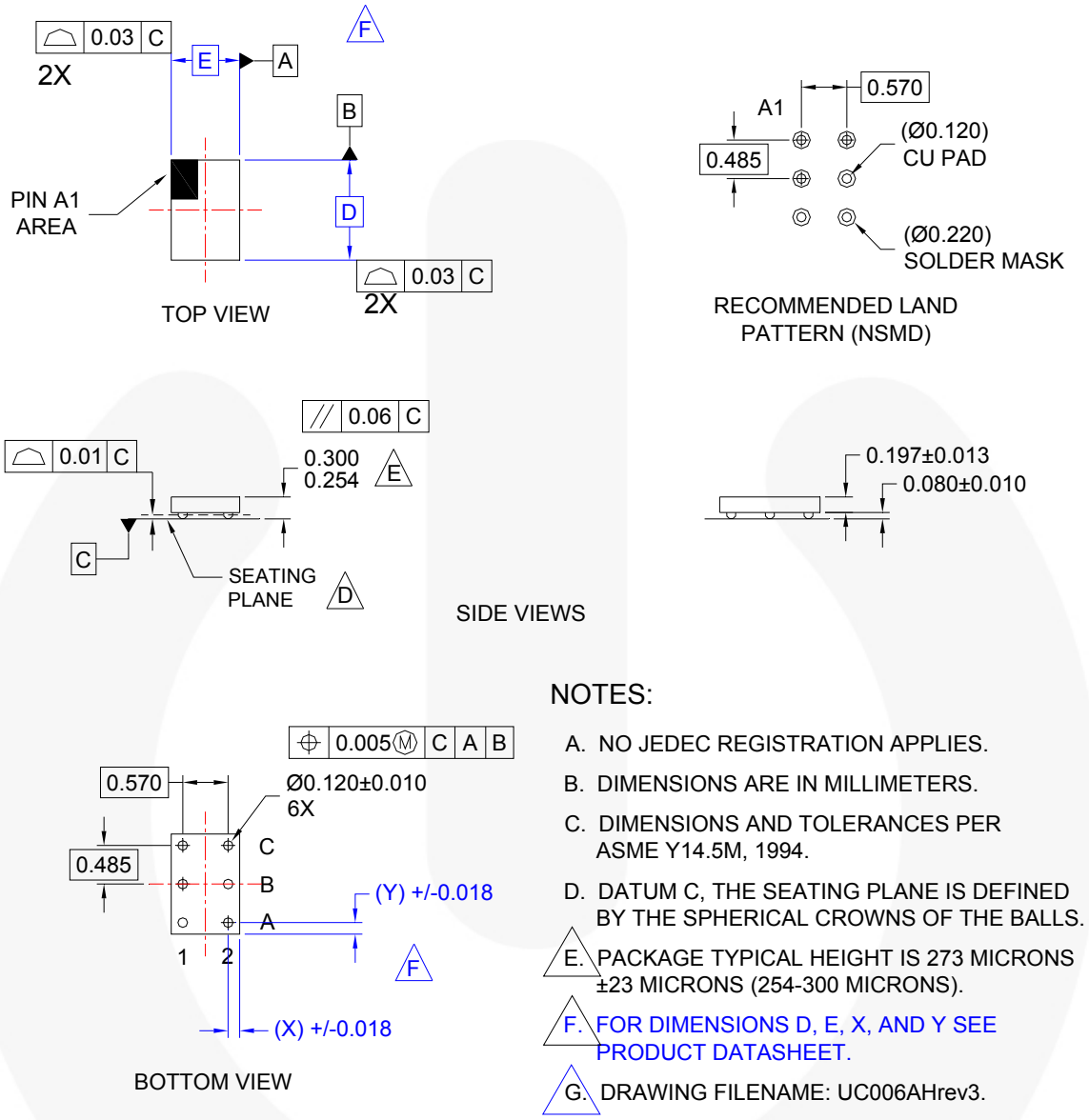
A 0.1µF decoupling capacitor is required for V_{DD}. It can be located either inside the microphone or on the PCB very close to the VDD pin.

Due to high input impedance, careful consideration should be taken to remove all flux used during the reflow soldering process.

A 100Ω resistance is recommended on the clock output of the device driving the FAN3850T to minimize ringing and improve signal integrity.

For optimal PSR, route a trace to the VDD pin. Do not place a V_{DD} plane under the device.

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 273 MICRONS ±23 MICRONS (254-300 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: UC006AHrev3.

Figure 10. 6-Ball, Wafer-Level Chip-Scale Package (WLCSP)

Table 1. Product-Specific Dimensions

D	E	X	Y
1.260mm	0.860mm	0.145mm	0.145mm
Ball Composition: SN97.5-Ag2.5			

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Rev. I58