

Features

256Kx32 bit CMOS Static Random Access Memory

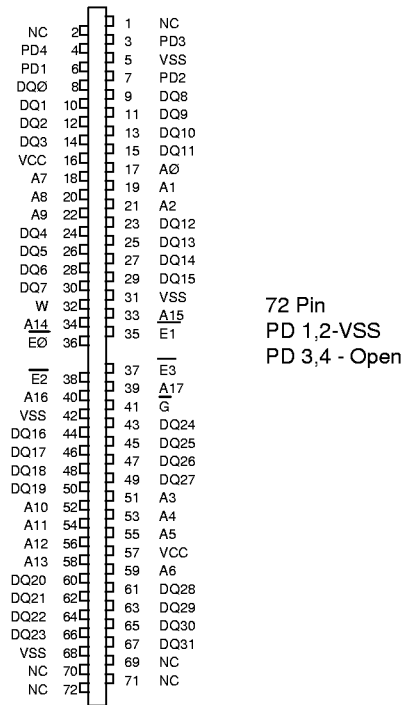
- Access Times
 - BiCMOS: 10 and 12ns
 - CMOS: 15, 20, 25, and 35ns
- Individual Byte Selects
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Package with JEDEC Standard Pinouts

- 72 Pin SIMM No. 175
- 72 Pin ZIP No. 176

Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram



**256Kx32 Static RAM
CMOS, High Speed Module**

The EDI9F32256C is a high speed 8 megabit Static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables (E0-E3) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

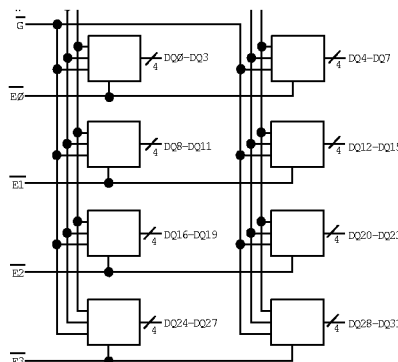
The EDI9F32256C is offered in 72 pin ZIP/SIMM package which enables eight megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

The ZIP and SIMM modules contain four PD (Presence Detect) pins which are used to identify module memory density in applications where alternate modules can be interchanged.

Pin Names

A0-A17	Address Inputs
E0-E3	Chip Enables
W,	Write Enables
G	Output Enable
DQ0-DQ31	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



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Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial.	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	7.5 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.3V	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max				Units
				10-12 ns	15ns	20 ns	25-35 ns	
Operating Power Supply Current	ICC1	$\bar{W}, \bar{E} = VIL, I/O = 0mA, \text{Min Cycle}$		1360	1280	1440	1280	mA
Standby (TTL) Power Supply Current	ICC2	$E \geq VIH, VIN \leq VIL \text{ or } VIN \geq VIH$		480	240	200	200	mA
Full Standby Power Supply Current	ICC3	$E \geq VCC-0.2V$		80	80	40	40	mA
		CMOS $VIN \geq VCC-0.2V \text{ or } VIN \leq 0.2V$						
Input Leakage Current	ILI	$VIN = 0V \text{ to } VCC$	--	±80	±80	±80	±80	µA
Output Leakage Current	ILO	$V I/O = 0V \text{ to } VCC$	--	±20	±20	±20	±20	µA
Output High Voltage	VOH	$IOH = -4.0mA$	2.4	--	--	--	--	V
Output Low Voltage	VOL	$IOL = 8.0mA$	--	0.4	0.4	0.4	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

\bar{E}	\bar{W}	\bar{G}	Mode	Output	Power
H	X	X	Standby	HIGH Z	ICC3
L	H	L	Read	DOUT	ICC1
L	L	X	Write	DIN	ICC1
L	H	H	Output Deselect	HIGH Z	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Control Line	CN	60	pF

These parameters are sampled, not 100% tested.

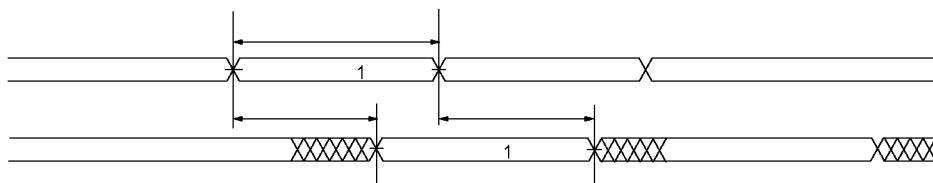
AC Characteristics Read Cycle

Parameter	Symbol		10ns*		12ns*		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	10		12		15		ns
Address Access Time	TAVQV	TAA		10		12		15	ns
Chip Enable Access	TELQV	TACS		10		12		15	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		5		6		8	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		5		8	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		4		4		5	ns

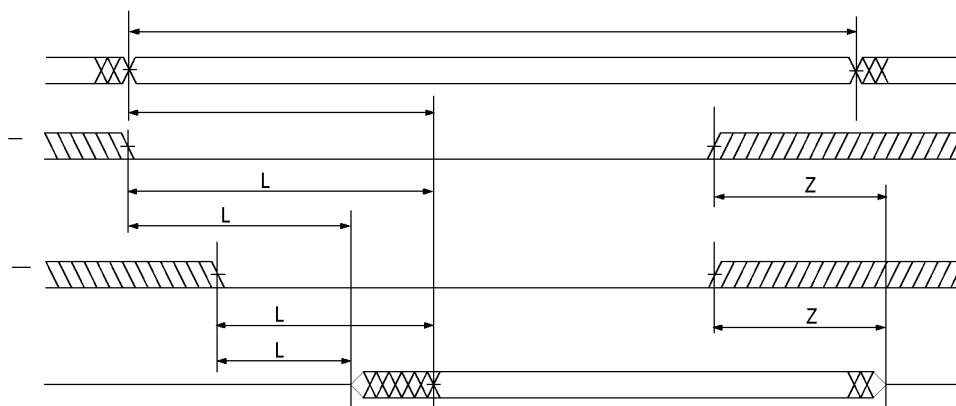
Note 1: Parameter guaranteed, but not tested.

*BICMOS

Read Cycle 1 - \overline{W} High, \overline{G} , \overline{E} Low



Read Cycle 2 - \overline{W} High

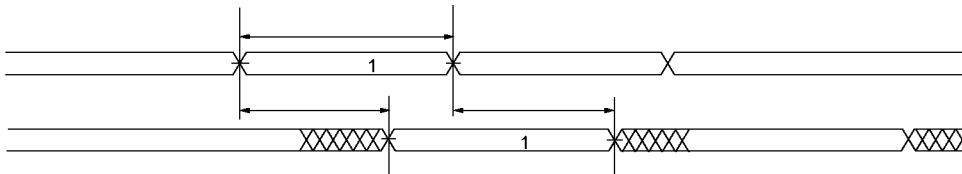


AC Characteristics Read Cycle

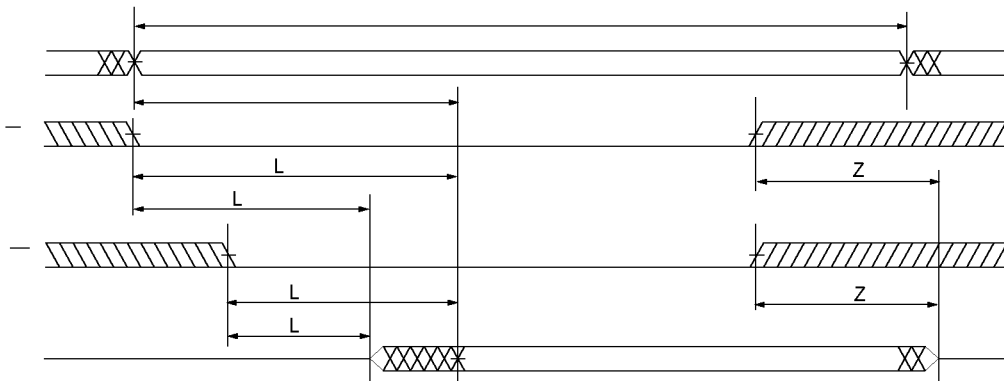
Parameter	Symbol		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	20		25		35		ns
Address Access Time	TAVQV	TAA		20		25		35	ns
Chip Enable Access	TELQV	TACS		20		25		35	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		10		12		15	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		13		15		20	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		8		10		12	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - \overline{W} High; \overline{G} , \overline{E} Low



Read Cycle 2 - \overline{W} High



AC Characteristics Write Cycle

Parameter	Symbol		10ns*		12ns*		15ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	10		12		15		ns
Chip Enable to End of Write	TELWH	TCW	7		8		12		ns
	TWLEH	TCW	7		8		10		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	7		8		10		ns
	TAVEH	TAW	7		8		10		ns
Write Pulse Width	TWLWH	TWP	7		8		10		ns
	TELEH	TWP	7		8		10		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	9	ns
Data to Write Time	TDVWH	TDW	5		6		7		ns
	TDVEH	TDW	5		6		7		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		ns

Note 1: Parameter guaranteed, but not tested.

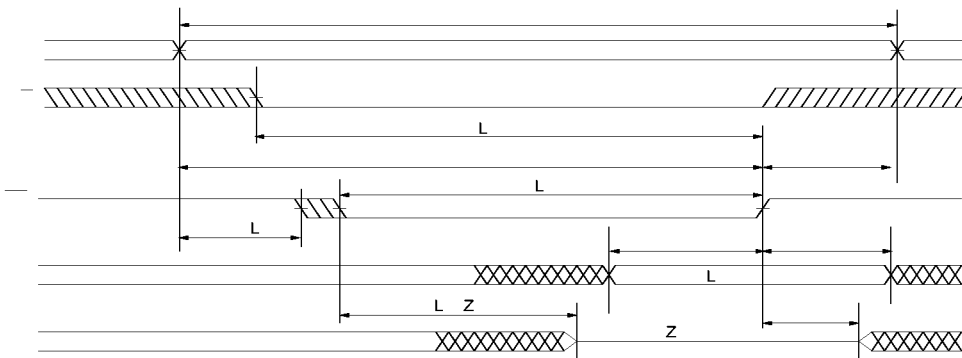
*BICMOS

AC Characteristics Write Cycle

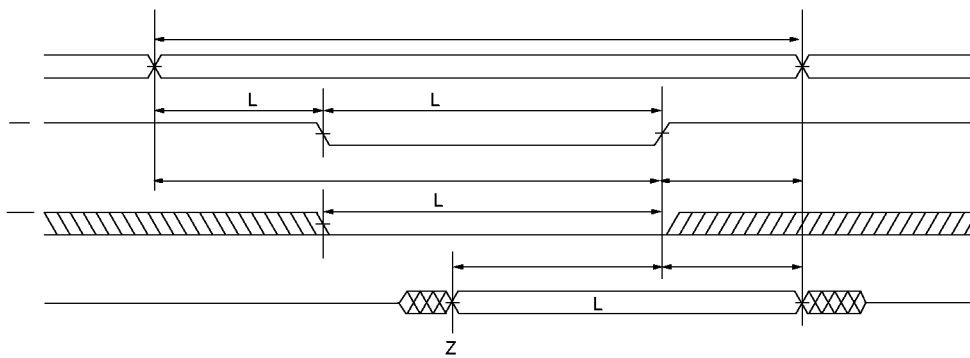
Parameter	Symbol		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	20		25		35		ns
Chip Enable to End of Write	TELWH	TCW	15		20		30		ns
	TWLEH	TCW	15		20		30		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	15		20		30		ns
	TAVEH	TAW	15		20		30		ns
Write Pulse Width	TWLWH	TWP	15		20		30		ns
	TELEH	TWP	15		20		30		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	10	0	12	0	15	ns
Data to Write Time	TDVWH	TDW	12		15		20		ns
	TDVEH	TDW	12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - \bar{W} Controlled



Write Cycle 2 - \bar{E} Controlled



EDI9F32256C

256Kx32 SRAM Module

Ordering Information

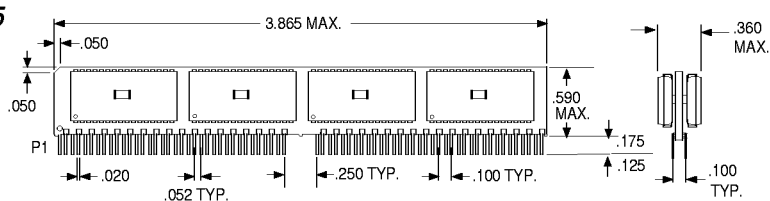
Part Number	Speed (ns)	Package No.
BICMOS		
EDI9F32256B10MNC	10	176
EDI9F32256B12MNC	12	176
CMOS		
EDI9F32256C15MNC	15	176
EDI9F32256C20MNC	20	176
EDI9F32256C25MNC	25	176
EDI9F32256C35MNC	35	176

Part Number	Speed (ns)	Package No.
BICMOS		
EDI9F32256B10MZC	10	175
EDI9F32256B12MZC	12	175
CMOS		
EDI9F32256C15MZC	15	175
EDI9F32256C20MZC	20	175
EDI9F32256C25MZC	25	175
EDI9F32256C35MZC	35	175

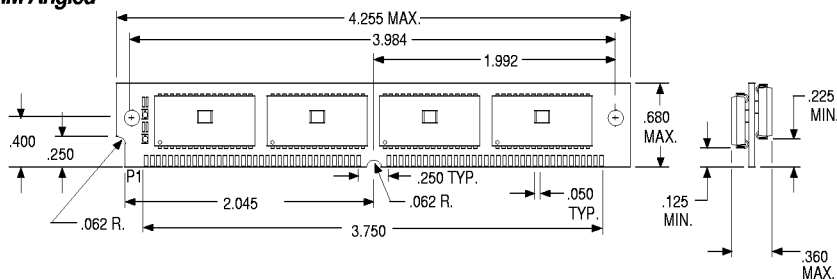
NOTE: Gold Contacts available on the 72 Pin SIMM add -G to the Part Number

Package Description

Package No. 175
72 Pin ZIP



Package No. 176
72 Pin SIMM Angled



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