

Frequency Generator for CPU, QPI, FBD, PCIe Gen 2 & SATA

ICS9FG104D

Description

The **ICS9FG104D** is a Frequency Timing Generator that provides 4 differential output pairs that are compliant to the Intel CK410 specification. It also provides support for PCI-Express and SATA. The part synthesizes several output frequencies from either a 14.31818 Mhz crystal or a 25 MHz crystal. The device can also be driven by a reference input clock instead of a crystal. It provides outputs with cycle-to-cycle jitter of less than 50 ps and output-to-output skew of less than 35 ps. The **ICS9FG104D** also provides a copy of the reference clock. Frequency selection can be accomplished via strap pins or SMBus control.

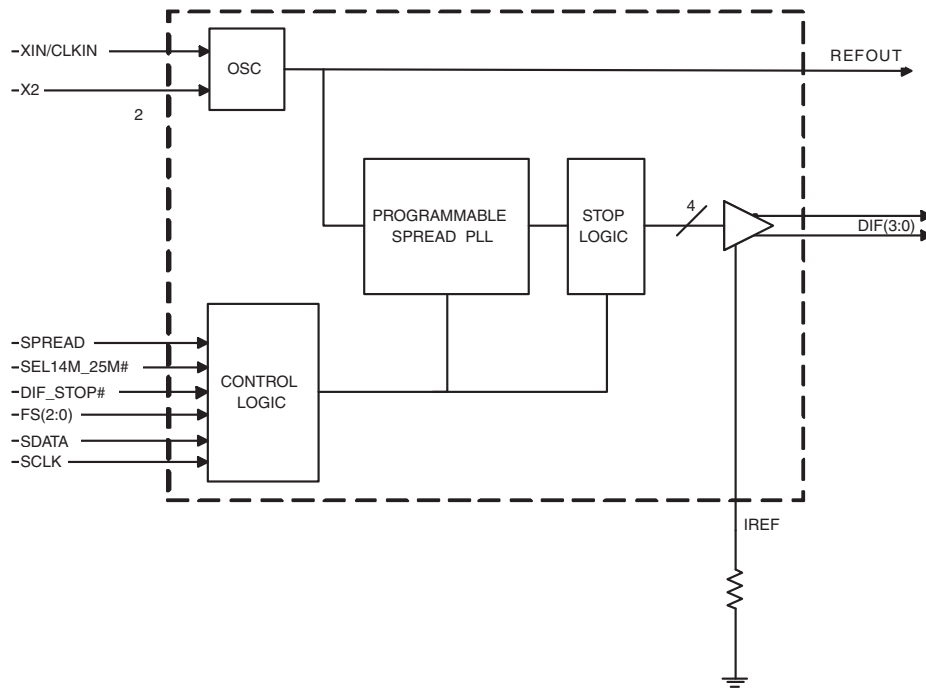
Features/Benefits

- Generates common frequencies from 14.318 MHz or 25 MHz
- Crystal or reference input
- 4 - 0.7V current-mode differential output pairs
- Supports Serial-ATA at 100 MHz
- Two spread spectrum modes: 0 to -0.5 downspread and +/-0.25% centerspread
- Unused inputs may be disabled in either driven or Hi-Z state for power management.

Key Specifications

- Output cycle-to-cycle jitter < 50 ps
- Output to output skew < 35 ps
- +/-300 ppm frequency accuracy on output clocks
- +/-50 ppm at any frequency w/spread off

Functional Block Diagram



Pin Configuration

| | | | | |
|-----------|----|-------------------|----|--------------|
| XIN/CLKIN | 1 | ICS9FG104D | 28 | VDDA |
| X2 | 2 | | 27 | GNDA |
| VDD | 3 | | 26 | IREF |
| GND | 4 | | 25 | vFS0 |
| REFOUT | 5 | | 24 | vFS1 |
| vFS2 | 6 | | 23 | DIF_0 |
| DIF_3 | 7 | | 22 | DIF_0# |
| DIF_3# | 8 | | 21 | VDD |
| VDD | 9 | | 20 | GND |
| GND | 10 | | 19 | DIF_1 |
| DIF_2 | 11 | | 18 | DIF_1# |
| DIF_2# | 12 | | 17 | ^SEL14M_25M# |
| SDATA | 13 | | 16 | vSPREAD |
| SCLK | 14 | | 15 | DIF_STOP# |

^ Pin has internal 120K pull up
 v Pin has internal 120K pull down

Functionality Table

| SEL14M_25M# (FS3) | FS2 | FS1 | FS0 | OUTPUT(MHz) |
|----------------------|-----|-----|-----|-------------|
| 0 | 0 | 0 | 0 | 100.00 |
| 0 | 0 | 0 | 1 | 125.00 |
| 0 | 0 | 1 | 0 | 133.33 |
| 0 | 0 | 1 | 1 | 166.67 |
| 0 | 1 | 0 | 0 | 200.00 |
| 0 | 1 | 0 | 1 | 266.00 |
| 0 | 1 | 1 | 0 | 333.00 |
| 0 | 1 | 1 | 1 | 400.00 |
| 1 | 0 | 0 | 0 | 100.00 |
| 1 | 0 | 0 | 1 | 125.00 |
| 1 | 0 | 1 | 0 | 133.33 |
| 1 | 0 | 1 | 1 | 166.67 |
| 1 | 1 | 0 | 0 | 200.00 |
| 1 | 1 | 0 | 1 | 266.00 |
| 1 | 1 | 1 | 0 | 333.00 |
| 1 | 1 | 1 | 1 | 400.00 |

28-pin SSOP/TSSOP

Power Groups

| Pin Number | | Description |
|------------|-------|------------------------------------|
| VDD | GND | |
| 3 | 4 | REFOUT, Digital Inputs |
| 9,21 | 10,20 | DIF Outputs |
| 28 | 27 | IREF, Analog VDD, GND for PLL Core |

Pin Description

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|--------------|----------|---|
| 1 | XIN/CLKIN | IN | Crystal input or Reference Clock input |
| 2 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 3 | VDD | PWR | Power supply, nominal 3.3V |
| 4 | GND | PWR | Ground pin. |
| 5 | REFOUT | OUT | Reference Clock output |
| 6 | vFS2 | IN | 3.3V Frequency select latched input pin with internal 120kohm pull down resistor. |
| 7 | DIF_3 | OUT | 0.7V differential true clock output |
| 8 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 9 | VDD | PWR | Power supply, nominal 3.3V |
| 10 | GND | PWR | Ground pin. |
| 11 | DIF_2 | OUT | 0.7V differential true clock output |
| 12 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 13 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 14 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 15 | DIF_STOP# | IN | Active low input to stop differential output clocks. |
| 16 | vSPREAD | IN | Asynchronous, active high input to enable spread spectrum functionality. This pin has a 120Kohm pull down resistor. |
| 17 | ^SEL14M_25M# | IN | Select 14.31818 MHz or 25 Mhz input frequency. This pin has an internal 120kohm pull up resistor. 1 = 14.31818 MHz, 0 = 25 MHz |
| 18 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 19 | DIF_1 | OUT | 0.7V differential true clock output |
| 20 | GND | PWR | Ground pin. |
| 21 | VDD | PWR | Power supply, nominal 3.3V |
| 22 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 23 | DIF_0 | OUT | 0.7V differential true clock output |
| 24 | vFS1 | IN | 3.3V Frequency select latched input pin with internal 120kohm pull down resistor. |
| 25 | vFS0 | IN | 3.3V Frequency select latched input pin with internal 120kohm pull down resistor. |
| 26 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 27 | GND_A | PWR | Ground pin for the PLL core. |
| 28 | VDDA | PWR | 3.3V power for the PLL core. |

Absolute Max

| Symbol | Parameter | Min | Max | Units |
|----------|---|------|-----|-------|
| VDDxx | 3.3V Supply Voltage | | 4.6 | V |
| Ts | Storage Temperature | -65 | 150 | °C |
| Tambient | Ambient Operating Temp•(Commerical Grade) | 0 | +70 | °C |
| Tambient | Ambient Operating Temp•(Industrial Grade) | -40 | +85 | °C |
| Tcase | Case Temperature | | 115 | °C |
| ESD prot | Input ESD protection•human body model | 2000 | | V |

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = T_{AMBIENT}; Supply Voltage V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------------|--------------------------------|---|-----------------------|----------|-----------------------|-------|-------|
| Input High Voltage | V _{IH} | 3.3 V +/-5% | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | 3.3 V +/-5% | V _{SS} - 0.3 | | 0.8 | V | 1 |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | uA | 1 |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| Operating Supply Current | I _{DD3.3OP} | Full Active, C _L = Full load; f = 400 MHz | | 125 | 150 | mA | 1 |
| | | Full Active, C _L = Full load; f = 100 MHz | | 110 | 125 | mA | 1 |
| | I _{DD3.3STOP} | All outputs stopped driven | | 106 | 120 | mA | 1 |
| | | All outputs stopped Hi-Z | | 48 | 60 | mA | 1 |
| Input Frequency ³ | F _i | SEL14M_25M# = 0 | 22.5 | 25.00 | 27.5 | MHz | 3 |
| | | SEL14M_25M# = 1 | 12.886 | 14.31818 | 15.75 | MHz | 3 |
| Pin Inductance ¹ | L _{pin} | | | | 7 | nH | 1 |
| Input/Output Capacitance ¹ | C _{IN} | Logic Inputs | 1.5 | | 5 | pF | 1 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization ^{1,2} | T _{STABcom} | From V _{DD} Power-Up to 1st clock (Commercial) | | | 1.8 | ms | 1,2 |
| | T _{STABind} | From V _{DD} Power-Up to 1st clock (Industrial) | | | 1.8 | ms | 1,2 |
| Modulation Frequency | f _{MOD} | SEL14M_25M# = 0 | | 32.541 | | kHz | 1,3,4 |
| Modulation Frequency | f _{MOD} | SEL14M_25M# = 1 | | 32.467 | | kHz | 1,3,4 |
| DIF output enable | t _{DIFOE} | DIF output enable after DIF_Stop# de-assertion | | | 15 | ns | 1 |
| Input Rise and Fall times | t _R /t _F | 20% to 80% of VDD | | | 5 | ns | 1 |

¹Guaranteed by design, not 100% tested in production.

²See timing diagrams for timing requirements.

³ Input frequency should be measured at the REF pin and tuned to 0 PPM to meet ppm frequency accuracy on PLL outputs.

⁴ These values assume 25MHz or 14.31818MHz inputs respectively. Using a higher or lower frequency will scale these frequencies accordingly. The output frequency selected by the FS inputs will also scale. For example, 27MHz input with an FS selection of 100MHz will yield an output frequency of 27/25 x 100 = 108MHz.

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair
 $T_A = T_{AMBIENT}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 2\text{pF}$, $R_S = 33.2\Omega$, $R_P = 49.9\Omega$, $I_{REF} = 475\mu\text{A}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|---------------|--|---------|---------|---------|----------|-------|
| Output Impedance | Z_O^1 | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | | 150 | | 1 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Crossing variation over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | -300 | | 300 | ppm | 1,2,5 |
| Average period | Tperiod | 400MHz nominal | 2.49988 | 2.5000 | 2.5001 | ns | 2 |
| | | 400MHz spread | 2.4993 | | 2.5133 | ns | 2,3 |
| | | 333.33MHz nominal | 2.99985 | 3.0000 | 3.0002 | ns | 2 |
| | | 333.33MHz spread | 2.9991 | | 3.016 | ns | 2,3 |
| | | 266.66MHz nominal | 3.74981 | 3.7500 | 3.7502 | ns | 2 |
| | | 266.66MHz spread | 3.7489 | | 3.77 | ns | 2,3 |
| | | 200MHz nominal | 4.9998 | 5.0000 | 5.0003 | ns | 2 |
| | | 200MHz spread | 4.9985 | | 5.0266 | ns | 2,3 |
| | | 166.66MHz nominal | 5.9997 | 6.0000 | 6.0003 | ns | 2 |
| | | 166.66MHz spread | 5.9982 | | 6.0320 | ns | 2,3 |
| | | 133.33MHz nominal | 7.4996 | 7.5000 | 7.5004 | ns | 2 |
| | | 133.33MHz spread | 7.4978 | | 5.4000 | ns | 2,3 |
| | | 100.00MHz nominal | 9.9995 | 10.0000 | 10.0005 | ns | 2 |
| | | 100.00MHz spread | 9.9970 | | 10.0533 | ns | 2,3 |
| Absolute min period | T_{absmin} | 400MHz nominal/spread | 2.4143 | | | ns | 1,2 |
| | | 333.33MHz nominal/spread | 2.9141 | | | ns | 1,2 |
| | | 266.66MHz nominal/spread | 3.6639 | | | ns | 1,2 |
| | | 200MHz nominal/spread | 4.8735 | | | ns | 1,2 |
| | | 166.66MHz nominal/spread | 5.8732 | | | ns | 1,2 |
| | | 133.33MHz nominal/spread | 7.3728 | | | ns | 1,2 |
| | | 100.00MHz nominal/spread | 9.8720 | | | ns | 1,2 |
| Rise Time | t_r | $V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$ | 175 | | 700 | ps | 1 |
| Fall Time | t_f | $V_{OH} = 0.525\text{V}$, $V_{OL} = 0.175\text{V}$ | 175 | | 700 | ps | 1 |
| Rise Time Variation | d- t_r | | | | 125 | ps | 1 |
| Fall Time Variation | d- t_f | | | | 125 | ps | 1 |
| Duty Cycle | d_{t3} | Measured Differentially | 45 | | 55 | % | 1 |
| Skew, output to output | t_{sk3} | $V_T = 50\%$ | | | 35 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jyc-cyc}$ | Measured Differentially | | | 50 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is tuned to 0

³Figures are for down spread.

⁴This figure is the peak-to-peak phase jitter as defined by PCI-SIG for a PCI Express reference clock. Please visit <http://www.pcisig.com> for additional details

⁵+/- 50 ppm at any frequency with spread off

Electrical Characteristics - REF-14.318/25 MHz

$T_A = T_{AMBIENT}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $R_S = 33\Omega$ $C_L = 5\text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------|------------------|--|---------|------|-----|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | 0 | | | ppm | 1,2 |
| Clock period | T_{period} | 14.318MHz output nominal | 69.8413 | | | ns | 1,2 |
| | | 25.000MHz output nominal | 40.0000 | | | ns | 1,2 |
| Output High Voltage | V_{OH} | $I_{OH} = -1\text{ mA}$ | 2.4 | | | V | 1 |
| Output Low Voltage | V_{OL} | $I_{OL} = 1\text{ mA}$ | | | 0.4 | V | 1 |
| Output High Current | I_{OH} | $V_{OH} @MIN = 1.0\text{ V}$, $V_{OH} @MAX = 3.135\text{ V}$ | -29 | | -23 | mA | 1 |
| Output Low Current | I_{OL} | $V_{OL} @MIN = 1.95\text{ V}$, $V_{OL} @MAX = 0.4\text{ V}$ | 29 | | 27 | mA | 1 |
| Rise Time | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | 1 | 1.6 | 2.5 | ns | 1 |
| Fall Time | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | 1 | 1.6 | 2.5 | ns | 1,2 |
| Duty Cycle | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 52.5 | 55 | % | 1,2 |
| Jitter | $t_{jyc-cycCOM}$ | $V_T = 1.5\text{ V}$ (commerical) | | 150 | 200 | ps | 1 |
| Jitter | $t_{jyc-cycIND}$ | $V_T = 1.5\text{ V}$ (commerical) | | 400 | 600 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Trim capacitors must be used to tune the REF to the exact Crystal Frequency.

Electrical Characteristics - Differential Phase Jitter Parameters

| PARAMETER | Symbol | Conditions | Min | Typ | Max | Units | Notes | |
|---------------|------------------|---|-----|----------|-----|-------------|-------------|---|
| Jitter, Phase | $t_{jphasePLL}$ | PCIe Gen 1 | | 40 | 86 | ps (p-p) | 1,2 | |
| | $t_{jphaseLo}$ | PCIe Gen 2 $10\text{kHz} < f < 1.5\text{MHz}$ | | 1.2 | 3 | ps (RMS) | 1,2 | |
| | $t_{jphaseHigh}$ | PCIe Gen 2 $1.5\text{MHz} < f < \text{Nyquist} (50\text{MHz})$ | | 2.2 | 3.1 | ps (RMS) | 1,2 | |
| | t_{jphQPI} | QPI 133MHz 4.8G/6.4Gb, 12UI | | 0.25/0.2 | 0.5 | ps (RMS) | 1,3 | |
| | $t_{jphFBD3.2G}$ | FBD specs (11 to 33MHz) | | | 2.2 | 3 | ps (RMS) | 1 |
| | $t_{jphFBD4.8G}$ | FBD specs (11 to 33MHz) | | | 1.8 | 2.5 | ps (RMS) | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²See <http://www.pcisig.com> for complete specs

³First number is 4.8G link speed, second number is 6.4G link speed. From Intel Clock Jit tool 1.5.1

General SMBus serial interface information for the ICS9FG104D

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $DC_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $DC_{(h)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $DD_{(h)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(h)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Controller (Host) | | ICS (Slave/Receiver) |
|--------------------------|-----------|----------------------|
| T | starT bit | |
| Slave Address $DC_{(h)}$ | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Data Byte Count = X | | ACK |
| Beginning Byte N | | ACK |
| | X Byte | ◇ |
| | | ◇ |
| | | ◇ |
| | | ◇ |
| Byte N + X - 1 | | ACK |
| P | stoP bit | |

| Controller (Host) | | ICS (Slave/Receiver) |
|--------------------------|-----------------|----------------------|
| T | starT bit | |
| Slave Address $DC_{(h)}$ | | |
| WR | WRite | |
| Beginning Byte = N | | ACK |
| Repeat starT | | ACK |
| Slave Address $DD_{(h)}$ | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | |
| ACK | | Beginning Byte N |
| | X Byte | ◇ |
| | | ◇ |
| | | ◇ |
| | | ◇ |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

SMBus Table: Device Control Register, READ/WRITE ADDRESS (DC/DD)

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|--|----------------------------|------|--|-----------------|---------|
| Bit 7 | 17 | | FS3 ¹ | RW | See Frequency Selection Table, Page 1 | | Pin 17 |
| Bit 6 | 6 | | FS2 ¹ | RW | | | Pin 6 |
| Bit 5 | 24 | | FS1 ¹ | RW | | | Pin 24 |
| Bit 4 | 25 | | FS0 ¹ | RW | | | Pin 25 |
| Bit 3 | 16 | | Spread Enable ¹ | RW | Off | On | Pin 16 |
| Bit 2 | - | Enable Software Control of Frequency, Spread Enable (Spread Type always Software Control) | | RW | Hardware Select | Software Select | 0 |
| Bit 1 | | | DIF_STOP# drive mode | RW | Driven | Hi-Z | 0 |
| Bit 0 | | | SPREAD TYPE | RW | Down | Center | 0 |

Notes:

1. These bits reflect the state of the corresponding pins at power up, but may be written to if Byte 0, bit 2 is set to '1'. FS3 is the SEL14M_25M# pin.

SMBus Table: Output Enable Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|------------------|------|---------|--------|---------|
| Bit 7 | - | Reserved | | | | | 1 |
| Bit 6 | - | DIF_3 EN | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | - | DIF_2 EN | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | Reserved | | | | | 1 |
| Bit 3 | - | Reserved | | | | | 1 |
| Bit 2 | - | DIF_1 EN | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | - | DIF_0 EN | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | - | Reserved | | | | | 1 |

SMBus Table: Output Stop Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|---------------|-----------------------|------|----------|-----------|---------|
| Bit 7 | - | Reserved | | | | | 0 |
| Bit 6 | - | DIF_3 STOP EN | Free Run/ Stop Enable | RW | Free-run | Stop-able | 0 |
| Bit 5 | - | DIF_2 STOP EN | Free Run/ Stop Enable | RW | Free-run | Stop-able | 0 |
| Bit 4 | - | Reserved | | | | | 0 |
| Bit 3 | - | Reserved | | | | | 0 |
| Bit 2 | - | DIF_1 STOP EN | Free Run/ Stop Enable | RW | Free-run | Stop-able | 0 |
| Bit 1 | - | DIF_0 STOP EN | Free Run/ Stop Enable | RW | Free-run | Stop-able | 0 |
| Bit 0 | - | Reserved | | | | | 0 |

SMBus Table: Frequency Select Readback Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------------------------------|------------------|------|--|----|---------|
| Bit 7 | 27 | SEL14M_25M# ¹ (FS3) | State of pin 17 | R | See Frequency Selection Table, Page 1 | | Pin 17 |
| Bit 6 | 6 | FS2 ¹ | State of pin 6 | R | | | Pin 6 |
| Bit 5 | 44 | FS1 ¹ | State of pin 24 | R | | | Pin 24 |
| Bit 4 | 45 | FS0 ¹ | State of pin 25 | R | | | Pin 25 |
| Bit 3 | 16 | SPREAD ¹ | State of pin 26 | R | Off | On | Pin 16 |
| Bit 2 | | Reserved | | | | | 0 |
| Bit 1 | | Reserved | | | | | 0 |
| Bit 0 | | Reserved | | | | | 0 |

Notes:

1. These bits reflect the state of the corresponding pins, regardless of whether software programming is enabled or not.

SMBus Table: Vendor & Revision ID Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | X |
| Bit 6 | - | RID2 | | R | - | - | X |
| Bit 5 | - | RID1 | | R | - | - | X |
| Bit 4 | - | RID0 | | R | - | - | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

SMBus Table: DEVICE ID

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|--------------------|------|---|---|---------|
| Bit 7 | - | DID7 | Device ID = 08 hex | R | - | - | 0 |
| Bit 6 | - | DID6 | | R | - | - | 0 |
| Bit 5 | - | DID5 | | R | - | - | 0 |
| Bit 4 | - | DID4 | | R | - | - | 0 |
| Bit 3 | - | DID3 | | R | - | - | 1 |
| Bit 2 | - | DID2 | | R | - | - | 0 |
| Bit 1 | - | DID1 | | R | - | - | 0 |
| Bit 0 | - | DID0 | | R | - | - | 0 |

SMBus Table: Byte Count Register

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | - | BC7 | Writing to this register will configure how many bytes will be read back, default is 07 = 7 bytes. | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |

SMBus Table: Reserved Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | | Reserved | | | | 0 |
| Bit 6 | - | | Reserved | | | | 0 |
| Bit 5 | - | | Reserved | | | | 0 |
| Bit 4 | - | | Reserved | | | | 0 |
| Bit 3 | - | | Reserved | | | | 0 |
| Bit 2 | - | | Reserved | | | | 0 |
| Bit 1 | - | | Reserved | | | | 0 |
| Bit 0 | - | | Reserved | | | | 0 |

SMBus Table: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | - | | Reserved | | | | 0 |
| Bit 6 | - | | Reserved | | | | 0 |
| Bit 5 | - | | Reserved | | | | 0 |
| Bit 4 | - | | Reserved | | | | 0 |
| Bit 3 | - | | Reserved | | | | 0 |
| Bit 2 | - | | Reserved | | | | 0 |
| Bit 1 | - | | Reserved | | | | 0 |
| Bit 0 | - | | Reserved | | | | 0 |

SMBus Table: M/N Programming Enable

| Byte 9 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------------|------------------|------|---------|--------|---------|
| Bit 7 | - | M/N_Enable | M/N Prog. Enable | RW | Disable | Enable | 0 |
| Bit 6 | - | | Reserved | | | | 1 |
| Bit 5 | 5 | REFOUT_En | REFOUT Enable | RW | Disable | Enable | 1 |
| Bit 4 | - | | Reserved | | | | 0 |
| Bit 3 | - | | Reserved | | | | 0 |
| Bit 2 | - | | Reserved | | | | 0 |
| Bit 1 | - | | Reserved | | | | 0 |
| Bit 0 | - | | Reserved | | | | 0 |

SMBus Table: PLL Frequency Control Register

| Byte 10 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|------------|---------------------------------|------|---|---|---------|
| Bit 7 | - | PLL N Div8 | N Divider Prog bit 8 | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $f_{XTAL} \times [N_{Div}(9:0)+8] / [M_{Div}(5:0)+2]$ | | X |
| Bit 6 | - | PLL N Div9 | N Divider Prog bit 9 | RW | | | X |
| Bit 5 | - | PLL M Div5 | M Divider Programming bit (5:0) | RW | | | X |
| Bit 4 | - | PLL M Div4 | | RW | | | X |
| Bit 3 | - | PLL M Div3 | | RW | | | X |
| Bit 2 | - | PLL M Div2 | | RW | | | X |
| Bit 1 | - | PLL M Div1 | | RW | | | X |
| Bit 0 | - | PLL M Div0 | | RW | | | X |

SMBus Table: PLL Frequency Control Register

| Byte 11 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|------------|---|------|---|---|---------|
| Bit 7 | - | PLL N Div7 | N Divider Programming Byte11 bit(7:0) and Byte10 bit(7:6) | RW | The decimal representation of M and N Divider in Byte 11 and 12 will configure the PLL VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $f_{XTAL} \times [N_{Div}(9:0)+8] /$ $[M_{Div}(5:0)+2]$ | | X |
| Bit 6 | - | PLL N Div6 | | RW | | | X |
| Bit 5 | - | PLL N Div5 | | RW | | | X |
| Bit 4 | - | PLL N Div4 | | RW | | | X |
| Bit 3 | - | PLL N Div3 | | RW | | | X |
| Bit 2 | - | PLL N Div2 | | RW | | | X |
| Bit 1 | - | PLL N Div1 | | RW | | | X |
| Bit 0 | - | PLL N Div0 | | RW | | | X |

SMBus Table: PLL Spread Spectrum Control Register

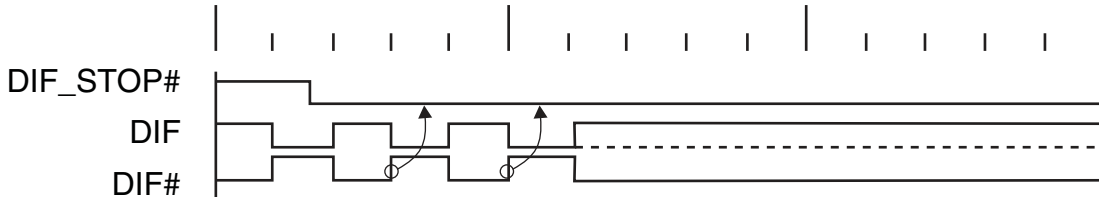
| Byte 12 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|----------|---|------|--|---|---------|
| Bit 7 | - | PLL SSP7 | Spread Spectrum Programming bit(7:0) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL | | X |
| Bit 6 | - | PLL SSP6 | | RW | | | X |
| Bit 5 | - | PLL SSP5 | | RW | | | X |
| Bit 4 | - | PLL SSP4 | | RW | | | X |
| Bit 3 | - | PLL SSP3 | | RW | | | X |
| Bit 2 | - | PLL SSP2 | | RW | | | X |
| Bit 1 | - | PLL SSP1 | | RW | | | X |
| Bit 0 | - | PLL SSP0 | | RW | | | X |

SMBus Table: PLL Spread Spectrum Control Register

| Byte 13 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|-----------|--|------|--|---|---------|
| Bit 7 | - | Reserved | | | | | 0 |
| Bit 6 | - | PLL SSP14 | Spread Spectrum Programming bit(14:8) | RW | These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage of PLL | | X |
| Bit 5 | - | PLL SSP13 | | RW | | | X |
| Bit 4 | - | PLL SSP12 | | RW | | | X |
| Bit 3 | - | PLL SSP11 | | RW | | | X |
| Bit 2 | - | PLL SSP10 | | RW | | | X |
| Bit 1 | - | PLL SSP9 | | RW | | | X |
| Bit 0 | - | PLL SSP8 | | RW | | | X |

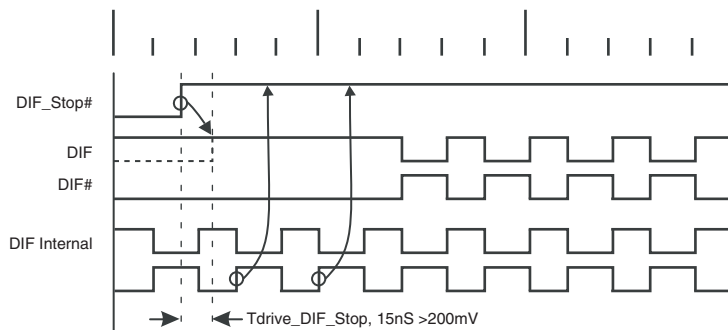
DIF_STOP# - Assertion (transition from '1' to '0')

Asserting DIF_STOP# pin stops all DIF outputs that are set to be stoppable after their next transition. When the SMBus DIF_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '0', DIF output will stop DIF_True = HIGH and DIF_Complement = LOW. When the SMBus DIF_STOP tri-state bit corresponding to the DIF output of interest is programmed to a '1', DIF outputs will be tri-stated.



DIF_STOP# - De-assertion (transition from '0' to '1')

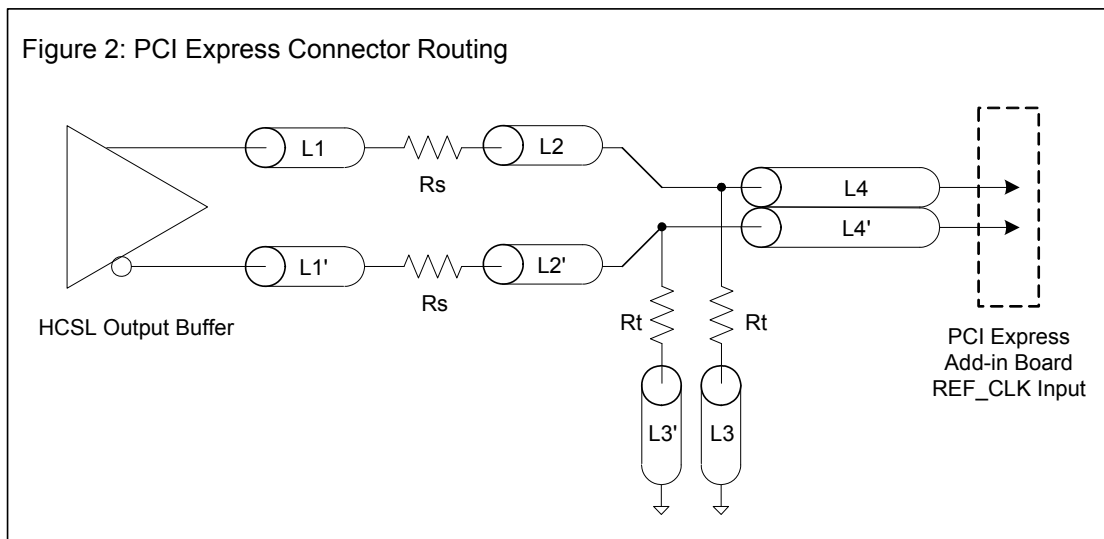
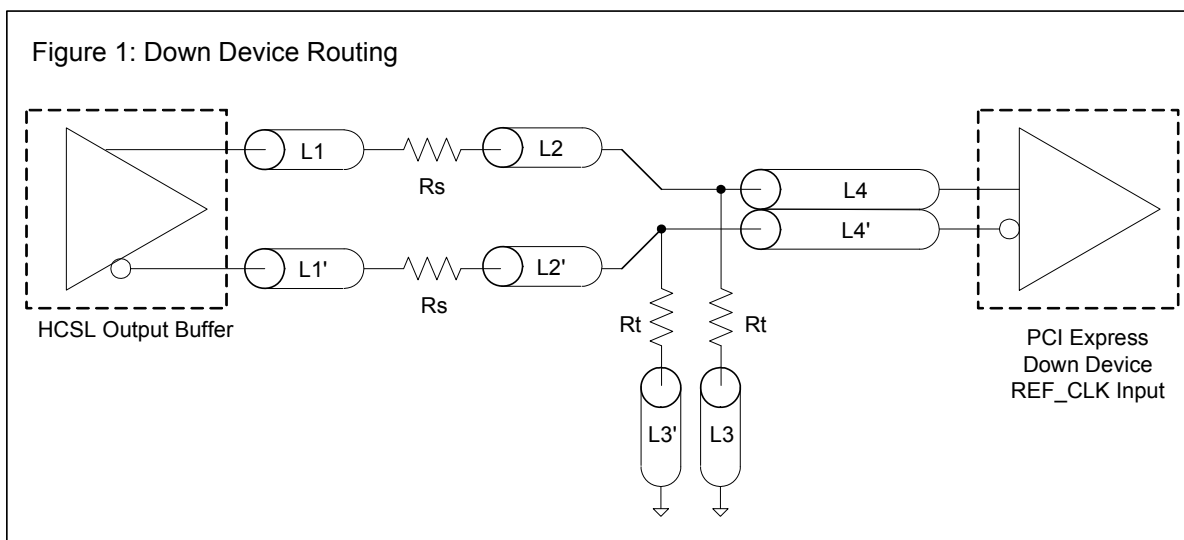
With the de-assertion of DIF_STOP# all stopped DIF outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is 2 - 6 DIF clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped DIF outputs will be driven High within 15nS of DIF_Stop# de-assertion to a voltage greater than 200mV.



| DIF Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| R_s | 33 | ohm | 1 |
| R_t | 49.9 | ohm | 1 |

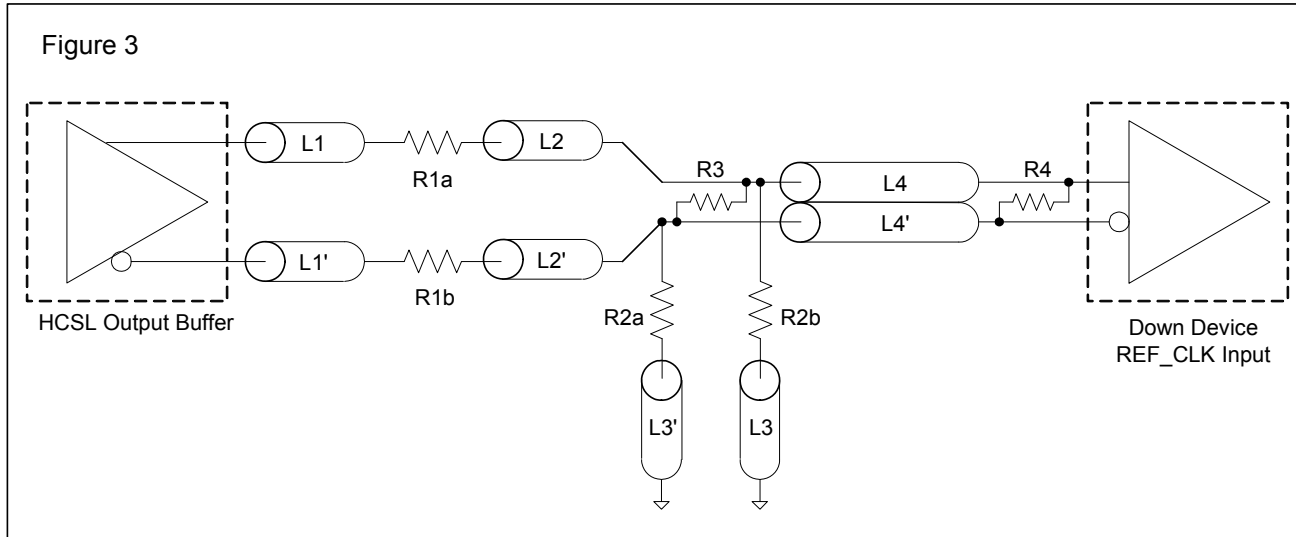
| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

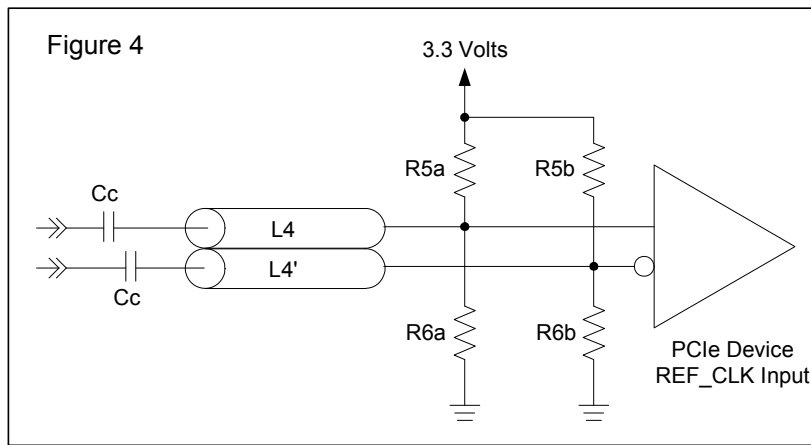


| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|-------|------|----|------|------|-----|--------------------------------|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

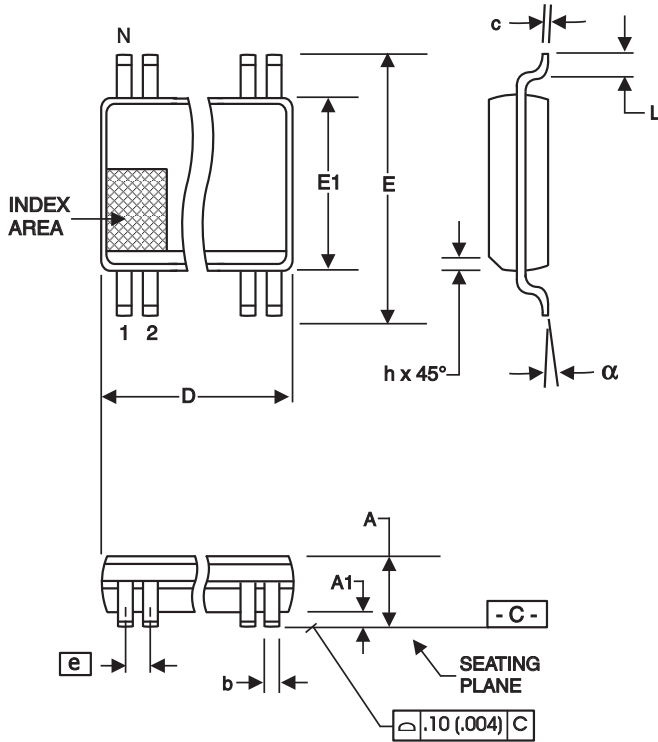
R1a = R1b = R1
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



28-Pin SSOP Package Drawing and Dimensions



209 mil SSOP

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 2.00 | -- | .079 |
| A1 | 0.05 | -- | .002 | -- |
| A2 | 1.65 | 1.85 | .065 | .073 |
| b | 0.22 | 0.38 | .009 | .015 |
| c | 0.09 | 0.25 | .0035 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 7.40 | 8.20 | .291 | .323 |
| E1 | 5.00 | 5.60 | .197 | .220 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.55 | 0.95 | .022 | .037 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

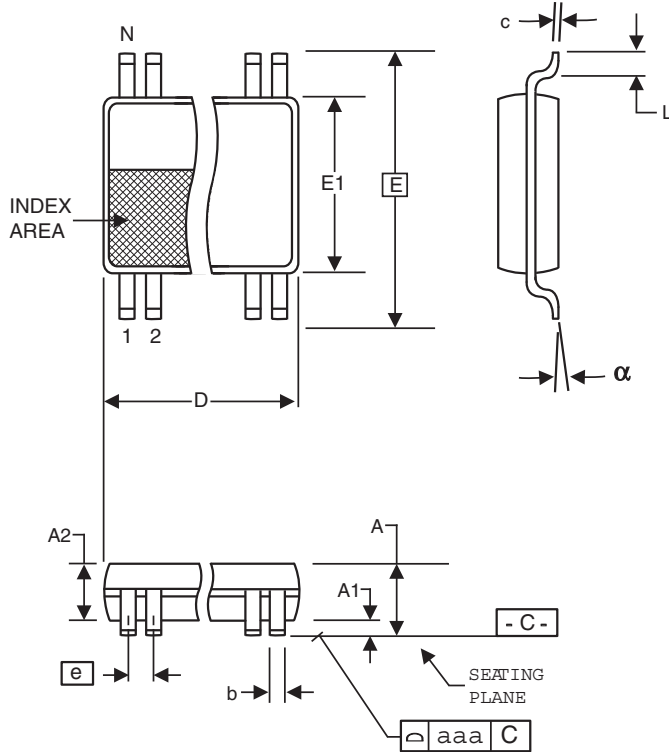
VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.90 | 10.50 | .390 | .413 |

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

28-Pin TSSOP Package Drawing and Dimensions



4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|----------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.60 | 9.80 | .378 | .386 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

| Part/Order Number | Shipping Packaging | Package | Temperature |
|-------------------|--------------------|--------------|--------------|
| 9FG104DFLF | Tubes | 28-pin SSOP | 0 to +70°C |
| 9FG104DFLFT | Tape and Reel | 28-pin SSOP | 0 to +70°C |
| 9FG104DFILF | Tubes | 28-pin SSOP | -40 to +85°C |
| 9FG104DFILFT | Tape and Reel | 28-pin SSOP | -40 to +85°C |
| 9FG104DGLF | Tubes | 28-pin TSSOP | 0 to +70°C |
| 9FG104DGLFT | Tape and Reel | 28-pin TSSOP | 0 to +70°C |
| 9FG104DGILF | Tubes | 28-pin TSSOP | -40 to +85°C |
| 9FG104DGILFT | Tape and Reel | 28-pin TSSOP | -40 to +85°C |

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|---|---------|
| 0.1 | 12/18/2008 | 1. Created Rev D data sheet from original non revision specific version. 2. Updated phase noise characteristics for Rev D. 3. Corrected footnote reference to ppm on CPU Electrical Characteristics | |
| 0.2 | 4/1/2009 | 1. Updated PPM footnotes 2. Modified input frequency ranges for each setting of the SEL14M_25M# input. | Various |
| A | 5/14/2009 | 1. Corrected/Added Tstab for Industrial Temperature Range 2. Corrected/Added REF cyc-cyc jitter for Industrial Temperature Range 3. Move to final | 4, 6 |
| B | 11/8/2010 | 1. Corrected PIN TYPE on pin 24. Changed pull up pull down designators to ^ and v respectively | 2, 3 |
| C | 12/16/2010 | Updated VDD Supply Voltage specs | 4 |
| | | | |
| | | | |
| | | | |

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales

800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support

408-284-6578
pcclockhelp@idt.com

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe

IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339



www.IDT.com