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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H7N0602LD, H7N0602LS, H7N0602LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

ADE-208-1526C (Z)

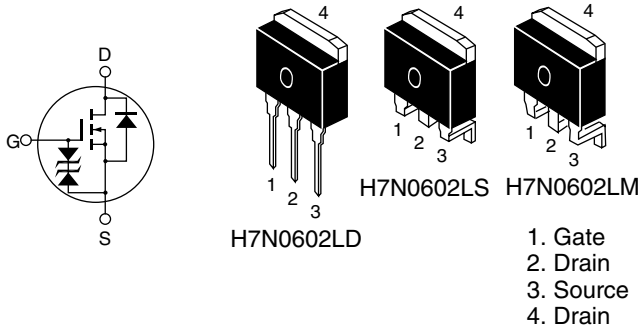
4th. Edition
May 2002

Features

- Low on-resistance
 $R_{DS(on)} = 4.1 \text{ m}\Omega$ typ.
- 4.5 V gate drive devices
- High Speed Switching

Outline

LDBPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	85	A
Drain peak current	I_D (pulse) ^{Note1}	340	A
Body-drain diode reverse drain current	I_{DR}	85	A
Avalanche current	I_{AP} ^{Note3}	65	A
Avalanche energy	E_{AR} ^{Note3}	362	mJ
Channel dissipation	Pch ^{Note2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at Tc = 25°C

3. Value at Tch = 25°C, Rg $\geq 50 \Omega$

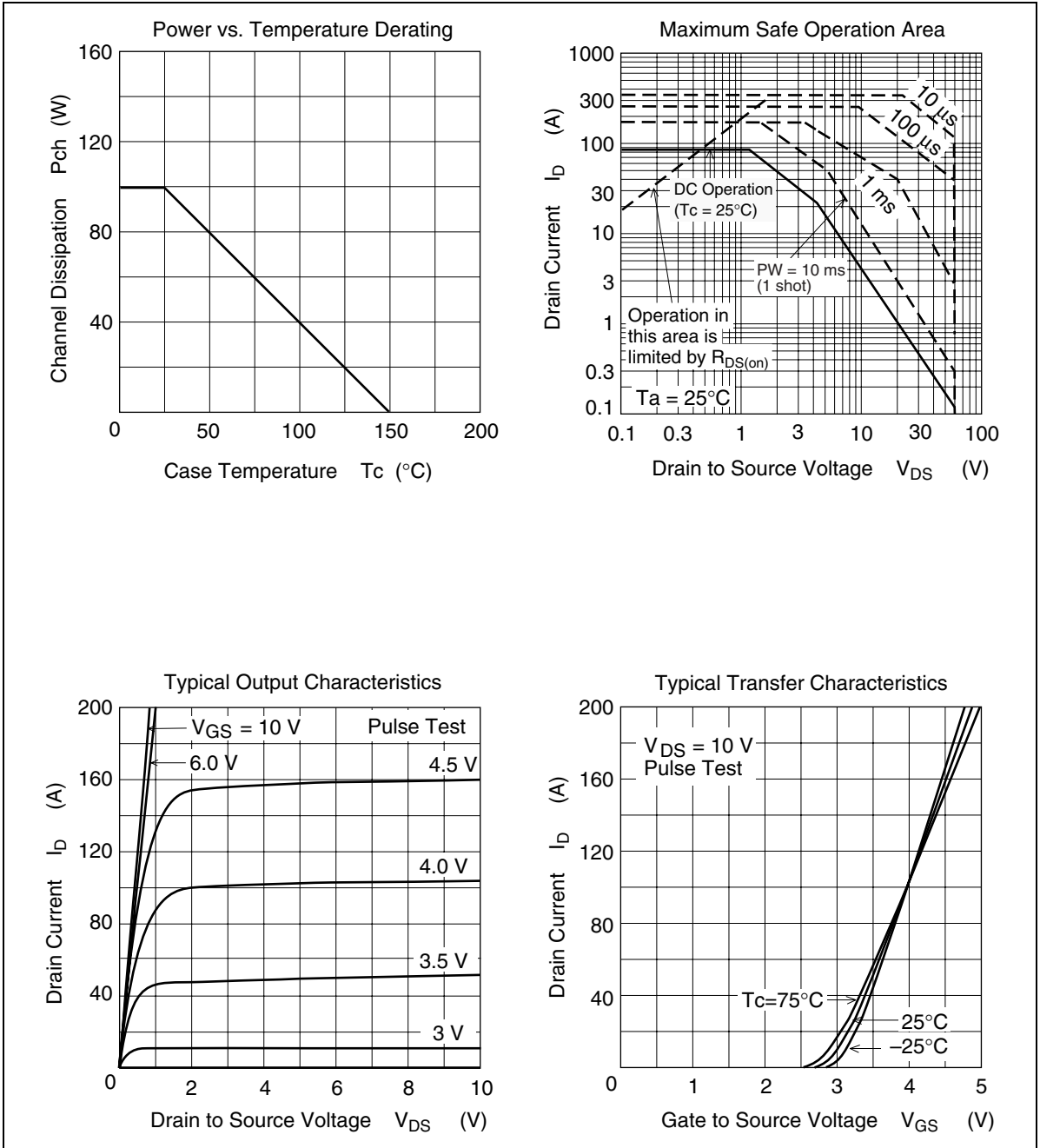
Electrical Characteristics

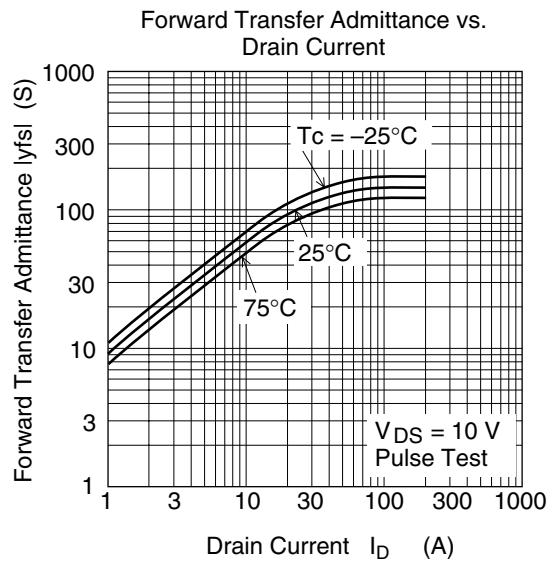
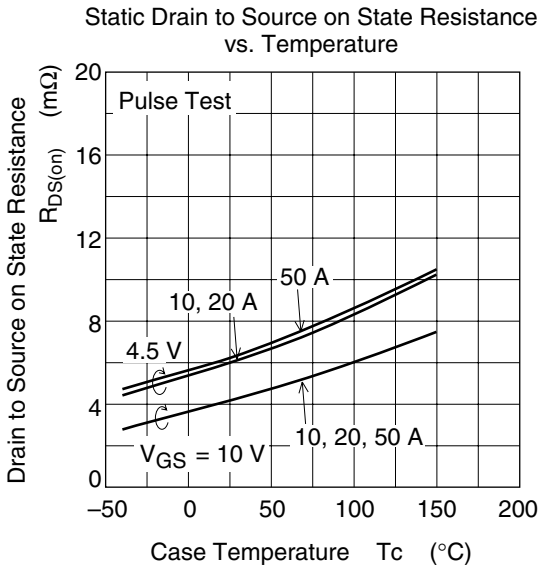
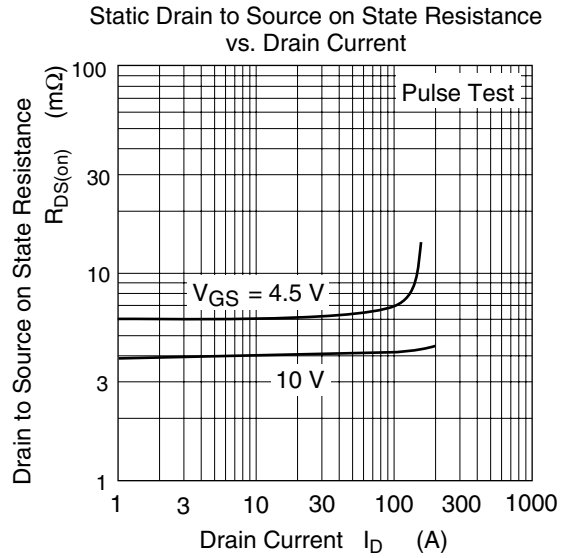
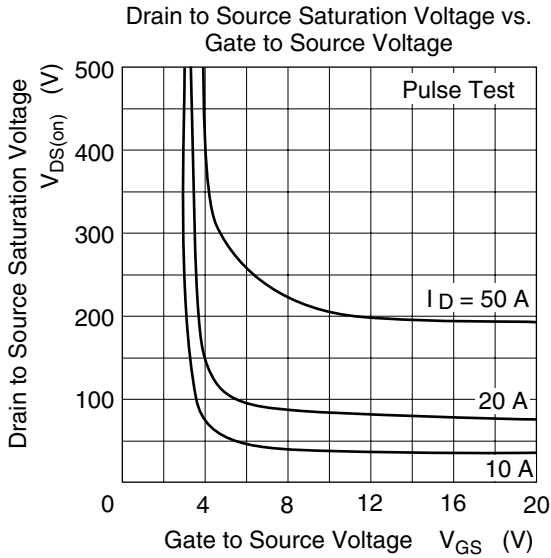
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu\text{A}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}^{\text{Note 1}}$
Forward transfer admittance	$ y_{fs} $	70	120	—	S	$I_D = 45 \text{ A}, V_{DS} = 10 \text{ V}^{\text{Note 1}}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.1	5.2	mΩ	$I_D = 45 \text{ A}, V_{GS} = 10 \text{ V}^{\text{note 1}}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.2	9.0	mΩ	$I_D = 45 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note 1}}$
Input capacitance	C_{iss}	—	9000	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	1000	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	470	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	140	—	nc	$V_{DD} = 25 \text{ V}$
Gate to source charge	Q_{gs}	—	30	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	30	—	nc	$I_D = 85 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	55	—	ns	$V_{GS} = 10 \text{ V}$
Rise time	t_r	—	290	—	ns	$I_D = 45 \text{ A}$
Turn-off delay time	$t_{d(off)}$	—	140	—	ns	$R_L = 0.67 \Omega$
Fall time	t_f	—	50	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.95	—	V	$I_F = 85 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	$I_F = 85 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

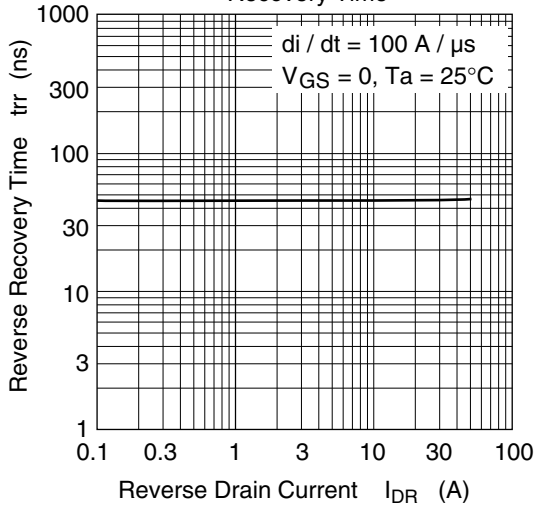
Notes: 1. Pulse test

Main Characteristics

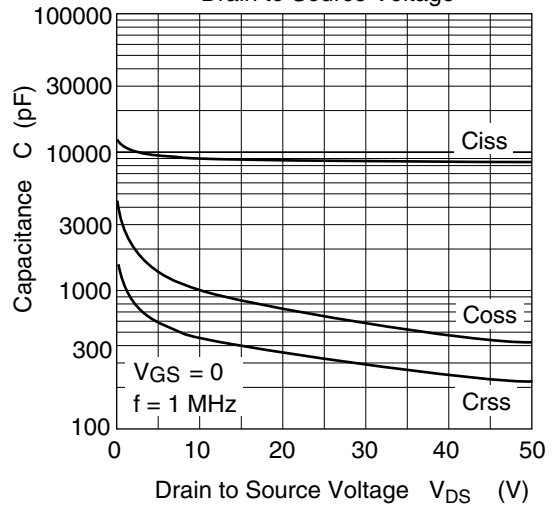




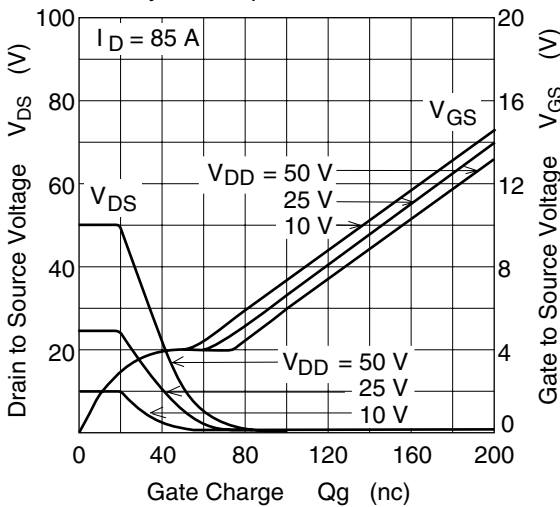
Body-Drain Diode Reverse Recovery Time



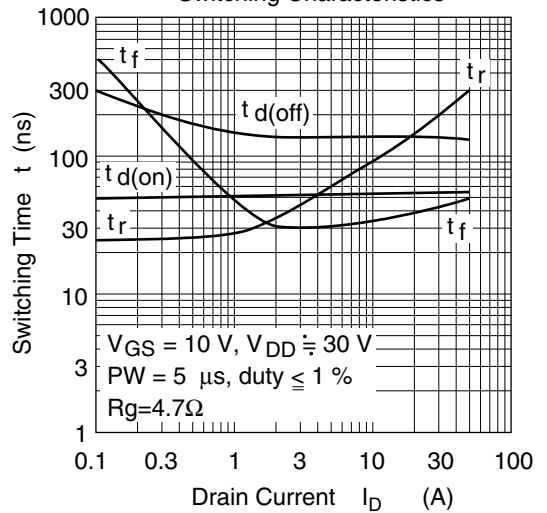
Typical Capacitance vs. Drain to Source Voltage

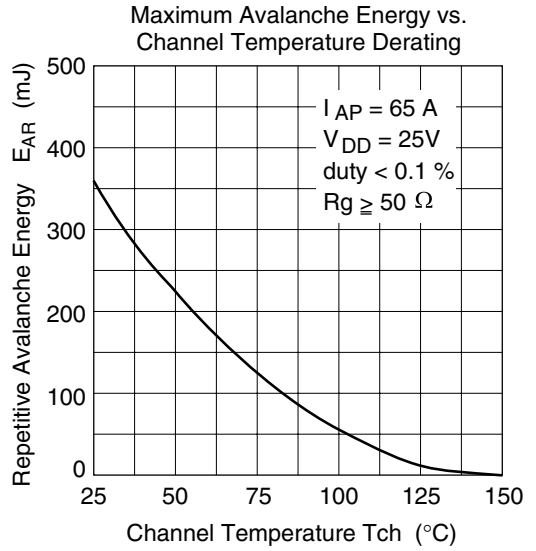
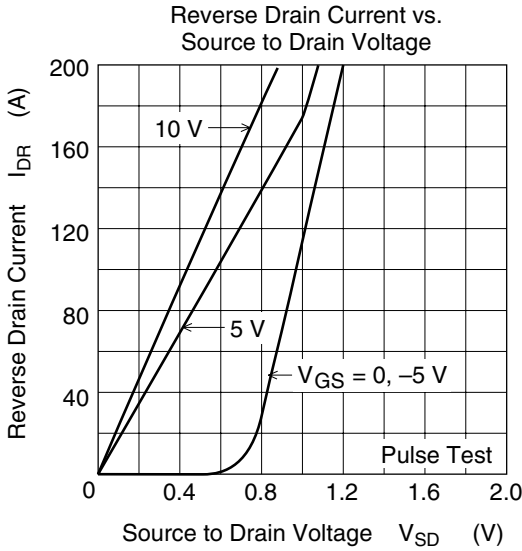


Dynamic Input Characteristics

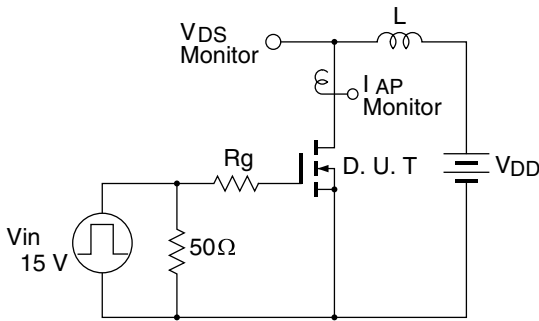


Switching Characteristics



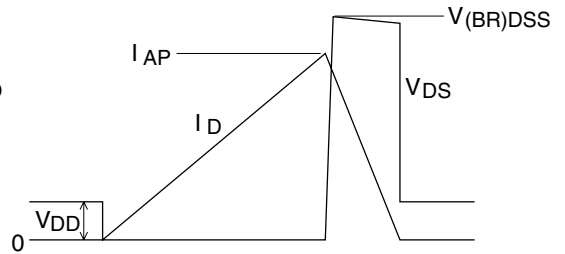


Avalanche Test Circuit

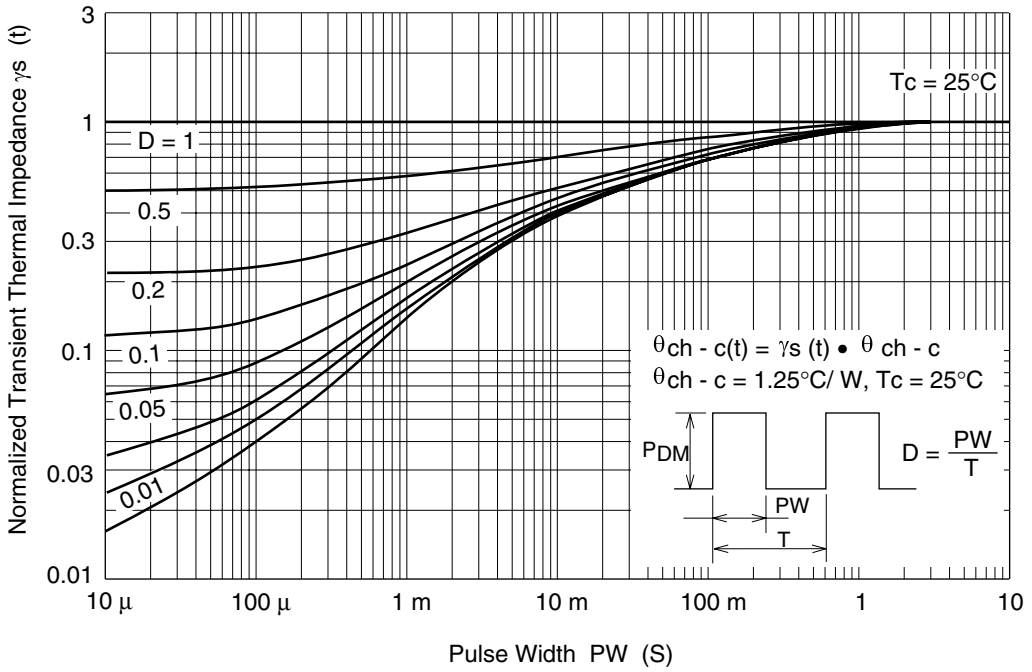


Avalanche Waveform

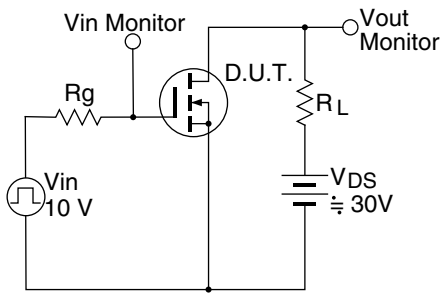
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



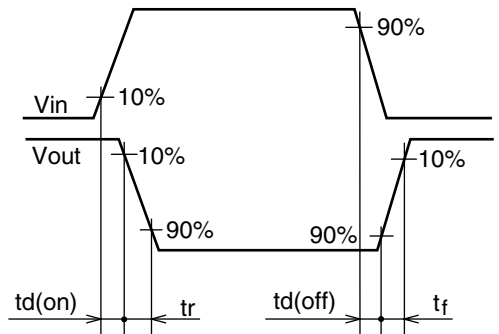
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

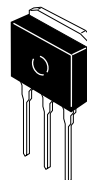
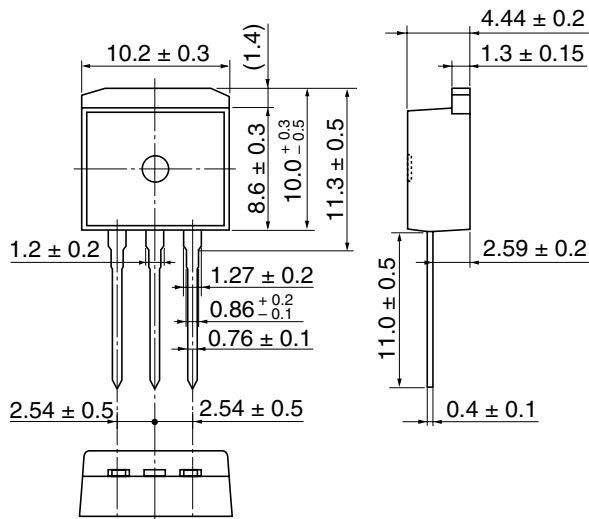


Waveform



Package Dimensions

As of January, 2002
Unit: mm

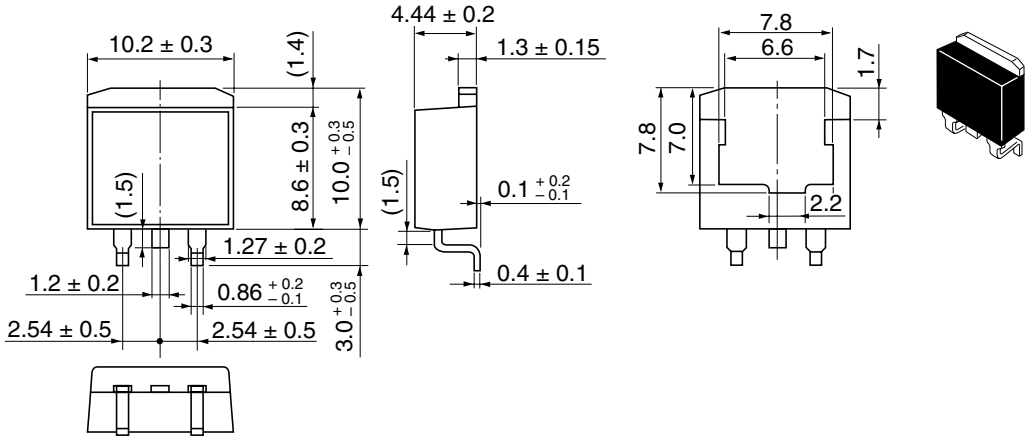


Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

H7N0602LD, H7N0602LS, H7N0602LM

As of January, 2002

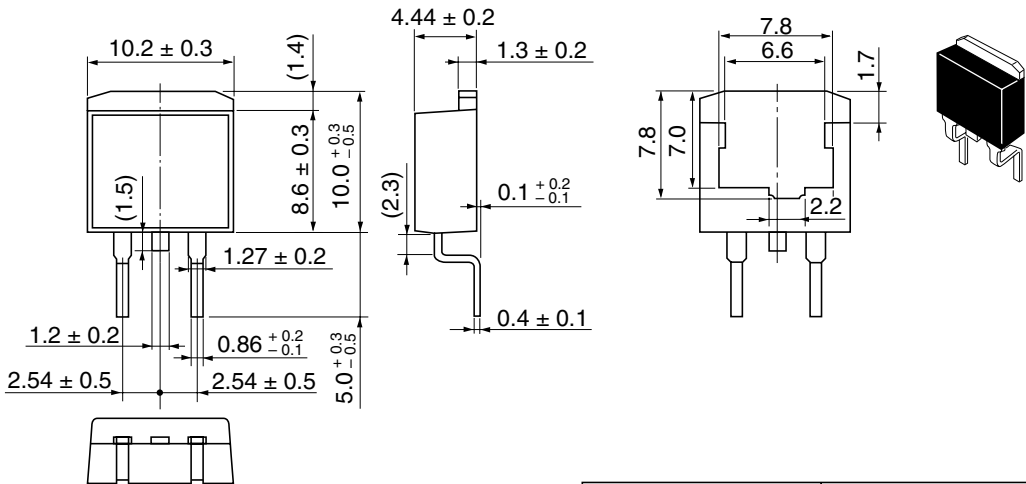
Unit: mm



Hitachi Code	LDK (S)-1
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

As of January, 2002

Unit: mm



Hitachi Code	LDK (S)-2
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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